

# Modules Subsystems



# How to Find Product Data in This Databook

The Databook contains Data Sheets for all products recommended for new designs, lists of Available Products not databooked here (data sheets upon request), and a Substitution Guide for products no longer available, plus Selection Guides and a wealth of background information.

# THERE ARE TWO VOLUMES

VOLUME I contains technical data on our integrated circuits and hybrids for data acquisition. VOLUME II has all data-acquisition products manufactured in the form of modules, cards, instruments, discrete-assembly subsystems and systems.

## DO YOU KNOW THE MODEL NUMBER?

If you know the model number, turn to the product index on page 1-18 (back of book) and look up the model number. You will find the Volume, Section, and Page location of data sheets bound into Volume I and Volume II.

If you're looking for a form-and-function-compatible version of an integrated circuit or hybrid product originally brought to market by some other manufacturer (second source), add our "AD" prefix (or "ADSP", for digital signal processing ICs) and look it up in the index.

# IF YOU DON'T KNOW THE MODEL NUMBER

There are two ways to find a device to perform your function:

### 1. FIND YOUR FUNCTION IN THE LIST ON THE OPPOSITE PAGE OR ON PAGE 2-1

Turn directly to the appropriate Section (or Volume). You will find one or more functional Selection Guides at the beginning of the Section. The Selection Guides will help you find the products that are closest to satisfying your need, and their Volume-Section-Page locations. Use them to compare all products in the category by salient criteria, no matter which Volume their technical data resides in.

# 2. IF THE FUNCTION IS NOT LISTED BY A NAME THAT YOU RECOGNIZE

Find it in the diagram (opposite page). It will help you find the Selection Guides for products in that functional category. Then use the Selection Guide(s) to find the Volume-Section-Page locations of products that will come closest to satisfying your need.

# A RELATED PRODUCT MAY BE WHAT YOU REALLY WANT

Text in each section often mentions related or complementary product categories having a greater or lesser degree of functional integration.

# IF YOU CAN'T FIND IT HERE . . . ASK!

See Worldwide Service Directory, 1-16 and 1-17, at the back of this volume.

# ANALOG DEVICES

# DATA-ACQUISITION DATABOOK 1984

# VOLUME II MODULES-SUBSYSTEMS

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# DATA-ACQUISITION DATABOOK 1984

# VOLUME II MODULES-SUBSYSTEMS

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Specifications and prices shown in this Databook are subject to change without notice.

Products in this book may be covered by one or more of the following patents. Additional patents are pending. See individual data sheets for further information:

U.S.: 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,747,088, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,872,466, 3,887,863, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,270,118, 4,268,759, 4,286,225, 4,309,693, 4,313,083, 4,323,795, 4,338,591, 4,349,811, 4,363,024, 4,374,314, 4,383,222, 4,395,647, 4,399, 345, 4,400,689, 4,400,690, DES 233,909. U.K.: 964,513, 1,310,591, 1,310,592, 1,364,233, 1,470,673, 1,470,674, 1,537,542, 1,531,931, 1,571,869, 1,590,136, 1,590,137, 1,599,538, 2,008,876, 2,012,135, 2,032,659, 2,040,087, 2,050,740, 2,081,040. France: 70.10561, 71.28952, 74.25263, 75-27557, 76 01788, 76 08238, 77 20799, 79 24021, 80 00960, 111 833. West Germany: 20 14 034, 21 39 560, MR 9379. Italy: 933,798. Japan: 452,263, 1,092,928, 1,101,824, 1,180,463. Canada: 984,015, 1,006,236, 1,025,558, 1,035,464, 1,054,248, 1,141,034, 1,141,820, 1,143,306, 1,150,414, 1,153,607, 1,157,571. Sweden: 7603320-8.

# General Information

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# **General Introduction**

Analog Devices designs, manufactures, and sells worldwide sophisticated electronic components and subsystems for use in precision measurement and control. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including bipolar, I<sup>2</sup>L, CMOS, and hybrid integrated circuits-and assembled products in the form of potted modules, printed-circuit boards, and instrument packages.

State-of-the-art technologies have been utilized (and, in many cases, invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Nearly twenty years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The continuing application of present state-of-the-art and the invention of future state-of-the-art processes strengthens the leadership position of Analog Devices in data-acquisition products.

## **MAJOR PROGRESS**

Since the publication of our two-volume 1982 Databook and its 1983 companion update volume, nearly 50 significant new products have been introduced. They are identified by bullets ( $\bullet$ ) in the index and in the table of contents for each section of this Databook. Examples of these new products include: The AD7226 Quad DAC - 4 bus-interfaced voltage-output 8-bit DACs on a single monolithic CMOS chip; the AD670 8-bit "ADCPORT," a complete ready-to-go monolithic µP-compatible 8-bit a/d converter with on-chip instrumentation amplifier; the AD667 complete 12-bit voltage-output D/A converter with 2µs voltage-settling time; the AD9700 monolithic DAC for raster displays; the ADSP-1110 single-port 16-bit multiplier/accumulator for digital signalprocessing; and the complete, expandable, stand-alone µMAC-5000 single-board measurement-and-control system, programmable in powerful µACBASIC.

### **MODULES-SUBSYSTEMS**

The list of product-category "bleed tabs" opposite the "How to Find It" Guides on the inside front cover of this Volume is a functional summary of our modular and board-level component, subsystem, and instrument classes. The complete table of contents, starting on page 2-1, provides a detailed panorama of products and functions, irrespective of technology, appearing in both Volumes of this Databook.

## **TECHNICAL SUPPORT**

Analog Devices offers extensive technical literature, which discusses the technology and applications of products for precision measurement and control. Besides comprehensive data sheets, of which there are many outstanding examples in this book, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several serial publications, including *Analog Dialogue*, our technical magazine, which provides in-depth discussions of new developments in analog and digital circuit technology as applied to data-acquisition and control, and MCDigest for users of subsystems and systems. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to data-book catalogs–such as this one–we also publish several short-form catalogs, on specific product families. You will find typical publications described on page 1-15 at the back of the book.

### SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Service Directory appears on pages 1-16 and 1-17 at the back of the book.

## PRODUCTS NOT CATALOGUED HERE

For maximum usefulness to designers of new equipment, without unwieldy size, we have limited the contents of the Databook to products most likely to be used for the design of new circuits and systems. If the data sheet for a product you are interested in is not in either Volume turn to page 1-13, at the back of this book, where you will find a list of older products for which data sheets are available upon request. On page 1-14 you will find a guide to substitutions for products no longer available.

### PRICES

At Analog Devices, we recognize that accurate, up-to-date prices of our products are an important consideration in making a choice among the many available product families. However, since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

(this section continues at the back of the book)

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# **Ordering Guide**

# INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

- 1. Find the correct part number for the options you want.
- 2. Get a price quotation and place an order with us.
- 3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

## MODEL NUMBERING

Many of the data sheets in the Databook have an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. Part numbering systems for ICs and hybrids will be found in Volume I, Section 3. If there is any question, call us.

## **ORDERING FROM ANALOG DEVICES**

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with Norwood. Orders and requests for quotations may be telephoned, sent via TWX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. On all orders under fifty dollars (\$50.00), a five-dollar (\$5.00) processing charge is required.

When prepaid, orders should include \$2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

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VOL. II, 3-2 ORDERING GUIDE

# **Operational Amplifiers**

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# **Selection Guide Operational Amplifiers**

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High CMR	>100dB	•							Company 1			
Low Offset Voltage	≤5mV ≤1mV ≤50µV	•		•	•	•	•	•	•	•	•	
Low Offset V, vs. Temp	≪5μV/°C ≪1μV/°C ≪0.6μV/°C				•	•	•	•				
Low Bias Current	≪50pA ≪5pA ≪0.5pA	•	•	•	•	•	•	•	•			
Fast Settling	≤1µs to 0.1% ≤5µs to 0.01%			_			•	•				
Wideband (Unity Gain)	≥2MHz ≥10MHz	•					•	•		•		
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Low Offset Voltage	≪5mV ≪1mV ≪50μV	•	•	•		•	•		•	•	•	•	•	•	
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Low Bias Current	≤50pA ≤5pA ≤0.5pA				100 p.e. 1 100 p.e. 1 219 - 119				•	•	•	•	•	•	
Wideband (Unity Gain)	>500kHz >2MHz				•	•		•	•						
High Slew Rate	≥10V/µs ≥30V/µs ≥100V/µs ≥1000V/µs					•		•							
Low Noise (0.1 to 1 $\leq 4\mu V p p$ $\leq 2\mu V p p$ $\leq 1\mu V p p$	OHz)		•	•			•	•	:		•	•		•	
High Voltage Out High Current Out Low Power	≥100V ≥20mA ≤75mW									•	•	•	•		
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NOTE <sup>1</sup> Chopper Stabilized

Shading indicates new product since publication of 1982-1983 Databook Update.

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# Selection Guide Operational Amplifiers

Fast/Wideband	1 .		[		2	7		FET IN	 PUT		7			7	UNITY GAIN BUFFER
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Multi-Device Technology	Hybrid Module				•	•	•	•	•	•	•	•	•	•	
High Open Loop Gain	≥100dB ≥140dB	•				•	•	•		•	٠				]
High CMR	>100dB														]
Low Offset Voltage	≤5mV ≤1mV ≤50μV	•	•		•	•	•	•	•		•	•	•	1	
Low Offset V, vs. Temp	≪5μV/°C ≪1μV/°C ≪0.6μV/°C			,   _ ,		•	•								1
Low Bias Current	≤50pA ≤5pA ≤0.5pA					•	•	•				•	•		
Fast Settling	≤1µs to 0.1% ≤5µs to 0.01%	•	•	•	•	•	•	•	•	•	•	•	•	•	1
Wideband (Unity Gain)	≥2MHz ≥10MHz ≥50MHz	•	•	•	•	•	•	•		•	•	•	•.	•	
High Slew Rate	≥10V/µs ≥30V/µs ≥100V/µs ≥1000V/µs	•	•	•	•	•	•	•	•	•	•	•	•	•	
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High Voltage Out High Current Out Low Power	≥100V ≥20mA ≤75mW	•			•		•	•	•	•	•		•	•	
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# **Orientation** Operational Amplifiers

The amplifiers listed in the two volumes of this catalog are intended to provide cost-effective solutions to the bulk of op-amp requirements in precision measurement and control, as well as to more-general requirements in electronic circuits. The technical data included in these books\* cover the properties of some 36 op-amp families, comprising more than 100 distinct types. Some are general purpose, others provide nearoptimum performance for specific classes of applications.

They differ in a variety of ways, for example, circuit technology, circuit architecture, input properties, output properties, operating temperature range, degree of isolation, and in terms of the many performance specifications. Some are high-performance modules, most are monolithic ICs (including precision dual devices), some are hybrid ICs.

The technical data in this volume embrace exceptionally highperformance (low-drift and high-speed) operational amplifiers, in the form of small encapsulated modules. As the Selection Guide indicates, there is also a universe of technical data, to be found in Volume I, on a wide range of monolithic and hybrid operational amplifiers—including devices screened to the requirements of MIL-STD-883B and chips for hybrid assembly.

### BACKGROUND

The operational amplifier is today the most-widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control), and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 4-16 a bibliography that should make available up to 99% of information need now and then, with "fanout" to the vast body of literature that – with some redundancy – will provide the remainder. It should come as no surprise to successful users of Analog Devices op amps that a number of the references are to the applications sections of data sheets included in Volume I or Volume II of this catalog.

## SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section

\*In addition to the products listed in the Selection Guide, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

1. A complete definition of the design objectives. Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.

2. Firm understanding of what the manufacturer means by the numbers published for the parameters. Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured and then must be able to interpret these published specifications in terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishing the circuit architecture, (2) defining the performance levels, and (3) choosing the amplifier(s).

1: To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier, or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks", and linear circuit books, as well as in application notes and data sheets.

2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps, and establish acceptable ranges of parameters, and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high-frequency performance and transient behavior of the op-amp block (and its effect on the closedloop circuit) for large and small signals. It will be helpful to develop an application checklist, which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy – static and dynamic – and the environmental conditions.

3. The designer must then relate acceptable performance of the op-amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications, and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows the next section.

#### APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

- *Character of the application:* The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier.
- Chopper stabilized amplifiers, for example, have not often been generally applicable where differential inputs are required.
- Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or a current source? Range of amplitude? Source impedance? Time/frequency characteristics?
- *Environmental conditions:* What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?
- Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, dc offset, and other parameters.

### SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas — bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the DC discussions below. The reader is then returned to an expanded discussion of gainbandwidth considerations.

Gain Bandwidth Considerations, A Capsule View Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

> A) If DC information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and all of the "drift" specifications may usually be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where DC information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. For example, if the closed-loop gain is 1000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

#### Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the DC offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed earlier as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

1. What input impedance must the circuit present to the signal source? This depends primarily on the source impedance,  $R_s$ , and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance,  $R_i$  and the upper limit on the magnitude of  $R_i$  is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance of the amplifier  $R_{cm}$ .

2. How much drift error can be tolerated? The question is related to the input signal level,  $e_s$ , and the required accuracy For example, to amplify or otherwise manipulate a DC input signal of one volt with an accuracy of 0.1%, the offset drift error,  $V_d$ , must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be  $100\mu V$ .

When this has been defined, the allowable limits of offset

voltage  $(e_{os})$ , bias current  $(i_b)$ , and difference current can be calculated by the equations of Figure 1. These equations relate offset voltage  $(e_{os})$ , bias current  $(i_b)$ , difference current  $(i_d)$  and the external circuit impedances to the drift error, V<sub>d</sub>, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, a referred

offset error voltage,  $i_b R_i = e_{out} \left(\frac{R_i}{R_f}\right)$ , is generated by the

bias current flowing through the feedback impedance. This error increases for increasing  $R_i$ . Since  $R_i$  also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for  $R_i$  can be used with an amplifier which has lower bias current.



Signal Input Drift Error = V

Input Impedance R<sub>IN</sub> ≈ R<sub>i</sub>

% Drift Error = 100Vd





% Drift Error = 
$$\frac{100V_d}{P_c}$$

Figure 1B. Noninverting Configuration

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through  $R_s$  for the noninverter and this will always be less than the input impedance,  $R_i$ , of the inverter. Input impedance of the noninverter (approximately  $R_{CM}$ ) is typically 10<sup>7</sup> ohms even for the least expensive bipolar amplifiers and up to 10<sup>11</sup> ohms for FET types.

Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offset can usually be zeroed at room temperature so that only the maximum temperature excursion ( $\Delta T$ ) from +25°C need be considered. For example, over the range of -25°C to +85°C, the maximum temperature excursion ( $\Delta T$ ) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

#### Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor,  $R_f$ , and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas,  $R_f$  in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance,  $R_{cm}$ , for the noninverting amplifier with temperature will cause variable loading on  $R_f$  and hence a change in sensitivity.



Figure 2A. Current Amplifier



#### Figure 2B. Voltage Amplifier with Sampling Resistor

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance  $R_{\rm IN}$  becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current,  $i_s$ . To obtain the drift of error current  $I_e$  referred to the input, use the following expression.

$$\Delta \mathbf{I}_{\boldsymbol{\mathcal{E}}} = \left[\frac{\Delta \boldsymbol{e}_{os}}{\Delta T} \left(\frac{\mathbf{R}_{f} + \mathbf{R}_{s}}{\mathbf{R}_{f} \mathbf{R}_{s}}\right) + \frac{\Delta \mathbf{i}_{B}}{\Delta T}\right] \Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current,  $I_e$ , over the operating temperature which is small compared to the signal current,  $i_s$ . Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the DC and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/µsec, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R<sub>f</sub> were one megohm, and stray capacitance, C<sub>S</sub>, were one picofarad then the closed loop bandwidth would be limited to 160kHz ( $1/(2\pi R_F C_S)$ ) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C<sub>S</sub> can be charged which in turn is related to signal level, e<sub>s</sub>, and input impedance, R<sub>i</sub>, by de<sub>0</sub>/dt = -e<sub>s</sub>/R<sub>i</sub>C<sub>s</sub>. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R<sub>i</sub> and R<sub>f</sub> must be large to obtain high input impedance. Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for  $R_1$  and  $R_2$ . Therefore, a low impedance can be used for  $R_2$  so that stray capacitance of  $C_s$  will not limit the circuit's bandwidth. In this case the minimum value for  $R_2$  is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.

For greater emphasis wideband applications can be separated into two categories – steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

#### A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. Is DC coupling required? If DC information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output DC offset. Your only concern here is that DC offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for AC signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at DC as shown in Figure 3. The gain of these circuits can be small at DC but large at high frequencies.



### Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. What closed loop gain and bandwidth are required? Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth,  $f_{c1}(-3dB)$ . For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade, each at lower gain. 3. What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary? The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ( $A\beta = A/G$ ). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ( $A\beta$ ) is the determining factor in performance. Some of the more notable examples of this point are as follows:



Figure 4. Closed Loop Bandwidth and Loop Gain

- a. Closed loop gain stability = △G/G
  △G/G = (△A/A) [1/(1 + Aβ)] where △A/A is the open loop gain stability, usually about 1%<sup>o</sup>C.
- b. Closed loop output impedance =  $Z_{ocl} = Z_o/(1 + A\beta)$ , where  $Z_o$  is the open loop output impedance, often 200 to 5000 ohms.
- c. Ciosed loop nonlinearity =  $L_{cl} = L_{ol}/(1 + A\beta)$ , where  $L_{ol}$  is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at DC and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. What full power response and/or slew rate are required? You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed  $f_p$ , the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected DC offsets at the output of the amplifier. For some monolithic amplifier designs available today their frequency response is not a simple 6dB roll-off; the response may be shaped with external RC components for improved performance, using a *compensation* terminal provided. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

### **B.** Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

### Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.



Figure 5. Typical Settling Time Characteristics

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, ideally linear, 6dB/octave amplifier with a closed loop bandwidth of  $\omega_{cl}$ is shown in Figure 6.

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However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed loop parameter, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar – i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.



Figure 6. Step Response for Linear 6dB/Octave Amplifier

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

### **ERRORS DUE TO NOISE**

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The root-square sum of these (uncorrelated) noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. A quiet power supply (nonswitching), adequate shielding, and low-pass filters on all incoming leads will usually prevent noise pick-up. Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:  $e_n = \sqrt{4 \text{KTBR}}$ 

where  $e_n$  = the rms value of the noise voltage

- $K = Boltzmann's Constant (1.38 \times 10^{-23} joules/kelvin)$
- T = absolute temperature of the resistance, kelvin

B = the bandwidth in which the noise is measured Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unwieldy for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

#### **Rules of Thumb**

(1) Remember that a  $100k\Omega$  resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n (rms) = (40 nV/\sqrt{Hz}) \left(\sqrt{\frac{R}{100 k\Omega}} (BW)\right)$$

(2) To convert the rms noise to a p-p value, a conversion factor of  $6.6\mu V$  p-p/ $\mu V$  rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.

(3) The total rms noise contribution due to several uncorrelated random noise sources is determined by the square root of the sum of the squares (RSS):

$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \dots + e_n^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately 5%.

(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

# DESIGN EXAMPLE

Figure 7A illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in RSS fashion.

Figure 7B illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, model 261J, the lowest noise non-inverting chopper type amplifier is being used with a 50k $\Omega$  source impedance. The two major noise sources, in addition to the 261J input voltage noise of 1 $\mu$ V p-p, are the Johnson noise (58 $\mu$ V p-p) and current noise (100 $\mu$ V p-p).



TOTAL NOISE =  $\sqrt{(e_{R_{JN}} G)^2 + [e_{R_S} (G+1)]^2 + e^2_{R_F} + [(i_{n_1} R_F)^2] + [(i_{n_2} R_S) (G+1)]^2 + [e_n (G+1)]^2}$ 







### THE SELECTION GUIDE

To assist the designer in rapidly distinguishing among the many types available from Analog Devices, and to narrow the field of further study to just a few types, the Selection Guide takes the form of a "bullet chart". One axis comprises a list of key op-amp characteristics—including manufacturing technology—and specification ranges; the other is the complete set of op-amp families catalogued in both volumes. For any specification level that can be satisfied by members of a given device family, a bullet (•) is placed at the appropriate intersection.

Once the required performance has been established, the Selection Guide is used to find the family, or families, coming closest to the requirements—or to determine quickly whether a particular family is suitable. The exact volume, section, and page location of each type is included in the table, so that the detailed technical and application data can be consulted with a minimum of effort.

An effort has been made to group the amplifiers by their most salient application areas, i.e., General Purpose (low cost), High Accuracy, and Fast/Wideband, and by appropriate subclasses within those major classes.

### THE AMPLIFIERS IN THIS SECTION IN BRIEF

High-Accuracy Low-Drift Differential-Input Modules. "Chopperless" low-drift designs with differential FET inputs, optimized for voltage offset and drift, bias current, de openloop gain, and CMR, should be considered for high-accuracy instrumentation, low-level transducer bridge circuits, precision voltage comparators, and for impedance buffer designs. The best overall performer in this group in high-impedance applications is the model 52K, which combines low offset and drift (0.5mV and  $1\mu$ V/°C) with 3pA bias current.

High-Accuracy Modules Using Chopper Techniques. The amplifiers in this class are widely accepted as the best choice when it is essential to maintain low voltage offsets and bias currents with time and temperature or whenever external offset adjustments are not practical in the application. Using carrier modulation techniques, these designs achieve drifts to  $0.1\mu V/^{\circ}C$  and long-term stability to  $\frac{1}{2}\mu V/mo$ . Typical applications include error-summing amplifiers for servo loops, precision regulators, and input amplifiers for laboratory-grade metering instruments and test equipment.

Two forms of amplifier are available. The *noninverting chopper-amplifier* (261 family) is a high gain feedback amplifier, containing a MOSFET chopper, optimized for follower-withgain applications. The chopper converts the difference between the dc or low-frequency input voltage, at high impedance, and the feedback voltage to a high-frequency square-wave, amplifies it with no drift, and demodulates and filters the result to produce an output waveform that is an amplified version of the input. The closed-loop gain is determined by the attenuation ratio of the feedback resistor-pair.

The initial offset is  $\pm 25\mu V$  max (trimmable to zero), with average drift-vs.-temperature of  $0.1\mu V/^{\circ}C$  max (model 261K). Bias current is respectable, at 300pA max, with a tempco of  $10pA/^{\circ}C$  max, to minimize errors with high-impedance sources.

Maximum noise voltage is  $0.4\mu V$  peak-to-peak, from 0.01 to 1.0Hz, and  $1.0\mu V$ , from 0.01 to 10Hz. Small-signal bandwidth, established by an external compensating capacitor that is chosen as a function of gain, is 100Hz.

Inverting chopper-stabilized amplifiers (234/235 family) employ narrow-band chopper amplifiers to measure the summingpoint voltage of the main amplifier (which should be at a null), chop, amplify, filter, and feed to the positive input of the main amplifier an amplified correction signal. Thus, the offset voltage and drift of the main amplifier (including the effects of input bias current) are reduced by the gain of the chopper amplifier, without a corresponding reduction of bandwidth. Chopper and chopper-stabilized amplifiers should be considered when long-term stability must be maintained with time and temperature, and wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include amplification of microvolt-level signals, precision integration, and analog computing.

Wide Bandwidtb, Fast-Settling Modules. High-speed op amps are characterized by high slewing rates, fast settling time, and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data, in buffers, d/a converters, and multiplexer circuitry, wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimal distortion, since the large-signal bandwidth is closely related to the slewing rate.

The products in this category with outstanding specifications are models 50J/K and 48J/K. Model 50's max slewing rate is 500V/ $\mu$ s inverting, 400V/ $\mu$ s noninverting, and small-signal unity-gain bandwidth is 70MHz; full-power bandwidth is 8MHz, min. In addition, these devices will deliver ±100mA of output current at ±10V, an important factor in video and line-driver circuitry, and in driving capacitive loads. For example, the current required to sustain 500V/ $\mu$ s in a 100pF load is I = C dV/dt = 50mA. Model 48J/K is optimized for settling time: 500ns maximum to 0.01%, inverting or noninverting, with output of ±20mA at ±10V.

Differential FET-Input Higb-Out Modules. This beefy group includes models 50, 51, and 171. Models 50 and 51 will furnish up to  $\pm 100$ mA at  $\pm 10V$  out. In addition both are excellent wideband amplifiers. Besides the applications suggested for them in the wide-bandwidth category, they are useful for such applications as current booster/buffer for op amps dealing with low-level signals—either outside the loop or inside the loop. They are protected against short circuits.

For extended-temperature-range operation, model 51A/B operates from -25 °C to +85 °C.

The model 171 has a large output voltage swing, ±140V at ±10mA, when used with ±150V supplies. However, it need not operate symmetrically; any combination of power-supply voltages between the limits of 15 to +300V for the positive side and -15 to -300V for the negative side is acceptable (including single-supply operation), provided that the total voltage across the amplifier is within the range of 30 to 300V. The output will swing to within 10V of the Vs<sup>+</sup> and Vs<sup>-</sup> supply rails. The output and both inputs are protected against short circuits to common or to either supply. Model 171K has an open-loop gain of 10<sup>6</sup> min, offset of 1mV, drift of  $15\mu V/^{\circ}C$  max, bias current of 20pA max, CMR of 100dB min, unity-gain smallsignal bandwidth of 3MHz, and slewing rate of  $10V/\mu$ s. Typical applications include high compliance-voltage current source, high-voltage follower-with-gain, high-voltage integrator, differential amplifier for high-common-mode-voltage bridge applications, and high-voltage reference supply.

Isolated Operational Amplifier Module. Model 277 (see Section 5) combines a high-performance uncommitted operational-amplifier input stage with a precision, isolated output stage, an isolated dual  $\pm 15$ V power supply, and transformercoupled isolation circuitry, to form a versatile isolation amplifier. It is rated to withstand input/output common-mode voltage of 3500V rms max (60Hz, 1 minute), and peak continuous ac or dc of  $\pm 2500$ V max, and has input-output CMR of 160dB min at dc and 120dB min at 60Hz, with leakage current of  $1\mu$ A @ CMV of 115V rms, 60Hz ( $Z_L = 10^{12} \Omega$ ||16pF).

The input-stage performance makes many op-amp applications feasible:  $\pm 1\mu V/^{\circ}C$  max offset tempco (trimmed, model 277K), bias current of  $\pm 20nA$  max, open-loop gain of 106dB min. In addition, isolated power output of  $\pm 15mA$  max at  $\pm 15V$ , referred to input common, is available for auxiliary front-end circuitry. The output stage has gain of 1V/V, nonlinearity of 0.05% max, 1.5kHz full-power bandwidth, and  $50\mu V/^{\circ}C$ offset tempco.

Typical applications for the 277 include general isolated opamp circuitry, programmable-gain isolated amplifier, isolated power source and amplifier for bridge measurements, instrumentation amplifier, instrumentation-grade process-signal isolator, and current-shunt measurements.

The extended-temperature-range equivalent of models 277J/K is model 277A.

# **DEFINITIONS OF SPECIFICATIONS**

#### Absolute Maximum Differential Voltage

Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, in some applications, such as voltage comparators, the voltage between the inputs can become large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

#### **Common-Mode Rejection**

An ideal operational amplifier responds only to the difference voltage between inputs  $(e^+ - e^-)$  and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode rejection is often expressed logarithmically: CMR (in dB) = 20 log<sub>10</sub> (CMRR).

The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified (on the other hand, the incremental CMR may be less in the neightborhood of large CMV). Published CMR specifications for op amps pertain to very low-frequency voltages, unless specified otherwise; CMR decreased with increasing frequency.

# Common-Mode Voltage, Maximum

For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Commonmode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connection.

## Drift vs. Supply

Offset voltage, bias current, and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

#### Drift vs. Temperature

Offset voltage, bias current, and difference current all change, or "drift", from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature ranges); the slopes generally are greater at the extremes of temperature than around normal ambient ( $+25^{\circ}$ C), which generally means that for small temperature excursions in the vicinity of  $+25^{\circ}$ C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more-) point measurements, at 25°C and at the high and low extremes of the range ( $T_H$ ,  $T_L$ ), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drifts in the two ranges must be less than the specified drift rate ( $\mu$ V/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less



than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").

The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

## Drift vs. Time

Offset voltage, bias current, and difference current change with time as components age. It is important to realize that drift with time is random, and rarely – if ever – accumulates linearly for healthy devices. For example, voltage drift for a chopper-stabilized amplifier might be quoted at  $1\mu V/day$ , whereas cumulative drift over 30 days might not exceed  $5\mu V$ , or  $15\mu V$ in a year (e.g., model 235). A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

#### Full-Power Response

The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the smallsignal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a pre-determined distortion level. There is no industry-wide accepted value for the distortion level which determines the full-linear-response limitation, but we use 3% as a maximum acceptable limit for modules.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a moreserious effect (often overlooked) is an effect equivalent to a dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often of interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

#### Initial Bias Current

Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average*. For single-ended amplifiers (i.e., chopper types), bias current refers to the current at the input terminal.

Analog Devices specifies initial bias current,  $I_b$ , as the bias current at either input, specified at +25°C ambient with the input junctions at normal operating temperature (some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each  $10^{\circ}$ C increase; since junction temperatures may warm up to  $20^{\circ}$ C or more above ambient, the "initial bias current" spec used by some manufacturers may be met only during a brief interval after the power is burned on, and I<sub>b</sub> may be quadrupled under ordinary operation conditions.)

### Initial Difference Current

Difference current is defined as the difference between the bias currents at the two inputs. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal resistance loads at both inputs.

#### Input Impedance

Differential input impedance is defined as the impedance between the two input terminals at  $+25^{\circ}$ C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry). However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the non-inverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

#### Input Offset Voltage

Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output, and dividing the measured value by the gain.

The initial offset voltage is specified at  $+25^{\circ}$ C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

#### Input Noise

Input voltage- and current-noise characteristics can be speci-

fied and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. The primary difference is that, when evaluating noise performance, bandwidth must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise", resistor noise, or junction noise, at various frequencies.

For this reason, several noise specifications are given. Lowfrequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3  $\sigma$  uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some types, spectral-density plots or "spot noise", at specific frequencies, in  $\mu V/\sqrt{Hz}$  or  $pA/\sqrt{Hz}$ , are provided.

### Open-Loop Gain

Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response*.

#### Overload Recovery

Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

#### Rated Output

Rated output voltage is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

#### Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A fullscale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extrawide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

#### Slewing Rate

The slewing rate of an amplifier, usually in volts per microsecond  $(V/\mu s)$ , defines the maximum rate of change of output voltage for a large input step change.

### Unity-Gain Small-Signal Response

Unity-gain small-signal response is the frequency at which the open-loop gain falls to 1V/V, or 0dB under a specified compensation condition. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification. For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and non-inverting configurations. However, if feedforward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

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- "How to Test Operational Amplifier Parameters", Application Note Section 20 of Volume 1

USEFUL TUTORIAL MATERIAL IN DATA SHEETS

Electrometer Circuitry, see AD515

High-Speed Amplifiers, see AD518 and Models 50/51

Low-Drift Differential Op Amp Performance, see AD504

Low-Level Applications of Chopper-Stabilized Amplifiers: Inverting, see Models 234, 235 Non-Inverting, see Model 261



# Fast Settling, Wideband, 100mA Output, FET Amplifiers

# **MODELS 50 & 51**

## FEATURES

Fast Settling: 200ns max, 0.05% (50J/K) 100ns max, 0.1% (50J/K) 100mA Output: dc to 8MHz (50J/K) dc to 6MHz (51A/B) All Hermetically Sealed Semiconductors (51A/B) -55°C to +125°C Temperature Range (51A/B) 100MHz Gain Bandwidth (50J/K)

## APPLICATIONS

A to D Input Amplifier D to A Current Converter Video Pulse Amplifier CRT Deflection Amplifier Wideband Current Booster

## **GENERAL DESCRIPTION**

Models 50 and 51 are ultra fast, wideband differential FET amplifiers, designed for applications requiring fast settling time with high output current in closed loop gain configurations of 2 or greater. Model 50 offers guaranteed settling time of 100ns maximum to  $\pm 0.1\%$  accuracy and 200ns maximum to  $\pm 0.05\%$ accuracy. Model 51 features all hermetically sealed semiconductors for greater reliability and wide operating temperature range (-55°C to +125°C) with guaranteed settling times of 140ns maximum to  $\pm 0.1\%$  and 250ns maximum to  $\pm 0.05\%$ .

Model 50 is available in two input voltage drift selections. Model 50J is  $\pm 50\mu V/^{\circ}C \max$ , model 50K is  $\pm 15\mu V/^{\circ}C \max$ . Other outstanding features of models 50J/K are 100MHz gain bandwidth product, slew rate of 500V/ $\mu$ s and output current of  $\pm 100$ mA from dc to 8MHz.

Model 51 is also available in two input voltage drift selections; model 51A is  $\pm 50\mu V/^{\circ}C$  max, model 51B is  $\pm 20\mu V/^{\circ}C$  max. Models 51A/B offer 80MHz gain bandwidth product, slew rate of 400V/ $\mu$ s and  $\pm 100$ mA output current from dc to 6MHz. Both models 50 and 51 offer significant improvement over previous designs with lower input voltage noise ( $6\mu V$  rms, 5Hz to 2MHz bandwidth), particularly important in display system D/A converter applications.

## FAST SETTLING APPLICATIONS

D/A converters require fast settling output amplifiers since conversion speed is often dictated by the settling time of the amplifier. Models 50 and 51 offer fast settling time performance at closed loop gains from 2 to 6. This characteristic is extremely important for D/A applications requiring fast current to voltage conversion from less than ideal current sources.



The circuit shown in Figure 1 is that of a typical current to voltage converter. The output of the D/A converter is often considered an ideal current source  $(R_{out} = \infty)$  which is converted to a voltage by the amplifier's feedback resistor. Although it may appear that in this application the amplifier is being operated in a closed loop gain of 1, a closer look at the D/A's specifications may show an output impedance of  $\mathcal{B}00$  to 2500 ohms. For this condition, the amplifier is operated in a closed loop gain of 2 to 6. This is then the range of gains over which settling time is important.



Figure 1. High Speed Current to Voltage Buffer

High speed amplifiers typically suffer significant degradation in settling time when operated in closed loop gains greater than unity. Model 50, with 100MHz gain bandwidth and model 51 with 80MHz gain bandwidth achieve fast settling time since they are far from the point of bandwidth limitations. For example, at a gain of 4, model 50 has a bandwidth of 20MHz, which represents a time constant of 8ns. For 0.1% settling, the bandwidth limitation is 6.9 time constants or approximately 55ns.

# **SPECIFICATIONS**

MODEL	50J	50K	51A	51B
OPEN LOOP GAIN				
DC, Load = 100 ohm	88dB min		94dB min	••
DC, Load = 2k ohm	94dB min	<u> </u>	97dB min	
RATED OUTPUT				
Voltage, $R_L \ge 100\Omega$	±10V min			
Current	±100mA min			
Impedance, Open Loop de	20012	•	•	
Load Capacitance, max	100 m			•
Noninverting	SODE max	•	•	•
EBEQUENCY BEEBONEE	Jopt max			
Small Signal Unity Cain	70MU-		56MH2	••
Small Signal -2dB Unity Cain	100 MHz	•	20MHz	••
Full Power	8MHz min	•	6MHz min	••
Slew Bate Noninverting	400V/us min	·•	300V/us. min	••
Slew Rate, Inverting	500V/us min	•	400V/us min	••
Overload Recovery	200ns	•	•	•
SETTLING TIME				
Inverting, Gain = 2				
+0.1% +10 Volt Sten	100ns max	•	140ns max	••
±0.05%, ±10 Volt Step	200ns max	•	250ns max	••
Noninverting Gain = 2				
+0.1% +10 Volt Step	150ns max	•	200 ns max	••
±0.05% ±10 Volt Sten	300ns max	•	400ns max	••
INPUT OFFSET VOLTAGE				
Initial @ +25°C	Adjust to Zero	•	•	•
Trim Potentiometer	1kΩ	•	•	•
With 499 $\Omega$ Fixed Resistor	±3mV	•	•	•
vs. Temperature	±50µV/°C max	±15µV/°C max	±50µV/°C max	±20µV/°C max
vs. Supply Voltage	±15µV/%	•	•	•
vs. Time	±500µV/month	•	•	•
Warm up Drift, 20 Minutes	±2mV	•	•	•
INPUT BIAS CURRENT				
Initial, @ +25°C	0, 0-2nA max	•	•	•
vs. Temperature	Double/+10°C	•	•	•
vs. Supply Voltage	10pA/%	•	•	•
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±100pA	•	•	•
vs. Temperature	Double/+10°C	•	•	•
INPUT IMPEDANCE				
Differential	10 <sup>10</sup> Ω  3.5pF	•	•	•
Common Mode	10 <sup>1</sup> Ω  3.5pF	•		•
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	5µV, p-p	•	•	•
5Hz to 2MHz	6μV, rms	•	•	•
Current, 0.1Hz to 10Hz	1pA, p-p	•	•	• <u> </u>
INPUT VOLTAGE RANGE				
Common Mode Voltage	±10V min	•	•	•
Max Safe Differential Voltage	±Vs	• •	•	•
Common Mode Rejection, $CMV = \pm 10V$	60dB, min	•	:	
Common Mode Rejection, CMV = ±5V	70dB, min	<u> </u>	·	· · · · · · · · · · · · · · · · · · ·
POWER SUPPLY		1		
Voltage, Rated Performance <sup>2</sup>	±15V dc		•	•
Voltage, Operating	±(12 to 18)V dc	•		
Current, Quiescent	±40mA	·		
TEMPERATURE RANGE	•		0	
Rated Specifications	0 to +70°C		-25 C to +85 C	••
Operating	-25°C to +85°C		-55°C to +125°C	
Storage	-55°C to +125°C		•	-
MECHANICAL			•	
Case Size, mm	1.8" x 1.2" x 0.6"	-		:
Weight, grams	31	-	-	-
Mating Socket	AC1034	-	-	-

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



## MATING SOCKET AC1034

## UNITY GAIN APPLICATIONS

Models 50 and 51 have been optimized for fast settling inverting applications, such as current to voltage conversion at the output of D/A converters. In these configurations the high speed amplifier is usually operating in a noise gain of about 5. (Noise Gain =  $1 + R_f/R_{out}$  of D/A). They have also been designed as fast noninverting amplifiers and offer excellent performance at noise gains of 2 or higher. For unity gain applications the circuits shown in Figure 2 and Figure 3 are recommended.



Figure 2. Recommended Circuit for Unity Gain Noninverting Buffer



Figure 3. Recommended Circuit for Unity Gain Inverter

NOTES

\*Specifications same as Model 50J.

\*\*Specifications same as Model 51A.

<sup>1</sup> Short circuit protected to ground.

<sup>2</sup> Recommended power supply ADI Model 920, ±15V @ 200mA.

<sup>3</sup>Model 51A and 51B have an operating temperature range of -55°C to +100°C when operating in the differential mode.

Specifications subject to change without notice.



# Low Noise, Low Drift Precision FET Amplifier

**MODEL 52** 

# FEATURES

Guaranteed Low Noise:  $1.5\mu V p$ -p max (52K). Low Voltage Drift:  $1\mu V/^{\circ}C$  max (52K) Low Bias Current: 3pA, max High CMR: 100dB, min High Voltage Gain: 120dB, min Wide Power Supply Range: ±9V to ±18V Excellent Long Term Stability:  $5\mu V$ /month Fast Thermal Response

#### APPLICATIONS

Low Level Instrumentation Preamp High Impedance Precision Buffer Long Term Integrator Current to Voltage Converter Precision Voltage Regulator Preamp for 16-Bit Resolution V/F Converters

# **GENERAL DESCRIPTION**

Model 52, a low noise, high accuracy FET input operational amplifier was designed for handling microvolt signals from high impedance (>100k $\Omega$ ) sources. It features guaranteed low voltage noise (1.5 $\mu$ V p-p max, 0.01 to 1Hz bandwidth 52K) with low input offset voltage drift (3 $\mu$ V/°C max, 52J; 1 $\mu$ V/°C max 52K). Unlike most available low drift amplifiers, model 52 voltage drift is unaffected by trimming the initial offset voltage (0.5mV max). The low input bias current (3pA max) is held constant over the entire ±10V common mode voltage range. High voltage gain (120dB, min) and high CMR (100dB, min) complete the performance profile. Model 52 is an excellent choice for high accuracy, high resolution linear signal processing applications.

By incorporating a new low noise N-channel monolithic FET input stage, thermal stability, voltage noise and differential signal performance are improved to a level previously obtainable only in the best bipolar amplifier designs. Model 52 is an excellent choice to replace chopper stabilized amplifiers where significant sources of error are introduced from zero beating, "chopper spikes" and ground loop currents.

The guaranteed accuracy performance of model 52 suggests critical applications such as low noise, low drift "front-end" preamplifiers for A to D converters and DVM's. For high impedance buffering applications, model 52 offers low input bias current, high linear common mode rejection, complete protection from input transients (offset voltage and bias current will not degrade due to reverse breakdown) and freedom from latch up when the common mode voltage range is exceeded. Model 52 is supplied in a reliable, compact epoxy module package. Output is protected from shorts to ground and/or supply voltage and is capable of driving up to  $0.01\mu$ F load capacitance.



#### IMPROVED OFFSET VOLTAGE STABILITY

Model 52 has been designed for the lowest possible input voltage drift over the 0 to  $+70^{\circ}$ C temperature range. In most operational amplifier designs, trimming is accomplished by unbalancing the current in the input stage. This trimming technique introduces an additional 2 to  $12\mu$ V/°C for each millivolt of E<sub>0S</sub> that is nulled. To provide performance consistent with low offset voltage drift, model 52 incorporates a three-point trim (see connection diagram) whereby a compensating voltage is introduced without unbalancing the input stage currents. By virtue of this trim scheme, there is no degradation in T.C. when E<sub>0S</sub> is nulled and the specified performance is achieved.

### IMPROVED NOISE PERFORMANCE

Input noise limits signal resolution in low level signal processing applications. The FET input stage of model 52 reduces noise current significantly from that of bipolar amplifiers, permitting high source impedance applications. Model 52 also offers voltage noise levels appreciably below that of other FET amplifiers. To illustrate the excellent low noise performance of model 52, Figure 1 shows typical input voltage noise in a 0.01 to 1Hz bandwidth. Noise is typically less than  $1\mu V$  p-p and is free of noise spikes.



Figure 1. Voltage Noise 0.01 to 1Hz Bandwidth

# SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	52J	52K
OPEN LOOP GAIN		
DC 2kΩ Load	120dB min (130dB typ)	· · · · · · · · · · · · · · · · · · ·
RATED OUTPUT <sup>1</sup>		
Voltage, 2kΩ Load	±10V min	
Current	±5mA min	•
Maximum Load Capacitance	0.01µF	•
Impedance, Open Loop	/352	
FREQUENCY RESPONSE	5001-11-	•
Unity Gain, Small Signal	JUOKHZ	•
Full Power	- Ariz min	•
Overland Recovery	130 <i>us</i>	•
Settling Time, ±0.1%, ±10V Step	100µs	+
Settling Time, ±0.01%, ±10V Step	150µs	•
INPUT OFFSET VOLTAGE	······	
$Initial^2$ , @ +25°C	±500µV max	•
With External Trim Potentiometer	Adjustable to Zero	*
vs. Temperature (0 to +70°C)	±3µV/°C max	±1μV/°C max
vs. Supply Voltage	±2µV/%	•
vs. Time	±5µV/Month	•
Warm-Up Drift, 5 Minutes	±5µV	•
INPUT BIAS CURRENT	<b>1</b>	
Initial, @ +25°C	-3pA max (-1pA typ)	•
vs. Temperature (0 to +70°C)	x2/+10°C	•
vs. Supply Voltage	±0.01pA/%	•
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	±1pA	•
vs. Temperature (0 to +70°C)	x2/+10°C	•
INPUT IMPEDANCE		
Differential	$10^{12} \Omega    3.5 \text{ pF}$	•
Common Mode	10 <sup>12</sup> Ω  3.5pF	•
INPUT NOISE		
Voltage, 0.01Hz to 1Hz	3.0μV p-p	1.5µV p-p max
10Hz to 10kHz	5.0µV rms	3.0µV rms max
f = 1Hz	70nV/ <del>V Hz</del> rms	
f = 10Hz	$25 \text{nV}/\sqrt{\text{Hz}} \text{rms}$	
f = 100Hz	20nV/VHz rms	
f = 1 kHz	13nV/VHz rms	
Current, 0.01Hz to 1Hz	0.1pA p-p	•
I = IHZ	2 SFA / Hz rms	•
f = 10047	$2.51A/\sqrt{Hz}$ mis	
f = 100112	$\frac{6fA}{H7}$ rms	•
Common Mode Voltage	+10V min	
Common Mode Rejection $CMV = \pm 10V$	100dB min (106dB typ)	•
Max Safe Differential Voltage	+V-	• .
POWER SUPPLY <sup>3</sup>		
Voltage, Rated Performance	±15V	•
Voltage, Operating	±(9 to 18)V	•
Current, Quiescent	±5mA	•
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	•
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	•
MECHANICAL		
Case Size	1.12" x 1.12" x 0.4"	•
Weight	16g	•
Mating Socket	AC1008	*

NOTES

\*Specifications same as model 52].

<sup>1</sup> Protected for short circuit to ground.

<sup>2</sup> With no external trim potentiometer connected.

<sup>3</sup> Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.



Dimensions shown in inches and (mm).



<sup>1</sup>Optional 1kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim pins left open, input offset voltage will be ±0.5mV, maximum.

\*Common Supply connection not required.

### MATING SOCKET AC1008



\*No connection required on Model 52.

### FREQUENCY RESPONSE

From the plot of Open Loop Voltage Gain and Phase Shift (see Figure 2) versus Frequency, it can be seen that model 52 is stable for all closed loop gains. Even at the crossover frequency of 500kHz, model 52 has a phase margin of 75°.



Figure 2. Open Loop Frequency Response and CMR


# High Voltage Differential FET Amplifier MODEL 171

### FEATURES

High Output Voltage:  $\pm$ 140V High CMR: 100dB min Operates With a Wide Range of Power Supplies High CMV:  $\pm$ (|V<sub>S</sub>| - 10V)

### APPLICATIONS

High Voltage Compliance Current Source High Voltage Follower With Gain High Voltage Integrator Diff. Amp for High CMV Bridge Applications Reference Power Supply



### **GENERAL DESCRIPTION**

Model 171 is a high performance FET input op amp designed for operation over a wide range of supply voltages. This module features an output range of  $\pm 15V$  to  $\pm 140V$  at 10mA, a minimum CMRR of 100dB and a high common mode voltage rating of  $\pm (V_S - 10V)$  min. DC offset is less than  $\pm 1mV$ , and maximum drift of either  $\pm 50$  or  $\pm 15\mu V/^{\circ}$ C is available in the J or K versions. Bias current is less than 50pA (171J) or 20pA (171K), doubling per +10°C increase of temperature. The model 171 also features small signal bandwidth of 3MHz for unity gain, full-power bandwidth of 15kHz, and slew rate of 10V/ $\mu$ s. These operating characteristics make model 171 an excellent choice for high voltage buffer applications, followers with gain, off-ground signal measurements and reference power supplies.

Excellent power supply rejection of  $7\mu V/V$  enables model 171 to be powered by inexpensive, low regulation supplies, without sacrificing any of the 171's inherent high performance. The supplies also need not be symmetrical. Any combination of power supply voltages between the limits of 15 to +300V for the positive side and 15 to -300V for negative side is acceptable provided the total voltage across the amplifier is within the range of 30 to 300V.

Model 171's output is completely short circuit protected by the use of a current limit scheme. This type of protection provides a short circuit output that is only slightly greater than the rated output current for normal operation. With this design the module and external circuitry are protected, internal heat dissipation and the associated high temperature rise are limited, and added reliability is built in.

### POWER SUPPLY VOLTAGES

Model 171 offers the flexibility of operating with an extensive range and combination of power supply voltages. Figure 1 shows a chart of permissible combinations of supply voltages for the 171. The model 171 maintains its normal operating characteristics when using asymmetrical power supply configurations.



Figure 1. Power Supply Voltage Combinations

# SPECIFICATIONS (typical @ +25°C and ±125V unless otherwise noted)

MODEL	171J	171K
OPEN LOOP GAIN	10 <sup>6</sup> min	*
RATED OUTPUT		- <u></u>
Voltage	$\pm( V_c  - 10V)$ min	*
Current	±10mA min	*
Maximum Load Capacitance	1000pF	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	3MHz	*
Slewing Rate	10V/μs min	.*
Full Power	15kHz min	*
Settling Time to ±0.1%, ±10V Step	25µs	*
Overload Recovery	5µs	*
INPUT OFFSET VOLTAGE		
Initial Offset, +25°C <sup>1</sup>	±1mV	*
Avg. vs. Temp (0 to $+70^{\circ}$ C)	±50µV/°C max	±15μV/°C max
vs. Supply Voltage	±7μV/V	* '
vs. Time	±250µV/mo	*
INPUT BIAS CURRENT		
Initial Bias, +25°C	-50pA max	-20pA max
vs. Temp (0 to +70°C)	x 2/10°C	*
Difference Current	±10pA	±5pA
INPUT IMPEDANCE		
Differential	10 <sup>11</sup> Ω∥3.5pF	*
Common Mode	10 <sup>11</sup> Ω∥3.5pF	*
INPUT NOISE		
Voltage, 0.01 to 1.0Hz	4μV p-p	*
10Hz to 10kHz	2.5µV rms	*
5Hz to 50kHz	6μV rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±( V <sub>S</sub>  -10V) min	. *
Common Mode Rejection	100dB min	*
Common Mode Rejection	114dB	*
Max Safe Differential Voltage	±V <sub>S</sub>	*
POWER SUPPLY		
Voltage, Rated Specification	±25 to ±150V dc	*
Voltage, Operating	±15 to ±150V dc	*
Current, Quiescent	±6mA typ	*
TEMPERATURE RANGE	· ·	
Rated Specification	0 to +70°C	*
Operating /	-25°C to +85°C	*
Storage	-40°C to +100°C	*
MECHANICAL		
Case Size	2.41" x 1.82" x 0.61	*
Weight	80g	*
Mating Socket	AC1037	

NOTES

\*Specifications same as 171J.

<sup>1</sup> No external trim connection required.

Specifications subject to change without notice.

## **OUTLINE DIMENSIONS**





### MATING SOCKET

Dimensions shown in inches and (mm).



### MATING SOCKET AC1037

SINGLE SUPPLY OPERATION As shown in Figure 1, the model 171 requires at least ±15 volts applied across it in order to operate properly. The 171 may be operated from a single floating supply voltage by using the power supply offsetting scheme shown in Figure 2. When this configuration is used, the 171 is capable of operating over its specified input and output voltage range.



Figure 2. Single Supply Operation



# Low Noise Chopper Stabilized Amplifiers

**MODELS 234, 235** 

FEATURES

Ultra-Low Noise:  $0.7\mu$ V p-p, 0.01Hz to 1Hz BW (234)  $0.5\mu$ V p-p, 0.01Hz to 1Hz BW (235) Very Low Offset Drift:  $0.1\mu$ V/°C, 1pA/°C (234L)  $0.1\mu$ V/°C, 0.5pA/°C (235L) Excellent Long Term Stability:  $5\mu$ V/year (235) Fast Settling:  $4\mu$ s to 0.01%, 2.5MHz BW (235)

APPLICATIONS

Precision Integration Servo/Null Detector Loops Microvolt/Picoamp Measurements Bridge Amplifier Controlled Current Source Balance Scales and Weighing Instruments



### GENERAL DESCRIPTION

Analog Devices' models 234, 235 are high performance, economy chopper-stabilized op amps that meet the demands of critical laboratory and industrial applications requiring ultra-low noise, exceptional long term offset stability and versatility. Both models feature compact plug-in modular design, and are ideally suited for new design applications, or upgrading of existing systems, where both improved performance and cost savings can be realized.

Model 234: The model 234 is designed for wideband applications and features  $10^7 \text{ V/V}$  open loop gain, 2.5MHz unity gain bandwidth, full power response to 500kHz and settling time of 4µs (to 0.01%, 10V step, 20k $\Omega$  load). The model 234 also features low input voltage noise of  $0.7\mu\text{V}$  p-p (0.01Hz to 1Hz BW), low offset voltage drift of  $1\mu\text{V/}^{\circ}\text{C}$  (234J),  $0.03\mu\text{V/}^{\circ}\text{C}$ (234K) or  $0.1\mu\text{V/}^{\circ}\text{C}$  (234L) and long term stability of  $\pm 2\mu\text{V/}$ month.

Incorporating MOSFET choppers and discrete components (vs. IC op amps) for the main and stabilizing amplifier channels, this inverting design is virtually free of input chopper spikes and offers reduced modulation ripple for quieter wideband performance. These characteristics are especially desirable when operating from high source impedances (above  $100k\Omega$ ) at wide bandwidths. To illustrate the improvements in noise and bandwidth performance, over previous Analog Devices' designs, comparative data is set forth in the following sections comparing models 232 and 233 with 234.

Model 235: The model 235 is recommended for applications where lowest cost and lowest noise are required. The model 235 features low input voltage noise of  $0.5\mu V p$ -p (0.01Hz to 1Hz BW), low offset voltage drift of  $0.5\mu V/^{\circ}C$  (235J),  $0.25\mu V/^{\circ}C$  (235K),  $0.1\mu V/^{\circ}C$  (235L) and a long term stability of  $5\mu V/y$ car.

This combination of noise and drift performance makes model 235 ideally suited for demanding applications such as balance scales and weighing instruments requiring high accuracy and excellent long-term stability without the use of "front panel" balance pots or periodic internal adjustment.

Model 235 has been designed to virtually eliminate intermodulation problems caused by "beating" against power line frequencies. The chopper's ultra-stable oscillator is precisely set at the factory to a frequency that minimizes ineractions with harmonics of 50Hz, 60Hz and 400Hz power lines.

### APPLICATIONS

In general, the models 234, 235 inverting amplifiers should be considered where long term stability of offset voltage must be maintained with time and temperature for precision designs, or wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include low drift amplification of microvolt signals, integration of low duty-cycle pulse trains and analog computing for general purpose designs. Low input noise and stable offset voltages also make 234, 235 an ideal preamp for precision low frequency applications such as DVMs, 12- to 16-bit A to D converters, and for error amplifiers in servo and null detector systems.



Figure 1. Model 234 Comparative Input Noise (RTI) Performance in a dc to 1kHz Bandwidth

# SPECIFICATIONS

+15V unloss otherwise noted) - -

MODEL	234J	234K	234L	235J	235K	235L
OPEN LOOP GAIN DC , 2k ohm load	10 <sup>7</sup> V/V min	•	•	5 x 10 <sup>7</sup> V/V min	**	**
RATED OUTPUT						
Voltage	±10V min	*	•	•	•	•
Current	±5mA min	•	•	•	•	•
Load Capacitance Range	0-1000pF min	•	•	0.01µF	**	** .
FREQUENCY <sup>1</sup>						
Unity Gain, Small Signal	2.5MHz	•	•	1MHz	**	••
Full Power Response	500kHz min	•	•	5kHz min	**	••
Slew Rate	30V/µs	•	•	0.3V/µs min	**	•• .
SETTLING TIME to 0.01% 20kΩ load, 10V step	4µs	•	• '	N/A	N/A	N/A
INPUT OFFSET VOLTAGE						
Initial Offset <sup>2</sup>	±50uV max	±20µV max	±20µV max	±25µV max	••	±15µV max
vs. Temp. 0 to $+70^{\circ}$ C	$\pm 1.0 \mu V/^{\circ} C max$	$\pm 0.3 \mu V/^{\circ} C max$	$\pm 0.1 \mu V/^{\circ} C max$	$\pm 0.5 \mu V/^{\circ} C max$	$\pm 0.25 \mu V/^{\circ} C max$	$\pm 0.1 \mu V/^{\circ} C max$
vs. Supply Voltage	±0.2µV/%	•	•	±0.1µV/%	**	**
vs. Time	±2µV/month	•	•	±5µV/vear	••	**
vs. Turn On, 10 sec to 10 min	±3µ∨	•	•	•	•	•
INPUT BIAS CURRENT						
Initial, @ +25°C	±100pA max	•	•	•	±50pA max	±50pA max
vs. Temp, 0 to +70°C	±4pA/°C max	±2pA/°C max	±1pA/°C max	1pA/°C max	0.5pA/°C max	0.5pA/°C max
vs. Supply Voltage	±0.5pA/%	•	•	0.2pA/%	••	**
Inverting Input to Signal Ground	300k ohms	•	•	•	•	•
INPUT NOISE						
Voltage, 0.01 to 1Hz	0.7 <i>u</i> V n-n	•	•	0.5µV p-p	2uV p-p max	2µV p-p max
0 1 to 10Hz	1.54V p-p	•	•	3.5µV p-p	**	••
10Hz to 10kHz	2uV rms	•	•	5µV rms	++	••
Current 0.01 to 1Hz	2 pA p-p	•	•	10pA p-p	**	**
0.1 to 10Hz	4pA p-p	•	•	30pA p-p	••	••
INPUT VOLTAGE RANGE					•	
(-) Input to Signal Ground	±15V max	•	•	•	•	•
POWER SUPPLY (V dc) <sup>3</sup>					······	
Rated Performance	±15V @ 5mA	*	•	•	•	•
Operating	±(12 to 18)V	•	•	•	•	•
TEMPERATURE RANGE				-	·····	
Rated Specifications	$0 to +70^{\circ}C$	•	• •	•	•	•
Operating	$-25^{\circ}$ C to $+85^{\circ}$ C	•	•	•	•	•
Storige	$-25^{\circ}$ C to $+100^{\circ}$ C	•	•	$-55^{\circ}$ C to $+125^{\circ}$ C	**	••

NOTES \*Specifications same as model 234J. \*Specifications same as model 235J. <sup>1</sup> Model 235 overload récovery, 10 sec typ.



Figure 2. Model 235 Voltage and Current Noise. Model 233 Voltage Noise Shown for Comparison.

 <sup>2</sup> Externally adjustable to zero.
 <sup>3</sup> Recommended power supply: Analog Devices model 904, ±15V dc @ 50mA. Specifications subject to change without notice.

### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



NOTES: \*Connect Trim Terminal to Common if Trim Pot is not used.

1. SG Tied to Common. 2. Mating Socket AC1010.

3, Weight: 27 grams,

# **Isolation Amplifiers**

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# Selection Guide Isolation Amplifiers





## **MODEL 277**

Versatile Op Amp Front End: Inverting, Noninverting, Differential Applications

Low Nonlinearity: 0.025% max, Model 277K Low Input Offset Voltage Drift: 1µV/°C max, Model 277K

Floating Power Supply: ±15V dc @ ±15mA High CMR: 160dB min @ dc High CMV: 3500V<sub>rms</sub>

## **MODEL 289**

Low Nonlinearity: ±0.012% max (289L) Frequency Response: (-3dB) dc to 20kHz (Full Power) dc to 5kHz Gain Adjustable 1 to 100V/V, Single Resistor 3-Port Isolation: ±2500V CMV Isolation Input/Output

Low Gain Drift: ±0.005%/°C max

Floating Power Output: ±15V @ ±5mA

120dB CMR at 60Hz: Fully Shielded Input Stage Meets UL Std. 544 Leakage: 2 $\mu$ A rms max, @

115V ac, 60Hz

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## MODEL 290A

Isolated Power Supply:  $\pm$  13V dc @  $\pm$ 5mA (290A) Low Nonlinearity: 0.1% @ 10V pk-pk Output High Gain Stability: 0.001%/1000 Hours; 0.01%/°C Small Size: 1.5" × 1.5" × 0.62"

Low Input Offset Voltage Drift: 10µV/°C (Gain = 100V/V)

Wide Input/Output Dynamic Range: 20V pk-pk High CMV Isolation: 1500V dc, Continuous Wide Gain Range: 1 to 100V/V

### MODEL 292A

Multichannel Capability Using External Oscillator (292A)

Isolated Power Supply: ±15mA (292A) ·

Low Nonlinearity: 0.1% @ 10V pk-pk Output High Gain Stability: 0.001%/1000 Hours; 0.01%/°C Small Size:  $1.5'' \times 1.5'' \times 0.62''$ 

Low Input Offset Voltage Drift: 10µV/°C (Gain = 100V/V)

Wide Input/Output Dynamic Range: 20V pk-pk High CMV Isolation: 1500V dc, Continuous Wide Gain Range: 1 to 100V/V

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# Selection Guide Isolation Amplifiers





## **MODEL 284**

High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous High CMR: 110dB min with 5kΩ Imbalance

Low Nonlinearity: 0.05% @ 10V pk-pk Output High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours

Low Input Offset Voltage Drift:  $10\mu V/^{\circ}C$ , G = 100V/V

Resistor Programmed Gain: 1 to 10V/V (284J) Isolated Power Supply: ±8.5V dc @ ± 5mA (284J) Meets IEEE Std 472: Transient Protection (SWC) Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.0µA max (284J)

**MODEL 286** 

High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous

High CMR: 110dB min with 5kΩ Imbalance Low Nonlinearity: 0.05% @ 10V pk-pk Output High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours

Low Input Offset Voltage Drift: 10µV/°C, G = 100V/V

Resistor Programmed Gain: 1 to 100V/V (286J) Isolated Power Supply:  $\pm$ 15V dc @  $\pm$  15mA (286J) Meets IEEE Std 472: Transient Protection (SWC) Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.5µA max (286J) **Page** Vol. II 5–11

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VOL. II, 5-4 ISOLATION AMPLIFIERS



### 

## AD293

High Common-Mode Voltage: AD293 ±2500V peak max Nonlinearity: ±0.05% max (AD293B)

Adjustable Input & Output Gain: 1V/V to 1000V/V

Complies with NEMA ICS1-111

Hermetically Sealed Hybrid Construction

## AD294

 High Common-Mode Voltage: ±8000V
 Vol. I

 peak max
 5-13

 Nonlinearity: ±0.05% of max
 Adjustable Input & Output Gain: 1V/V to 1000V/V

 Complies with NEMA ICS1-111
 Meets UL Std 544 Leakage: 2.0µA max @

 115V ac, 60Hz
 Hermetically Sealed Hybrid Construction

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# **Orientation** Isolation Amplifiers

The isolation amplifier (or isolator) has an input circuit that is galvanically isolated from the power supply and the output circuit. Isolators are intended for applications requiring safe, accurate measurement of dc and low-frequency voltage or current in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and.line-frequency leakage must be maintained at levels well below certain mandated minima.\* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process-control systems.

Analog Devices Isolators described in this section use electromagnetically coupled high-frequency carrier techniques for communication of power to and signals from the input circuit.

### CHOOSING AN ISOLATOR

The choice of an isolator depends on the desired functional characteristics and the required specifications. Functional characteristics include such considerations as number of channels, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning), and the availability of isolated power for additional external front-end circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, an applications guide<sup>1</sup>, available upon request, provides information useful to the circuit designer.

The devices described in this section are all voltage-output isolation amplifiers, useful in general-purpose circuit applications for instrumentation amplifiers or op amps where isolation is a necessity. In addition to these devices, there are a growing number of isolators available from Analog Devices that perform dedicated functions, for use where isolation is necessary or desirable. Some of their applications can be seen in the *Transducer Interfacing Handbook*<sup>2</sup>.

Data for other products employing isolation techniques may be found in these sections of this Volume: Transducers and Signal Conditioners, Digital-to-Analog Converters, Synchro/ Resolver-Digital Converters, Digital Panel Instruments, Intelligent Measurement-and-Control Subsystems, Linear Test Systems, and MACSYM. Power Supplies and DC-DC Converters, being transformer-coupled, also provide isolation.

•Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.

 <sup>1</sup> Analog Devices "Applications Guide to Isolation Amplifiers" (1984)
 <sup>2</sup> Sheingold, D. H., ed. Transducer Interfacing Handbook-A guide to analog signal conditioning. Norwood MA 02062 (P.O. Box 796): Analog Devices, Inc., 1980, \$14.50 Examples of such products include the 2B54 Thermocouple/mV 4-Channel Multiplexer/Amplifier, the 2B22 Voltage-or-Currentto 4-to-20mA Converter, the DAC1423 10-bit Digital-to-4-to-20mA Converter, the AD2036, AD2037, and AD2038 Scanning Panel Instruments, and the  $\mu$ MAC-5000 Intelligent Measurement-and-Control Subsystems.

Functional Characteristics The figure shows the circuit architecture of a self-contained isolator, Model 289. The various models differ, but their properties can be discussed in terms of the device shown. An isolator of this type requires power from a two-terminal dc supply. An internal oscillator converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output. The ac carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and amplified, using isolated dc power, derived from the carrier.

The amplifier in this example is a resistor-protected op amp (actually, the protection works both ways - it protects the amplifier against differential overloads (120V rms continuous) and it protects sensitive input sources from supply voltage if the amplifier malfunctions), connected for a programmable gain from 1 to 100V/V, as determined by a single external resistor. Since both input terminals are floating, the amplifier functions effectively as an instrumentation amplifier. All but one of the amplifiers in this series function in the instrumentation-amplifier mode, but with various gain ranges. The 277 is an exception; its input stage is an uncommitted high-gain lowdrift, low-noise op amp, and the output terminal of the input stage is available for feedback connections to perform a wide range of single-ended or differential operations. Because of the transformer coupling, the outputs of all these devices are isolated from their input stages.



In the figure, it can be seen that the demodulator drive is magnetically coupled from the oscillator to the output stage. This permits the output to operate at a dc common-mode potential with respect to power common. An isolator of this type is said to provide *three-port* isolation, because there are three isolated ports: input, power supply, and output. The AD293 and AD294 have 3 isolated sections, but the op amp supply is tied to output common. The data sheets carry block diagrams, which show the architecture of each device; 3-port devices, in general, have an output common-mode voltage spec in the "Rated Output" section. Two-port devices are those in which there is a dc connection between the oscillator power supply and the output stage.

The 289, as can be seen, is a completely self-contained device. There are applications for which a degree of "unbundling" can lead to economy and improved performance. For example, if there are many input channels to be isolated, economies can be realized by the use of a common oscillator. In addition, the common oscillator makes it possible to avoid the possibility of small errors due to beat frequencies developed by small amounts of crosstalk. Several synchronized multichannel devices are available. Model 292A is essentially a 290A with a power amplifier instead of an oscillator. It requires a de power input and a pair of leads for a low-power oscillator input, which can be furnished by a 281 synchronizable oscillator. The 281 will drive from one to 16 292As, and it will also synchronize additional 281s for increments of up to 16 292s per 281.

### SPECIFICATIONS

The illustration on the next page shows a typical specification block and defines the specifications of key interest.

NONLINEARITY -- This is the peak deviation from a best straight line, expressed as a % of peak-to-peak output. Should be considered when signal fidelity is of prime importance.

MAX SAFE DIFFERENTIAL **INPUT** – Max voltage that can be safely applied across input terminals. Important to consider for fail-safe designs in the presence of high voltages.

**OVERLOAD RESISTANCE -**This is the apparent input impedance under conditions of amplifier saturation. It limits differential fault currents.

**INPUT NOISE** - Total noise, referred to the input. Facilitates comparison with expected signal input levels.

**ISOLATED SUPPLY** - Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input signal conditioners, front-end amplifiers, as well as remote transducers.

### Model

GAIN (NONINVERTING) Range Formula Deviation from Formula vs. Temperature (0 to +70°C) Nonlinearity, (±5V Swing)<sup>2,3</sup> INPUT VOLTAGE RATINGS Linear Differential Range (G = 1V/V) Max Safe Differential Input Continuous 1 Minute Max CMV (Inputs to Outputs) Continuous ac or de ac, 60Hz, 1 Minute Duration CMR, Inputs to Outputs 60Hz  $R_S \leq 1k\Omega$ , Balanced Source Impedance  $R_S \leq 1k\Omega$ , HI IN Lead Only Max Leakage Current, Input to Output @ 115V rms, 60Hz ac INPUT IMPEDANCE Differential Overload Common Mode INPUT DIFFERENCE CURRENT Initial @ +25°C vs. Temperature (0 to 70°C) INPUT NOISE (GAIN = 100V/V) Voltage 0.05Hz to 100Hz 10Hz to 1kHz Current 0.05Hz to 100Hz FREQUENCY RESPONSE Small Signal -3dB G = 1V/VG = 100V/VFull Power, 10V p-p Output G = 1V/VG = 100V/V Full Power, 20V p-p Output G = 1V/V G = 100V/VSlew Rate Settling Time<sup>4</sup>, ±0.05%, ±10V Step OFFSET VOLTAGE, REFERRED TO INPUT Initial. @ +25°C vs. Temperature (0 to +70°C) vs. Supply Voltage (+15V to +20V change) RATED OUTPUT Voltage, 2kΩ Load Output Impedance Output Ripple, 0.1MHz Bandwidth No Signal IN +10VIN ISOLATED POWER SUPPLY Voltage

Accuracy Current Regulation No Load to Full Load Ripple, 0.1MHz Bandwidth, No Load Full Load POWER SUPPLY, SINGLE POLARITY Voltage, Rated Performance Voltage, Operating Current, Quiescent (@ VS = +15V) TEMPERATURE RANGE Rated Performance Operating Storage

### 289K

1 to 100V/V  $G = 1 + \frac{10k\Omega}{R_G (k\Omega)}$ ±1.5% max 15ppm/°C typ (50ppm/°C max) ±0.025% max

120V rms 240V rms

±2500V peak max 2500V m 120dB

104dB min 2µA rms max

±10V min

33pF∥10<sup>8</sup>Ω 100kΩ  $20 pF\|5\times 10^{10} \Omega$ 

10nA (75nA max) 0.15nA/°C

8μV p-p 3µV rms 3pA rms

20kHz 5kHz 5kHz 3 SkHz

2.3kHz

2 3kHz

0.14V/µs 400µs <u>10</u> mV max ±5 ±

 $\pm 15 \pm \frac{100}{C}$  max  $\pm 2 \pm \frac{10}{G} \mu V/V$ 

±10V min <1Ω(dc to 100Hz)

5mV p-p 50mV p-p +15V dc

±10% ±5mA, min ±5% 25mV p-p 75mV p-p

> +14 4V to +25V +8.5V to +25V +25mA

0 to +70°C -15°C to +75°C -55°C to +85°C 1.5" × 2.0" × 0.75"

NO 125: 'Gain temperature drift is specified as a percentage of output signal level. 'Gain nonlinearity is specified as a percentage of 10V pkyk output span. 'When isolated power output is used, nonlinearity increases by 40002%/mA of current drawn. 'G = 1VV', with 2-pole, 5kHz output filter. 'Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

CASE DIMENSIONS

NOTES

CMV. INPUTS TO OUTPUTS -Voltage that may be safely applied to both inputs with respect to outputs or power common. Neces-

sary consideration in applications with high CMV input or when high voltage transients may occur at the input.

### CMR, INPUTS TO OUTPUTS -

Indicates ability to reject common mode voltages between inputs and outputs. Important when processing small signals riding on high common mode voltages.

LEAKAGE CURRENT - Maximum input leakage current when power-line voltage is impressed on inputs. Vital consideration for patient safety in medical applications.

**OFFSET VOLTAGE REFERRED** TO INPUT - Total input drift is composed of two sources (input

and output stage drifts) and is gain (G) dependent. Referring offsets to the input allows them to be compared to signal levels.

## ANALOG DEVICES Hig

## Precision Isolation Amplifier High CMV/CMR, ±15V Floating Power

**MODEL 277** 

### FEATURES

Versatile Op Amp Front End: Inverting, Non-Inverting, Differential Applications Low Nonlinearity: 0.025% max, Model 277K Low Input Offset Voltage Drift: 1µV/°C max, Model 277K Floating Power Supply: ±15V dc @ ±15mA High CMR: 160dB min @ dc High CMV: 3500V<sub>rms</sub>

### APPLICATIONS

Programmable Gain Isolated Amplifier Isolated Power Source and Amplifier for Bridge Measurements Instrumentation Amplifier Instrumentation Grade Process Signal Isolator Current Shunt Measurements

### **GENERAL DESCRIPTION**

Model 277 is a versatile isolation amplifier which combines a high-performance, uncommitted operational amplifier front end with a precision, isolated output stage and a floating power supply section. This configuration, shown in Figure 1, makes the 277 ideally suited to instrumentation applications where the need for various forms of signal conditioning, high CMV protection and isolated transducer power requirements are encountered.

The input stage is a low drift  $(\pm 1\mu V)^{\circ}C$  max, model 277K) differential op amp that may be connected for use in inverting, non-inverting and differential configurations. The circuitry employed around the operational amplifier input stage can be designed by the user to suit each application's particular signal processing needs. A full  $\pm 10V$  signal range is available at the output of the front end amplifier.



Figure 1. Transducer, Power, Gain Resistors, and Shielding Interconnection



The isolated output stage includes a special modulator/demodulator technique which provides the 277 with 160dB minimum dc common mode rejection between input and output common and an input-to-output CMV rating of  $3500V_{ms}$ . When combined with the output stage's low nonlinearity (0.05%, models 277J/A and 0.025% model 277K), these high CMR and CMV ratings facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays. In addition, model 277A offers a -25°C to +85°C rated operating temperature range. All versions of model 277 have a ±10 volt output range.

The floating power supply section provides isolated  $\pm 15$  volt outputs capable of delivering currents up to  $\pm 15$ mA. This feature permits model 277 to power transducers and auxiliary isolated circuitry, thereby eliminating the need for a separate isolated dc/dc converter.

All of the features of the model 277 isolation amplifier are packaged in a compact ( $3'' \times 2.2'' \times 0.59''$ ) module. As an assurance of high performance reliability, every model 277 is factory tested for CMV rating by application of  $3500V_{ms}$ (±4900V peak) between input and output common terminals for one minute (meets NEMA and CSA requirements for  $660V_{ms}$  service.) In addition, the 277 has a calculated MTBF of 133,000 hours.



Figure 2. Model 277 Functional Block Diagram

# **SPECIFICATIONS** (typical at +25°C and ±15V unless otherwise noted)

MODEL	277j	277K	277A
INPUT STAGE PERFORMANCE <sup>1,2</sup>	10/10		
OPEN LOOP GAIN	106dB min	•	•
INPUT OFFSET VOLTAGE	t1 SmV max	•	•
vs. Temperature	-1.501 * 104X		
Offset Untrimmed	±5µV/°C max	•	±5µV/°C
Offset Trimmed to Zero	±3µV/°C max	±1µV/°C max	•
vs. Supply voltage	±30µv/v ±3.5µV/mo	•	
INPUT BIAS CURRENT	- 515 (4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		
Initial, @ +25°C	±20nA max	•	•
vs. Temperature	±50pA/°C	•	•
vs. Supply Voltage	±100pA/V	•	•
INPUT DIFFERENCE CURRENT	·		
Initial, @ +25 C	±6nA ±50nA/V		:
	230pA/V	·····	
Differential	4ΜΩ	•	•
Common Mode <sup>3</sup>	100MΩ∥4pF	•	•
INPUT NOISE			
Voltage, 0.01Hz to 10Hz	1μV p-p	•	•
10Hz to 1kHz	3µV rms	:	•
		·	<u> </u>
INPUT VOLTAGE RANGE Common Mode Voltage <sup>3</sup>	+10V min	•	•
Common Mode Rejection <sup>3</sup> , CMV = $\pm 10V$ , 60Hz	100dB	•	•
Max Safe Differential Voltage	±13V	•	•
ISOLATED POWER SUPPLY <sup>4</sup>			
Voltage/Current <sup>2</sup>	±15V @ ±15mA max	•	•
Load Regulation (No Load – Full Load)	+0, -6%	•	•
Line Regulation	1V/V 20mV p.p @ 70kUz		
	Somv p-p @ 70kHz		
OUTPUT STAGE PERFORMANCE	11/0/	•	•
Gain Error	±0.5% max	•	•
vs. Temperature	±50ppm/°C max	•	•
Nonlinearity, ±10V Output	±0.05% max	±0.025% max	•
VOLTAGE RATINGS <sup>5</sup>			
Max CMV, Output Com/Input Com			
Nonrecurring Spike (<1 Second)	3500V <sub>mns</sub> max	:	:
Peak ac or dc. Continuous	±2500V pk max	•	•
CMR, Output Com/Input Com5			
dc	160dB min	•	•
60Hz	120dB min	:	•
Leak Cur., Input/output 115 Virms, 80Hz	1µA rms max		
IsoLATION IMPEDANCE*	10 <sup>12</sup> 0116-F	•	
	10 32#10pF		
Initial @ +25°C (Adjustable to Zero)	±10mV max	•	•
vs. Temperature	±100µV/°C max	±50µV/°C max	$\pm 100 \mu V/^{\circ} C max$
vs. Supply Voltage	±1mV/V	•	•
vs. Time	±100µV/mo	•	•
FREQUENCY RESPONSE			
Small Signal, -30B Full Power, 20V p.n Output	2.5kHz	•	•
Settling Time ±10V Step to 0.1%	lms	•	•
RATEDOUTPUT			
Voltage/Current	±10V min @ ±5mA min	•	•
OUTPUT NOISE			
Voltage, 0.01Hz to 10Hz	7μV p-p	•	•
10Hz to 1kHz	25µV rms	•	•
POWER SUPPLY <sup>6</sup>		. –	
Voltage, Rated Performance	±15V dc		••••
Current Quiescent	$\pm (14 \text{ to } 16) \text{ V dc}$		:
TEMPERATURE RANCE	· 55, -510A	· · · · · · · · · · · · · · · · · · ·	
Rated Performance	0 to +70°C	•	-25°C to +85°C
Operating	-25°C to +85°C	•	•
Storage	-55°C to +85°C	•	•
CASE SIZE	3.0" x 2.2" x 0.59"	•	•

### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm)



MATING SOCKET - AC1053



Figure 3. Input Stage Gain, CMR and Phase vs. Frequency



Figure 4. Output Stage Gain and Phase vs. Frequency

<sup>1</sup>Current drawn from INPUT FEEDBACK terminal must be <5mA. <sup>1</sup>Total current drawn from IN FEEDBACK and either +V<sub>ISO</sub> or +V<sub>ISO</sub> must be <15mA. <sup>1</sup>Input common mode specifications are measured at +IN and -IN terminals with respect to INPUT COM. <sup>1</sup>Protected for momentary shorts to IN COM.

Isolation specifications are measured at INPUT COM with respect to OUT COM and PWR COM. Recommended power supply, ADI model 904, ±15V @ ±50mA.

\*Specifications same as model 277J.

Specifications subject to change without potice.

# 

## High CMV, High Performance Isolation Amplifiers

### FEATURES

High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous

High CMR: 110dB min with  $5k\Omega$  Imbalance Low Nonlinearity: 0.05% @ 10V pk-pk Output High Gain Stability:  $\pm 0.0075\%^{\circ}$ C,  $\pm 0.001\%/1000$  hours Low Input Offset Voltage Drift:  $10\mu V/^{\circ}$ C, G = 100V/V(Model 286J)

Resistor Programmed Gain: 1 to 10V/V (284J) 1 to 100V/V (286J)

Isolated Power Supply: ±8.5V dc @ ±5mA (284J) ±15V dc @ ±15mA (286J)

Meets IEEE Std 472: Transient Protection (SWC) Meets UL Std 544 Leakage @ 115V ac, 60Hz:

2.0µA max (284J)

2.5µA max (286J)

### APPLICATIONS

Fetal Heartbeat Monitoring

Multi-Channel ECG Recording

Ground Loop Elimination in Industrial and Process Control High Voltage Protection in Data Acquisition Systems 4-20mA Isolated Current Loop Receiver

### GENERAL DESCRIPTION

The models 284J, 286J are low cost, high performance isolation amplifiers designed for high CMV isolation and low leakage in biomedical, industrial and data acquisition systems. Using modulation techniques with reliable transformer isolation, the models 284J, 286J protect both patients and ultrasensitive equipment from high CMV transients up to  $\pm 5000V$ pk (10ms pulse) or 2500V dc continuous, high CMR of 110dB (5k $\Omega$  imbalance) and feature maximum leakage current of less than  $3\mu$ A rms, @ 115V ac, 60Hz (inputs to power common).

The model 284J is a self-contained isolation amplifier for single channel applications. For multi-channel applications, the model 286J combined with an external synchronizing oscillator such as the model 281 may be used; up to 16 model 286J amplifiers can be driven from 1 model 281 oscillator. Additional channels may be obtained by configuring an unlimited number of 284Js with several ganged 281 oscillators.

Both models also provide resistor-programmable gain of 1 to 10V/V (284J) or 1 to 100V/V (286J), high gain stability of  $0.0075\%^{\circ}$ C, low nonlinearity of 0.05% @ 10V pk-pk output and isolated power supply outputs of ±15V dc @ ±15mA (286J) or ±8.5V dc @ ±5mA (284J).

### WHERE TO USE MODELS 284J, 286J

Industrial Applications: In data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, models 284J, 286J offer complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded

## MODELS 284J, 286J, 281



with model 286J's 20V pk-pk or model 284J's 10V pk-pk input signal range at a gain of 1V/V operation. In portable field designs, single supply, wide range operation (+8V to +16V) offers simple battery operation.

Medical Applications: In biomedical and patient monitoring equipment such as multi-channel VCG, ECG, and polygraph recorders, models 284J, 286J offer protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with low input noise ( $8\mu$ V pk-pk @ G = max gain) and high CMR (110dB, min @ 60Hz).

### DESIGN FEATURES AND USER BENEFITS

High Reliability: Models 284J, 286J are conservatively designed, compact modules, capable of reliable operation in harsh environments. Models 284J, 286J have calculated MTBF of over 390,000 hours and are designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 284J and 286J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

Isolated Power Supply: Dual regulated supplies, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers as well as remote transducers such as thermistors or bridges.

Adjustable Gain: A single external resistor enables gain adjustment from 1V/V to 100V/V (286J) or 1V/V to 10V/V (284J) providing the flexibility of applying models 284J, 286J in both high-level transducer interfacing as well as low-level sensor measurements.

# **SPECIFICATIONS**

MODEL	284J	286J <sup>1</sup>
GAIN (NON-INVERTING)		
Range (50k Load)	1 to 10V/V 100kΩ	1 to 100V/V 100kΩ
Formula	$Gain = [1 + \frac{10.7kO + P.(kO)}{10.7kO + P.(kO)}]$	Gain = $\left[1 + \frac{1k\Omega + R_{c}(k\Omega)}{1k\Omega + R_{c}(k\Omega)}\right]$
Deviation from Formula	±3%	±4%
vs. Time	±0.001%/1000 Hours	*
vs. Temperature (0 to $+70^{\circ}$ C) <sup>2</sup>	±0.0075%/°C	•
Nonlinearity, 10V pk-pk Output <sup>2</sup>	±0.05%	•
INPUT VOLTACE PATINCS	· · · · · · · · · · · · · · · · · · ·	
Liness Differential Range C = 1V/V	+SV min	+10V min
Max Sofe Differential Input	_5 ¥ mm	100 1111
Continueut	2401	•
Pulse 10ms duration 1 pulse/10 sec	+6500V . max	•
Pulse, Toms duration, 1 pulse/10 sec	10500vpk max	
Max CMV, inputs to Outputs	25001/	•
Pulse 10ms duration 1 pulse/10 sec	+2500V max	•
With 510kQ in ceries with Guard	+5000V   max	.•
Continuour AC or DC	+2500V _ max	•
CMR inputs to Outputs 60Hz $R_0 \leq 5k\Omega$	-2500 V pk max	
Balanced Source Impedance	114dB	•
5kQ Source Impedance Impalance	110dB min	•
CMR. Inputs to Guard 60Hz		
$1k\Omega$ Source Impedance Impalance	78dB	•
Max Leakage Current, Inputs to Power Comm	on	
@ 115VAC. 60Hz	2.0µA rms max	2.5µA rms max
INPUT IMPEDANCE		
Differential	10-32#/0pF	10-32(150pF
Overload	500K32	
Common Mode	5x10* 52120pF	
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	±7nA max	•
vs. Temperature (0 to +70°C)	±0.1nA/°C	•
INPUT NOISE		
Voltage <sup>3</sup>		
0.05Hz to 100Hz	8µV pk-pk	•
10Hz to 1kHz	10µV rms	3μV rms
Current	•	·
0.05Hz to 100Hz	5pA pk-pk	•
EBEQUENCY RESPONSE		
Small Signal 3dB	1kHz	•
Slew Rate	25mV/us	•
Full Power 10V n-p Output	200Hz	900Hz
Full Power 20V p-p Output	N/A	400Hz
Recovery Time, to ±100µV after Application		
of ±6500V_1. Differential Input Pulse	200ms	•
OFFSET VOLTAGE REFERRED TO INPUT		HII HII
Terre are the second second second	I(3 + 20/G)mV	1(3 + 45/G)mV
vs. remperature (0 to +/0 C)	$\pm (1 + 150/G)\mu V/C$	±(/ + 250/G)μV/°C
vs. Supply voltage	11mv/%	R
RATED OUTPUT		LO IN/
Voltage, 50kΩ Load	±5V min	±10V min com
Output Impedance	1kΩ	•
Output Ripple, 1MHz Bandwidth	5mV pk-pk	20mV pk-pk
ISOLATED POWER OUTPUTS		
Voltage, ±5mA Load	±8.5V dc	±15V dc
Accuracy	±5%	0, -6%
Current	±5mA min	±15mA min
Regulation, No Load to Full Load	+0, -15%	+0, -10%
Ripple, 100kHz Bandwidth	100mV pk-pk	200mV pk-pk
POWER SUPPLY, SINGLE POLARITY	····	
Voltage Rated Performance	+15V do	•
Voltage Operating	+13 + 40 +(8 to 15 \$)V de	• н
Current. Ouiescent	+10mA	+13mA
TEMPERATURE RANGE		
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	LO IN/
Operating	-25 °C to +85 °C	- COM
Storage	-55 °C to +85 °C	
CASE DIMENSIONS <sup>5</sup>	1.5" x 1.5" x 0.62"	•

### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



GAIN = 1 + 100kΩ 10.7kΩ + Ri(kΩ) (1V/V TO 10V/V)

Figure 1. Block Diagram – Model 284J



Figure 2. Block Diagram - Model 286J

NOTES

\*Specifications same as model 284J.

<sup>3</sup> Specifications for model 286J apply when driven by ADI model 281 oscillator.
<sup>3</sup> Gain temperature drift and gain nonlinearity are specified as a percentage of

<sup>a</sup> Model 284J; Gain = 10V/V; Model 286J; Gain = 100V/V.
 <sup>a</sup> Model 284J; Gain = 10V/V; Model 286J; Gain = 100V/V.
 <sup>a</sup> Recommended power supply, ADI model 904, ±15V @ 50mA.
 <sup>a</sup> Recommended mounting sockets – model 284J; ADI Part Number AC1049; model 286J; ADI Part Number AC1054.

Specifications subject to change without notice.

## **Understanding the Isolation Amplifier Performance**

### INTERCONNECTION AND GUARDING TECHNIQUES

Models 284J, 286J can be applied directly to achieve rated performance as shown in Figures 3 and 4. To preserve the high



NOTE 4. R2 ~ 200Ω, G = 1; R2 ~ 2kΩ, G>1





Figure 4. Model 286J Basic Isolator Interconnection



### Figure 5. Model 286J Optional Connection: Offset Voltage Trim Adjust, Bandwidth (-3dB) Rolloff and Gain Adjust (G>100V/V)

CMR performance, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 284J or 286J. The GUARD (Pin 6) should be connected to this shield. The guard-shield is provided with the mounting socket. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low. Offset Voltage Trim Adjust: The trim adjust circuits shown in Figures 3 and 5 can be used to zero the output offset voltage over the specified gain range. The output terminals, HI OUT and LO OUT, can be floated with respect to PWR COM up to  $\pm 50V_{pk}$  max, offering three-port isolation. A  $0.1\mu$ F capacitor is required from LO OUT to PWR COM whenever the output terminals are floated with respect to PWR COM. LO OUT can be connected directly to PWR COM when output offset trimming is not required.

### INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kM\Omega. Figures 6 and 8 illustrate the CMR ratings at 60Hz and 5k $\Omega$  source imbalance between signal input/output terminals, along with their respective capacitance.





COL WHEN GUARD TIED TO INPUT COMMON MODE SOURCE

Figure 6. Model 284J Terminal Capacitance and CMR Ratings

Figure 7. Model 284J Terminal Ratings





Figure 8. Model 286J Terminàl Capacitance and CMR Ratings

Figure 9. Model 286J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figures 7 and 9 and Table I illustrate models 284J, 286J ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V <sub>PK</sub> (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	±240V <sub>RMS</sub>	Withstand Voltage, Steady State
V2 (pulse)	$\pm 2500 V_{PK}$ (10ms) R <sub>G</sub> = 0	Transient
V2 (pulse)	$\pm 5000 V_{PK}$ (10ms) R <sub>G</sub> = 510k $\Omega$	Isolation, Defibrillator
V2 (cont.)	±2500VPK	Isolation, Steady State
V3 (cont.)	±50VPK	Isolation, dc
Z1	50kMΩ  20pF	Isolation Impedance
I (286J)	50µA rms	Input Fault Limit, de to 200kHz
I (284J	35µA rms	Input Fault Limit, de to 60kHz

Table I. Isolation Ratings Between Terminals

s

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.0 $\mu$ A rms (284J) and 2.5 $\mu$ A rms (286J) at 115V ac, 60Hz (or 0.02 $\mu$ A/V ac). As shown in Figures 10 and 11, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current. Line frequency leakage current levels are unaffected by the power on or off condition of models 284J, 286J.

For medical applications, models 284Jand 286J are designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies (e.g., model 286J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference Leakage Current, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, models 284J, 286J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.



Figure 10. Model 284J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions



Figure 11. Model 286J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

### GAIN AND OFFSET TRIM PROCEDURE, MODEL 284J

- 1. Apply  $e_{IN} = 0$  volts and adjust  $R_0$  for  $e_0 = 0$  volts.
- 2. Apply  $e_{IN} = +1.000V \text{ dc}$  and adjust  $R_G$  for  $e_O = +5.000V \text{ dc}$ .
- 3. Apply  $e_{IN} = -1.000V$  dc and measure the output error (see
- curve a). 4. Adjust R<sub>G</sub> until the output error is one half that measured in step 3 (see curve b).
- 5. Apply  $e_{IN}$  = +1.000V dc and adjust  $R_0$  until the output error is one half that measured in step 4 (see curve c).



Figure 12. Gain and Offset Adjustment

GAIN AND OFFSET TRIM PROCEDURE, MODEL 286J In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/Vis desired.

- 1. Apply  $e_{IN} = 0$  volts and adjust  $R_0$  for  $e_0 = 0$  volts.
- 2. Apply  $e_{IN} = +0.500 \text{ V} \text{ dc}$  and adjust  $R_G$  for  $e_O = +5.000 \text{ V} \text{ dc}$ .
- 3. Apply  $e_{IN} = -0.500V$  dc and measure the output error (see curve a).
- 4. Adjust  $R_G$  until the output error is one half that measured in step 3 (see curve b).
- 5. Apply +0.500V dc and adjust R<sub>O</sub> until the output error is one half that measured in step 4 (see curve c).



Figure 13. Gain and Offset Adjustment

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Figure 14. Model 284J Common Mode Rejection vs. Frequency



Figure 15. Model 286J Common Mode Rejection vs. Frequency



Figure 16. Model 284J Common Mode Rejection vs. Source Impedance Imbalance



Figure 17. Model 286J Common Mode Rejection vs. Source Impedance Imbalance



Figure 18. Model 284J Input Voltage Noise vs. Bandwidth



Figure 19. Model 286J Input Voltage Noise vs. Bandwidth



Figure 20. Model 284J Input Offset Voltage Drift vs. Gain



Figure 21. Model 286J Input Offset Voltage Drift vs. Gain

## Applying the Multi-Channel Isolation Amplifier



Figure 22. Model 286J Gain Nonlinearity vs. Output Voltage

### **REFERENCE EXCITATION OSCILLATOR\***

When applying model 286J, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 23, or purchasing a module from Analog Devices - model 281.



FREQ. ADJUST: ADJUST TRIM POT FOR OUTPUT FREQUENCY OF 100kHz ±5%. FOR SLAVE OPERATION, REMOVE JUMPER FROM SYNC OUT AND SYNC IN PINS. USE CERAMIC CAPACITOR, "COG" OR "NPO" CHARACTERISTIC.

### Figure 23. Model 281 100kHz Oscillator - Logic and Interconnection Diagram

The block diagram of model 281 is shown in Figure 24. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.



Figure 24. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 286 Is as shown in Figure 25. An additional model 281 may be driven in a slave-mode, as shown in Figure 26 to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

### **\*CAUTION:**

ESD(Electro-static-discharge) sensitive device. Permanent damage may occur on unconnected devices subjected to high-energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

### **EXTERNAL OSCILLATOR INTERCONNECTION**



Figure 25. Model 281/286 Connection for Driving from 1 to 16 Isolators



Figure 26. Model 281/286 Connection for Driving > 16 Isolators

### SPECIFICATIONS

(typical @ +25°C and Vs = +15V dc unless otherwise noted)

MODEL	281•
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage ( $\phi$ and $\overline{\phi}$ terminals)	0 to +12V pk
Fan-Out <sup>1,2</sup>	16 max
POWER SUPPLY RANGE <sup>3</sup>	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
MECHANICAL	
Case Size	1.4" x 0.6" x 0.49"
Weight	10 grams
NOTES	

<sup>1</sup>Model 286J oscillator drive input represents unity oscillator load.

<sup>2</sup> For applications requiring more than 16 286Js, additional 281s may be used in a master/slave mode. Refer to Figure 26. <sup>3</sup> Full load consists of 16 model 286 js and 281 oscillator slave.

Specifications subject to change without notice.



### **OUTLINE DIMENSIONS**

PIN TERMINAL IDENTIFICATION

MATING SOCKET: Cinch #16 DIP or Equivalent



### VOL. II, 5-16 ISOLATION AMPLIFIERS

# 

## Precision, Wide Bandwidth, Synchronized Isolation Amplifier

**MODEL 289** 

### FEATURES

Low Nonlinearity: ±0.012% max (289L) Frequency Response: (-3dB) dc to 20kHz (Full Power) dc to 5kHz Gain Adjustable 1 to 100V/V, Single Resistor 3-Port Isolation: ±2500V CMV Isolation Input/Output Low Gain Drift: ±0.005%/°C max Floating Power Output: ±15V @ ±5mA 120dB CMR at 60Hz: Fully Shielded Input Stage Meets UL Std. 544 Leakage: 2µA rms max, @ 115V ac, 60Hz

### APPLICATIONS

Multi-Channel Data Acquisition Systems Current Shunt Measurements Process Signal Isolator High Voltage Instrumentation Amplifier SCR Motor Control

### **GENERAL DESCRIPTION**

Model 289 is a wideband, accurate, low cost isolation amplifier designed for instrumentation and industrial applications. Three accuracy selections are available offering guaranteed gain nonlinearity error at 10V p-p output: ±0.012% max (289L), ±0.025% max (289K), ±0.05% max (289J). All versions of the 289 provide a small signal frequency response from dc to 20kHz (-3dB) and a large signal response from dc to 5kHz (full power) at a gain of 1V/V. This new design offers true 3-port isolation, ±2500V dc between inputs and outputs (or power inputs), as well as 240V rms between power supply inputs and signal outputs. Using carrier modulation techniques with transformer isolation, model 289 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. It provides 120dB Common Mode Rejection between input and output common. The high CMV and CMR ratings of the model 289 facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays.

### WHERE TO USE THE MODEL 289

The model 289 is designed to interface single and multichannel data acquisition systems with dc sensors such as thermocouples, strain gauges and other low level signals in harsh industrial environments. Providing high accuracy with complete galvanic isolation, and protection from line transients of fault voltages, model 289's performance is suitable for applications such as process controllers, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.

Use the model 289 when data must be acquired from floating transducers in computerized process control systems. The photograph above shows a typical multichannel application allowing potential differences or interrupting ground loops, among transducers, or between transducers and local ground.



## DESIGN FEATURES AND USER BENEFITS

**Isolated Power:** The floating power supply section provides isolated  $\pm 15V$  outputs ( $\oplus \pm 5mA$ ). Isolated power is regulated to within  $\pm 5\%$ ). This feature permits model 289 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers such as thermistors or bridges, eliminating the need for a separate isolated dc/dc converter.

Adjustable Gain: A single external resistor adjusts the model 289's gain from 1V/V to 100V/V for applications in high and low level transducer interfacing.

Synchronized: The model 289 provides a synchronization terminal for use in multichannel applications. Connecting the synchronization terminals of model 289s synchronizes their internal oscillators, thereby eliminating the problem of oscillator "beat frequency" interference that sometimes occurs when isolation amplifiers are closely mounted.

Internal Voltage Regulator: Improves power supply rejection and helps prevent carrier oscillator spikes from being broadcast via the isolator power terminal to the rest of the system.

**Buffered Output:** Prevents gain errors when an isolation amplifier is followed by a resistive load of low impedance. Model 289 can drive a  $2k\Omega$  load.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates need for power supply and output ports being returned through a common terminal.

Reliability: Model 289 is conservatively designed to be capable of reliable operation in harsh environments. Model 289 has a calculated MTBF of 271,835 hours. In addition, the model 289 meets UL Std. 544 leakage, 2µA rms @ 115V ac, 60Hz.

## **SPECIFICATIONS** (typical @ $+25^{\circ}$ C and V<sub>S</sub> = +14.4V to +25V dc unless otherwise noted)

Model	289J	289K	289L
GAIN (NONINVERTING)			
Range		1 to 100V/V	
Formula		$G = 1 + \frac{10k\Omega}{R_{p}(k\Omega)}$	
Deviation from Formula		±1.5% max	
vs. Temperature (0 to +70°C) <sup>1</sup>		15ppm/°C typ (50ppm	/°C max)
Nonlinearity, (±5V Swing) <sup>2,3</sup>	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS	·		
Linear Differential Range (G = 1V/V)		±10V min	
Continuous		120V rms	
1 Minute		240V rms	
Max CMV (Inputs to Outputs)		+2500V neek max	
ac. 60Hz, 1 Minute Duration		2500V rms	
CMR, Inputs to Outputs 60Hz			
$R_S \le 1k\Omega$ , Balanced Source Impedance		120dB	
R <sub>S</sub> ≤ 1kM, HI IN Lead Only Max Leakage Current, Input to Output @ '		104dB min	
115V rms, 60Hz ac		2µA rms max	
INPUT IMPEDANCE			
Differential		33pF  10 <sup>8</sup> Ω	
Overload		$100k\Omega$	
		20pF    5 × 10 - 32	
Initial @ +25°C		10nA (75nA max)	
vs. Temperature (0 to 70°C)		0.15nA/°C	
INPUT NOISE (GAIN = 100V/V)			
Voltage			
0.05Hz to 100Hz		8µV p-p	
TOHZ TO TRHZ		sμv rms	
0.05Hz to 100Hz		3pA rms	
FREQUENCY RESPONSE		- <u></u> -	
Small Signal –3dB			
G = 1V/V		20kHz	
G = 100 V/V Full Power, 10V p-p Output		SKHZ	
G = 1V/V		5kHz	
G = 100V/V		3.5kHz	
Full Power, 20V p-p Output		2 2442	
G = 100V/V		2.3kHz	
Slew Rate		0.14V/µs	
Settling Time <sup>4</sup> ±0.05%, ±10V Step		400µs	
OFFSET VOLTAGE, REFERRED TO INPUT		10	
Initial, @ +25 C		$\frac{15}{G}$ mv max	
vs. Temperature (0 to +70°C)	$\pm 20 \pm \frac{200}{C}$ max	$\pm 15 \pm \frac{100}{2}$ max	$\pm 10 \pm \frac{50}{C} \mu V/^{\circ} C max$
-	G	10	G
vs. Supply Voltage (+15V to +20V change)		$\pm 2 \pm \frac{10}{G} \mu V/V$	
RATED OUTPUT			
Voltage, 2kΩ Load		±10V min	*
Output Ripple, 0.1MHz Bandwidth		<132(de to 100H2)	
No Signal IN		5mV p-p	
+10V <sub>IN</sub>		50mV p-p	
ISOLATED POWER SUPPLY	•		
Accuracy		±15V dc ±10%	
Current	1.1.1	±5mA, min	
Regulation No Load to Full Load		±5%	
Ripple, 0.1MHz Bandwidth, No Load		25mV p-p	
Full Load		75mV p-p	
Voltage, Bated Performance		+14 4V to +25V	
Voltage, Operating		+8.5V to +25V	
Current, Quiescent (@ V <sub>S</sub> = +15V)		+25mA	
TEMPERATURE RANGE			· · ·
Rated Performance		0 to +70°C	
Operating Storage		-15 C to +75 C -55°C to +85°C	
		15" ¥ 20" ¥ 0.75"	
NOTES		1.3 ~ 2.0 ~ 0.73	·
NOTES			



Dimensions shown in inches and (mm).



### SHIELDED MATING SOCKET AC1214



### INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of model 289, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 289 as illustrated in the outline drawing above (screened area). The LO IN/ISO PWR COM (pin 1) must be connected to this shield. This shield is provided with the mounting socket, model AC1214 (solder feedthrough wire to the socket pin 1 and copper foil surface). A recommended shielding technique using model AC1214 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable for the input signal to reduce inductive and capacitive pickup. To further reduce effective cable capacitance, the cable shield should be connected to the common mode signal source as close to signal low as possible (see Figure 1).

<sup>2</sup>Gain nonlinearity is specified as a percentage of 10V pk-pk output signal level.

<sup>3</sup>When isolated power output is used, nonlinearity increases by ±0.002%/mA of current drawn <sup>4</sup>G = 1V/V; with 2-pole, 5kHz output filter.

<sup>5</sup> Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

## **Understanding the Isolation Amplifier Performance**



NOTE: GAIN RESISTOR R.G. 1% SOOPM/C METAL FILM TYPE IS RECOMMENDED. FOR GAIN + TV/V, LEAVE PIN 4 OPEN FOR GAIN + TV/V, CONNECT GAIN RESISTOR (R\_G) BETWEEN PIN 4 AND PIN 1 GAIN = 1 +  $\frac{10k\Omega}{r_{\rm eff}}$ 



### **THEORY OF OPERATION**

The remarkable performance of the model 289 is derived from the carrier isolation technique used to transfer both signal and power between the amplifier's input stage and the rest of the circuitry. A block diagram is shown in Figure 2.





The input signal is filtered and appears at the input of the noninverting amplifier, A1. This signal is amplified by A1, with its gain determined by the value of resistance connected externally between the gain terminal and the input common terminal. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulated voltage is filtered, amplified and buffered by amplifier A2, and applied to the output terminal. The voltage applied to the V<sub>S</sub> terminal is set by the regulator to +12Vwhich powers the 100kHz symmetrical square wave power oscillator. The oscillator drives the primary winding of transformer T2. The secondary windings of T2 energize both input and output power supplies, and drives both the modulator and demodulator.

## INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

**Capacitance:** Interelectrode terminal capacitance, arising from stray coupling capacitance effects between the input terminals and the signal output terminals, are each shunted by leakage resistance values exceeding  $50G\Omega$ . Figure 3 illustrates model 289's capacitance, between terminals.



Terminal Ratings: CMV performance is given in both peak pulse and continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 illustrates model 289 ratings between terminals.

### GAIN AND OFFSET TRIM PROCEDURE

The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and Gain = 10V/V.

- 1. Apply  $E_{IN} = 0$  volts and adjust  $R_0$  for  $E_0 = 0$  volts.
- 2. Apply  $E_{IN}$  = +0.500V dc and adjust  $R_G$  for  $E_O$  = +5.000V dc.
- 3. Apply  $E_{IN} = -0.500V$  dc and measure the output error (see curve a).
- 4. Adjust  $R_G$  until the output error is one-half that measured in step 3 (see curve b).
- 5. Apply +0.500V dc and adjust  $R_0$  until the output error is one-half that measured in step 4 (see curve c).





Figure 5a. Recommended Offset and Gain Adjustment for Gains > 1



Figure 5b. Recommended Offset Adjustment for G = 1V/V

### PERFORMANCE CHARACTERISTICS



Figure 6. Typical 289 Phase vs. Frequency



Figure 7. Typical 289 Common Mode Rejection vs. Source Impedance



Figure 8. Typical Input Voltage Noise vs. Bandwidth



Figure 9. Typical Gain Nonlinearity vs. Output Swing



Figure 10. Typical Gain Nonlinearity vs. Gain



Figure 11. Typical Common Mode Rejection vs. Frequency at a Gain of 1V/V, CMR is typically 6dB Lower than at a Gain of 100V/V

### MULTICHANNEL APPLICATIONS

Isolation amplifiers containing internal oscillators may exhibit a slowly varying offset voltage at the output when used in multichannel applications. This offset voltage is the result of adjacent internal oscillators beating together. For example, if two adjacent isolation amplifiers have oscillator frequencies of 100.0kHz and 100.1kHz respectively, a portion of the difference frequency may appear as a slowly varying output offset voltage error. Model 289 eliminates this problem by offering a synchronization terminal (pin 8). When this terminal is interconnected with other model 289 synchronization terminals, the units are synchronized. Alternately, one or more units may be synchronized to an external 100kHz ±2% squarewave generator by the connection of synchronization termial(s) to that generator. The generator output should be 2.5V-5.0V p-p with  $1k\Omega$  source impedance to each unit. Use an external oscillator when you need to sync to an external 100kHz source, such as a sub-multiple of a microprocessor clock. A differential line driver, such as SN75158, can be used to drive large clusters of model 289. When using the synchronization pin, keep leads as short as possible and do not use shielded wire. These precautions are necessary to avoid capacitance from the synchronization terminal to other points. It should be noted that units synchronized must share the same power common to ensure a return path.

# 

## Low Cost, Single and Multichannel Isolation Amplifier

## **MODELS 290A, 292A**

### FEATURES

### Low Cost

Multichannel Capability Using External Oscillator (292A) Isolated Power Supply: ±13V dc @ ±5mA (290A) or ±15mA (292A)

Low Nonlinearity: 0.1% @ 10V pk-pk Output High Gain Stability: 0.001%/1000 Hours; 0.01%/°C Small Size:  $1.5'' \times 1.5'' \times 0.62''$ Low Input Offset Voltage Drift:  $10\mu V/°C$  (Gain = 100V/V) Wide Input/Output Dynamic Range: 20V pk-pk High CMV Isolation: 1500V dc, Continuous Wide Gain Range: 1 to 100V/V

### APPLICATIONS

Ground Loop Elimination in Industrial and Process Control High Voltage Protection in Data Acquisition Systems Off-Ground Signal Measurements

### GENERAL DESCRIPTION

Models 290A and 292A are low cost, compact, isolation amplifiers that are optimized for single and multichannel industrial applications, respectively. The model 290A has a self-contained oscillator and is intended for single channel applications. A single external synchronizing oscillator can drive up to 16 model 292As or, a virtually limitless number of model 292As can be configured using multiple oscillators. The user can supply the external oscillator circuit or specify model 281 oscillator module, which includes a voltage regulator for operation over a wide single supply voltage range of +8V to +28V.

Models 290A and 292A design features include: adjustable gain, from 1 to 100V/V, dual isolated power,  $\pm 13V$  dc,  $\pm 1500V$  dc off ground isolation, 100dB minimum CMR at 60Hz, 1k $\Omega$ source imbalance, in a compact  $1.5'' \times 1.5'' \times 0.6''$  module. Models 290A and 292A achieve low input noise of 1 $\mu$ V pk-pk (10Hz bandwidth, G = 100V/V), nonlinearity of  $\pm 0.1\%$  @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, models 290A and 292A will interrupt ground loops, leakage paths, and voltage transients, while providing dc to 2kHz (-3dB) response.

### WHERE TO USE MODELS 290A AND 292A

Industrial Applications: In data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, models 290A and 292A offer complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded



with 20V pk-pk input signal range at a gain of 1V/V operation. In portable single or multichannel designs, single power supply operation (+8V to +16V) enables battery operation.

### DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual  $\pm 13V$  dc output, completely isolated from the input power terminals ( $\pm 1500V$  dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Models 290A and 292A adjustable gain offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 100V/V providing flexibility in both high level transducer interfacing as well as low level sensor measurement applications.

Floating, Guarded Front-End: The input stage of models 290A and 292A can directly accept floating differential signals or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Models 290A and 292A are conservatively designed, compact modules, capable of reliable operation in harsh environments. They have a calculated MTBF of over 400,000 hours and are designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

# **SPECIFICATIONS** (typical @ +25°C; G = 100V/V and VS = +15V dc, unless otherwise noted)

MODEL	290A		292A
GAIN (NONINVERTING)			
Range (50kΩ Load)		1 to 100V/V 🔍	
Formula		$Gain = \begin{bmatrix} 1 + \frac{1}{1k\Omega} \end{bmatrix}$	$\frac{00k\Omega}{R_{1}(k\Omega)}$
Deviation from Formula		±3%	
vs. Time		±0.001%/1000 Ho	urs
vs. Temperature (-25°C to +85°C) <sup>1</sup>		±0.0075%/°C	
Nonlinearity, G = 1V/V to 100V/V <sup>2</sup>		±0.1% (±0.25%) <sup>3</sup>	
INPUT VOLTAGE RATINGS			
Linear Differential Range, G = 1V/V		±5V min (±10V m	in) <sup>3</sup>
Max Safe Differential Input			
Continuous, 1 min		110v ms	
ac 60Hz 1 Minute Duration		1500V rms max	
Continuous, ac		±1000V pk max	
Continuous, dc		±1500V pk max	
CMR, Inputs to Outputs, 60Hz, $R_S \leq 1k\Omega$			
Balanced Source Impedance		106dB	
1k12 Hi In Lead Only		100dB min	
@ 115V ac 60Hz	non	100 A rms max	
		TOUR THIS HEAR	
Differential		10 <sup>8</sup> Oll705 F	
Overload		10 M/ 100kΩ	
Common Mode		5 X 10 <sup>10</sup> Ω  100pl	7
INDUT DIFFERENCE CURPENT			
Initial @ +25°C		+3nA	
vs. Temperature (-25°C to +85°C)		±0,1nA/°C	
Voltage G = 100V/V			
0.01Hz to 10Hz		1μV p-p	
10Hz to 1kHz		1.5µV rms	
Current			
0.05Hz to 100Hz		5pA p-p	
FREQUENCY RESPONSE			
Small Signal, -3dB, G = 1V/V		2.5kHz	
Slew Rate		50mV/µs	
Full Power, 10V p-p Output	2 01-11 (1 01-11-)3		3 01-11 (1 01-11.)3
	2.0KHZ(1.0KHZ)		S.OKHZ(1.OKHZ)
OFFSET VOLTAGE REFERRED TO INPUT		+(5 + 50/C)mV	
$r_{1}$ $r_{2}$ $r_{2$	+(10+150/G)//V	1(3 + 30/G)IIIV	+(8+250/G)//V/°C
vs. Supply Voltage	=(10 / 190/0/µ/	±1mV/%	-(0 * 250/0/µ1/ 0
PATED OUTPUT			
Voltage 50k Load		±5V min (±10V n	nin) <sup>3</sup>
Output Impedance		1kΩ	,
Output Ripple, 1MHz Bandwidth		10mV pk-pk	
OSCILLATOR DRIVE INDUT			
Input Voltage	N/A		8 to 16V pk-pk
Input Frequency	N/A		100kHz ±5%, max
ISOLATED POWER OUTPUTS			
Voltage Full Load		±13V dc	
Accuracy		±5%	
Current <sup>4</sup>	±5mA min		±15mA min
Regulation, No Load to Full Load		+0, -15%	
Ripple, 100kHz Bandwidth	200mV p-p		250mV p-p
POWER SUPPLY, SINGLE POLARITY			
Voltage, Rated Performance	1.1	+15V dc	
Voltage, Operating	•	+8V dc to +15.5V	/ dc
Current, Quiescent		+20mA	
TEMPERATURE RANGE	•		N
Rated Performance		-25°C to +85°C	
Storage		->5 °C to +85 °C	*
CASE DIMENSIONS		1.5" × 1.5" × 0.63	2″ .
NOTES			
Gain temperature drift is specified as a percentage of Gain poplinearity is specified as a percentage of 10V	output signal level.		
<sup>3</sup> These specs apply for a 20V pk-pk output span.	L. bu outher shall		
<sup>4</sup> Do not load VISO when operating at output spans gr	eater than 10V pk-p	k.	

### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



GAIN = 1 + 100kΩ 1kΩ + R<sub>1</sub> (kΩ) (1V/V TO 100V/V)

PON





### Figure 2. Model 290A and 292A Terminal Ratings

Symbol	Rating	Remarks
$\begin{matrix} V_1 \\ V_2 \\ V_2 \\ V_2 \\ V_3 \\ Z_1 \end{matrix}$	±110V rms (cont.) ±1000V pk (cont.) ±1500V pk (cont.) ±1500V rms (1 min) ±50V pk (cont.) 50GΩ  20pF	Withstand Voltage, Steady State Isolation, Steady State, ac Isolation, Steady State, de Isolation, ac, 60Hz Isolation, dc Isolation Impedance

Table I. Isolation Ratings Between Terminals

### CAUTION:

Specifications subject to change without notice.

ESD(Electro-static-discharge) sensitive device. Permanent damage may occur on unconnected devices subjected to high-energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



## **Understanding the Isolation Amplifier Performance**



Figure 3. Transducer - Amplifier Interface

### GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/Vis desired.

- 1. Apply  $E_{IN} = 0$  volts and adjust  $R_0$  for  $E_0 = 0$  volts.
- 2. Apply  $E_{IN}$  = +0.5V dc and adjust  $R_G$  for  $E_O$  = +5.0V dc.
- 3. Apply  $E_{IN} = -0.5V$  dc and measure the output error (see curve a).
- 4. Adjust  $R_G$  until the output error is one half that measured in step 3 (see curve b).
- 5. Apply +0.5V dc and adjust R<sub>O</sub> until the output error is one half that measured in step 4 (see curve c).





### Figure 4. Gain and Offset Adjustment



Figure 5. Selecting Bandwidth with a 3-Pole 5Hz Active Filter for Improved 60Hz Noise Reduction (typ 150dB @ 60Hz and 1k $\Omega$  Imbalance)

### PERFORMANCE CHARACTERISTICS



Figure 6. Typical Common Mode Rejection vs. Frequency



Figure 7. Typical Common Mode Rejection vs. Source Impedance Imbalance



Figure 8. Typical Gain Nonlinearity vs. Output Voltage



Figure 9. Typical Input Voltage Noise vs. Bandwidth Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 10 illustrates total input drift over the gain range of 1 to 100V/V.



Figure 10. Typical Input Offset Voltage Drift vs. Gain

**REFERENCE EXCITATION OSCILLATOR, MODEL 281** When applying model 292A, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 11, or purchasing a module from Analog Devices-model 281.







The block diagram of model 281 is shown in Figure 12. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.



Figure 12. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 292As. As shown in Figure 13, an additional model 281 may be driven in a slave-mode to expand the total system channels from 16 to 32. By adding additional model 281s in this manner, systems of over 1000 channels may be easily configured.



### Figure 13. External Oscillator Interconnection **SPECIFICATIONS**

(typical @  $+25^{\circ}$  C and Vs = +15 V dc unless otherwise noted)

MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage ( $\phi$ and $\overline{\phi}$ terminals)	0 to +12V pk
Fan-Out <sup>1,2</sup>	16 max
POWER SUPPLY RANGE <sup>3</sup>	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
, F.L.	+33mA
TEMPERATURE	· · ·
Rated Performance	$0 \text{ to } +70^{\circ} \text{C}$
Storage	-55°C to +85°C

Model 292A oscillator drive input represents unity oscillator load. <sup>2</sup> For applications requiring more than 16 292As, additional 281s may

be used in a master/slave mode, Refer to Figure 13. <sup>9</sup> Full load consists of 16 model 292As and 281 oscillator slave.

Specifications subject to change without notice.

See Caution note on specifications table.

### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



**CINCH #16 DIP OR EQUIVALENT** 

# **Analog Multipliers/Dividers**

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# Selection Guide Analog Multipliers/Dividers





## AD532

Pretrimmed to  $\pm 1.0\%$  (AD532K) No External Components Required Guaranteed  $\pm 1.0\%$  max 4-Quadrant Error (AD532K) Diff Inputs for  $(X_1 - X_2)(Y_1 - Y_2)/10$  Transfer Function Monolithic Construction

## AD534

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)

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All Inputs (X, Y and Z) Differential, High Impedance for  $[(X_1 - X_2)(Y_1 - Y_2)/10V] + Z_2$  Transfer Function Scale-Factor Adjustable to Provide up to X100 Gain Low Noise Design: 90µV rms, 10Hz–10kHz Low Cost, Monolithic Construction Excellent Long Term Stability



STABLE REFERENCE AND BIAS

TRANSLINEAR MULTIPLIER ELEMENT

0.75 ATTEN

X1 C

X2

Y1

Y2

Z1

Z2 25 v

v٠

## AD539

**Two Quadrant Multiplication/Division Two Independent Signal Channels** Signal Bandwidth of 60MHz (IOUT) Linear Control-Bandwidth of 5MHz Full-Calibrated, Monolithic Circuit

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٧s 0 -Vs TRANSFER FUNCTION (X1 - X2) (Y1 - Y2) - (Z1 - Z2) V<sub>0</sub> = A 10 А OUT HIGH GAIN

OUTPUT

### AD632

Pretrimmed to ±0.5% max 4-Quadrant Error All Inputs (X, Y and Z) Differential, High Impedance for  $[(X_1 - X_2)(Y_1 - Y_2)/10V] + Z_2$  Transfer Function Scale-Factor Adjustable to Provide up to X10 Gain Low Noise Design: 90µV rms, 10Hz-10kHz Low Cost, Monolithic Construction **Excellent Long Term Stability** 

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### ANALOG MULTIPLIERS/DIVIDERS VOL. II, 6-3

# **Selection Guide Analog Multipliers/Dividers**





1.0%/0.5% Accuracy Without Trimming (429A/B)
Low Drift to 1.0mV/°C max
Wideband – 10MHz
0.2% Nonlinearity max (429B)
External Amplifiers not Required
MTBF: 169, 268 Hours

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## AD535

Pretrimmed to ±0.5% max Error, 10:1 Denominator Range (AD535K) ±2.0% max Error, 50:1 Denominator Range (AD535K)

All Inputs (X, Y and Z) Differential **Monolithic Construction** 

**MODEL 429** 

### VOL. II, 6-4 ANALOG MULTIPLIERS/DIVIDERS

# **Orientation** Analog Multipliers/Dividers

The devices catalogued in this section are high-performance modules that accept analog voltages and multiply, divide, square, and/or square-root them, depending on device properties and connections. As the Selection Guide indicates, a variety of additional devices performing comparable functions using IC technologies may be found in Volume I.

Multiplication For two inputs,  $V_x$  and  $V_y$ , a multiplier will provide the output,  $E_{out} = V_x V_y / E_{ref}$ , where  $E_{ref}$  is a dimensional constant, usually of 10V nominal value. If  $E_{ref} = 10V$ ,  $E_{out} = 10V$  when  $V_x$  and  $V_y$  are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement, and mathematical operations in analog computing, curve fitting, and linearizing.

If the inputs may be of either positive or negative polarity, and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the 4 quadrants of the X-Y plane.

Squaring If  $V_x = V_y = V_{in}$ , a multiplier's output will be  $V_{in}^2 / E_{ref}$ . A four-quadrant multiplier, used as a squarer, will have an output that is positive, whether  $V_{in}$  is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads, and mathematical operations.

Division For a numerator input,  $V_z$ , and a denominator input,  $V_x$ , an analog divider will provide the output,  $E_{out} = E_{ref}(V_z/V_x)$ . If  $E_{ref} = 10V$ ,  $E_{out}$  will be 10V or less for  $V_z \leq V_x$ .  $V_x$  is of a single polarity and will not provide meaningful results if it approaches zero too closely. If  $V_z$  may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of  $V_z$ . Analog dividers are used to compute ratios—such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements, and for mathematical operations in analog computing.

Square rooting For a numerator input,  $V_{in}$ , and a denominator input,  $E_0$  (the output fed back to the denominator input), the output of a divider is  $E_0 = E_{ref}(V_{in}/E_0)$ ; hence  $E_0 = \sqrt{E_{ref}V_{in}}$ . A square-rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

### CHOOSING A MULTIPLIER, DIVIDER, etc.

A number of devices are listed here, differing in internal architecutre, external functional configuration, and performance specifications. Most have essentially fixed references; the model 433 is a *multifunction device* that performs the onequadrant operation,  $E_0 = V_z(V_y/V_x)^m$ , where m is an exponent adjustable from 1/5 to 5. With one exception (model 436 precision 2-quadrant divider), all of the devices listed here can be used for any of the functions defined above.

Considerable information on these functions, the nature of

devices to perform them, and extensive discussions of their applications can be found in two publications available from Analog Devices.<sup>1,2</sup> A wealth of information is also to be found in the data sheets for the individual devices, published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Arcbitecture All of the devices in this section rely on the logarithmic properties of silicon P-N junctions. With the exception of models 433 and 436, the circuit employed is basically like that of the "Gilbert cell" (its 4-quadrant-multiplying circuitry and performance are described in (1) and (2), with further references to original sources). The input voltages are converted to currents, the currents are multiplied together and divided by a reference, and the net output current,  $I_x I_y / I_{ref}$ , is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division.



Basic 4-Quadrant Variable-Transconductance Multiplier Circuit

$$I_0 = (I_3 + I_5) - (I_4 + I_6) = \frac{2 V_X V_Y}{I R_X R_Y}$$



In multifunction devices like Model 433, the feedback currents of the input op amps are used to develop logarithmic

<sup>1</sup>Multiplier Application Guide, available upon request

<sup>a</sup>Nonlinear Circuits Handbook, D. H. Sheingold, ed., 1976, 536pp., \$5.95, P.O. Box 796, Norwood MA 02062

voltages across transistor base-emitter junctions; these voltages are summed and differenced and produce an exponential current proportional to  $V_y V_z / V_x$  via another transistor junction in the input path of the output amplifier. Thus, the output voltage is proportional to  $V_y V_z / V_x$ ; an internally generated reference voltage is available as a fixed reference for the odd input in two-variable operations. In the 433, the internal emittervoltage difference proportional to  $\log (V_z/V_x)$  can be amplified or attenuated by the appropriate connection of a resistive attenuator with an attenuation ratio, m; since the antilog of m(log  $V_z/V_x$ ) is  $(V_z/V_x)^m$ , the output of the 433 is proportional to  $V_y(V_z/V_x)^m$ . In the model 436 divider, the inputs are scaled and linearly combined, before the log-antilog computation takes place; the result is that the numerator (of  $V_z/V_x$ ) may have positive or negative values. The 436 circuit is optimized and trimmed for performance as a dedicated divider; it has a fixed reference.

*External functional configuration* As noted earlier, with the exception of the model 436 dedicated divider, all of the devices listed here can be used for multiplication, division, squaring, and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. Performance of pretrimmed devices is optimized in specified modes of operation. The data sheets show how devices are connected for the various modes of operation; where appropriate, the trim circuits and procedures for optimizing performance are provided.

Technologies The devices described in these two volumes are either monolithic integrated circuits or high-performance modules. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The modules in Volume II provide the highest performance: speed (model 429), accuracy as a divider (436), and accuracy in multifunction applications (433). On the other hand, the ICs in Volume I provide economy of cost and space, and the availability of "mil-temp" range ( $-55^{\circ}$ C to  $+125^{\circ}$ C) versions. The pretrimmed IC's (AD534, AD535 and AD532) use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors to 0.25%, and linearities as yet unmatched in the industry.

*Performance* Multiplier performance, specifications and test circuitry are described in great detail in the NONLINEAR CIRCUITS HANDBOOK. Here is a brief digest of the factors relating to low-frequency performance.

In theory, a multiplier has an output which is ideally the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities, which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practice (see the figure), the multiplier may be considered



Functional Block Diagram of Typical Multiplier/Divider

Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The figure shows a model used for considering errors.  $X_0$ and  $Y_0$  are input offset voltages,  $Z_0$  is the offset-referred-tothe-input of the output amplifier, and F(X', Y') is the nonlinearity, viewed as the departure from the ideal multiplication,  $\frac{X'Y'}{10R}$ . The output equation, including the errors is of the form

$$E_{o} = \frac{XY}{10B} \pm \left[ \frac{X_{o}Y}{10B} \pm \frac{XY_{o}}{10B} \pm Z_{o} + f(X,Y) \right]$$
Product
$$\underbrace{X_{offset}}_{Linear} Feedthrough}_{"Y"} \underbrace{V_{offset}}_{"X"}$$
Output Nonlinearity
offset and feedthrough

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by applying external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

 $f(X,Y) \cong |V_X| \epsilon_X + |V_V| \epsilon_V$ 

were  $\epsilon_x$  and  $\epsilon_y$  are the specified fractional linearity errors (%/100) and  $\dot{V}_x$  and  $V_y$  are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage  $(10V/V_x)$ , and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (e.g., 10:1), will always benefit greatly by the trimming of offsets, especially Zo (affects offsets) and Xo (affects gain), for small values of X.

### **DEFINITIONS OF SPECIFICATIONS\***

Accuracy is defined in terms of total error of the multiplier at room temperature and constant nominal supply voltage. Total error includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. Temperature dependence and supply-voltage effects are specified separately.

Scale Factor The scale-factor error (or gain error) is the difference between the average scale factor and the ideal scale factor (e.g.,  $(10V)^{-1}$ ). It is expressed in percent of the output signal. Temperature dependence is specified.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output offset vs. temperature is also specified.

Linearity Error or Nonlinearity is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an input offset at the zero input, which can be trimmed out (but can drift and has a temperature specification), and a nonlinear one, which is irreducible. Feedthrough is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the multiplier may improve smallsignal resolution significantly.

### Dynamic Parameters include: small-signal bandwidth, fullpower response, slew(ing) rate, small-signal amplitude error, and settling time.

Small-signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

Full-power response is the maximum frequency at which the multiplier can produce full-scale voltage into its rated load without noticeable distortion.

Slew(ing) rate is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a fullscale step input.

Small-signal amplitude error is defined in relation to the frequency at which the amplitude response, or scale factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Settling time, for the product of a ±10V step and 10Vdc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

Vector error is the most-sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.

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VOL. II, 6–8 ANALOG MULTIPLIERS/DIVIDERS
# 

# Accurate, Wideband, Multiplier, Divider, Square Rooter

#### FEATURES:

1.0%/0.5% Accuracy without Trimming (429A/B). Low Drift to 1.0mV/°C max Wideband – 10MHz 0.2% Nonlinearity max (429B) External Amplifiers not Required MTBF: 169, 268 Hours

APPLICATIONS: Fast Divider Modulation and Demodulation Phase Detection Instrumentation Calculations Analog Computer Functions Adaptive Process Control Trigonometric Computations

#### GENERAL DESCRIPTION

The model 429, an extremely fast multiplier/divider, should be considered if bandwidth, temperature coefficient, or accuracy are critical parameters. Based on the transconductance principle to achieve high speed, the model 429 offers a unique combination of features, those being ½% max error (429B) and 10MHz small signal bandwidth.

Both models 429A and 429B are internally trimmed achieving max errors of 1.0% and 0.5% respectively. By fine trimming the offset and feedthrough with external trim potentiometers typical performance may be improved to 0.5% for the 429A and 0.2% for the 429B.

In addition to high accuracy and high bandwidth, the model 429 offers exceptionally good stability for changes in ambient temperature. Model 429B is 100% temperature tested in order to guarantee an overall accuracy temperature coefficient of only 0.04%/°C max. Additionally, offset drift is held to only 1mV/°C max. To satisfy OEM requirements of low cost, the 429 uses transconductance principles with the latest design techniques and components to achieve guaranteed performance at competitive prices.

#### MULTIPLICATION ACCURACY

Multiplication accuracy is generally specified as a percentage of full scale output. This implies that error is independent of signal level. However, for signal levels less than 2/3 of full scale, error tends to decrease roughly in proportion to the input signal. A good approximation of error behavior is:

f (X, Y)  $\cong$  |X|  $\epsilon_x$  + |Y|  $\epsilon_y$ , where  $\epsilon_x$  and  $\epsilon_y$  are the fractional nonlinearities specified for the X and Y inputs

*EXAMPLE:* For model 429A,  $\epsilon_x = 0.5\%$ ,  $\epsilon_y = 0.3\%$ . What maximum error can one expect for x = 5V, y = 1V, providing



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the offset is zeroed out? Can one get less by interchanging inputs?

- 1. Nominal output is XY/10 = (5)(1)/10 = 500 mV
- Expected error is (5) (0.5%) + (1) (0.3%) = 28mV, 5.6% of output (0.28% of F.S.)
- Interchanging inputs (1) (0.5%) + (5) (0.3%) = 20mV, 4.0% of output (0.20% of F.S.)

Compare this with the overly conservative error predicted by the overall 1% of full scale specification: 100mV, or 20% of output.

#### FREQUENCY RELATED SPECIFICATIONS

Accuracy, and its components, feedthrough, linearity, gain, (and phase shift) are frequency dependent. Feedthrough is constant up to 100kHz for the Y input, and up to 400kHz for the X input. Beyond these frequencies it rises at approximately a 6dB/octave rate due to distributed capacitive coupling. A plot of typical feedthrough vs. frequency is shown in Figure 1. For this measurement one input is driven with a 20V p-p sine wave while the other input is grounded and the feedthrough is measured at the output. This error will decrease roughly in proportion to the input signal, and will also vary with temperature (about  $0.01\%/^{\circ}$ C of the nonzero input). Low frequency feedthrough error can be further reduced from the internally trimmed limits by the use of optional external potentiometers.

Nonlinearity likewise increases with frequency at a 6dB/ octave rate above the break frequency. With the Y input driven at 10V p-p, and the X input anywhere between  $\pm$ 10V dc, the break frequency is 25kHz. For corresponding X input conditions, the break occurs at 60kHz. Figure 2 is a plot of the typical nonlinearity vs. frequency for the model 429.

# SPECIFICATIONS (typical @ +25°C and ±15VDC unless otherwise noted)

MODEL	429A	429B
MULTIPLICATION		
CHARACTERISTICS		
Output Function	XY/10	•
Error, with Internal Trim, at +25°C	±1% max	±0.5% max
Error, with External Trim, at +25°C	±0.7%	±0.3%
Avg. vs. Temp (-25°C to +85°C)	±0.05%/°C	±0.04%/°C max
Avg vs. Supply	±0.05%/%	•
SCALE FACTOR		
Initial Error at +25°C	0.5%	0.25%
Avg vs. Temp (-25°C to +85°C)	0.03%/°C	0.02%/°C
Avg vs. Supply	0.03%/%	•
OUTPUT OFFSET		
Initial at +25°C (Adjustable to Zero)	±20mV max	±10mV max
Avg vs. Temp (-25°C to +85°C)	±2mV/°C	±1mV/°C max
Avg vs. Supply	±1mV/%	*
NONLINEARITY		
X Input		
$(X = 20V p - p 50Hz, Y = \pm 10V)$	0.5% max	0.2% max
Y Input		
$(Y = 20V p - p 50Hz, X = \pm 10V)$	0.3% max	0.2% max
FEEDTHROUGH		
X = 0, Y = 20V p-p, 50Hz	50mV p-p, max	20mV p-p, max
With External Trim	16mV p-p	10mV p-p
Y = 0, X = 20V p - p, 50Hz	100mV p-p, max	30mV p-p, max
With External Trim	50mV p-p	20mV p-p
BANDWIDTH		
-3dB	10MHz	· ·
Full Power Response	2MHz min	•
Slew Rate	120V/µs min	
1% Amplitude Error	300kHz min	
1% Vector Error (0.57°)	50kHz min	
Differential Phase Shift $(\theta_x - \theta_y)$	1° @ 1MHz	•
Small Signal Rise Time 10-90%	40ns	:
Settling to ±1% (±10V step)	500ns	
Overload Recovery	0.2μs	· · · · · · · · · · · · · · · · · · ·
OUTPUT NOISE		
5Hz to 10kHz	0.6mV rms	
5Hz to 10MHz	3.0mV rms	<u> </u>
OUTPUT CHARACTERISTICS		
Voltage, 1kΩ load	±11V min	
Current	±11mA min	
Load Capacitance	0.01µF max	*
INPUT RESISTANCE	_	
X Input	10kΩ±5%	•
Y Input	11k\$2±2%	
Z Input	27k\2±10%	
INPUT BIAS CURRENT		•
Input X, Y, Z	±100nA	•
Z	±20µA	<u> </u>
MAXIMUM INPUT VOLTAGE		
For Rated Accuracy	±10.5V	*
Maximum Safe	±16V	*
WARM UP	-	
To Rated Specifications	l second	*
POWER SUPPLY <sup>1</sup>	· •	
Rated Performance	±(14.8 to 15.3)V dc	*
Operating	±(14 to 16)V dc	*
Quiescent Current	±12mA	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL	1	
Weight	2 oz.	*
Socket	AC1023	* '
Case Dimensions	1.5" x 1.5" x 0.62"	*

NOTES

\*Specifications same as model 429A.

<sup>1</sup> Recommended power supply, ADI model 904, ±15V @ 50mA output. Specifications subject to change without notice.



All trim pots  $20k\Omega$ .

#### VOL. II, 6-10 ANALOG MULTIPLIERS/DIVIDERS

Gain and input to output phase shift for the model 429 are shown in Figure 2. Naturally, no multiplier will maintain accuracy at frequencies approaching the small signal bandwidth. For the model 429, the 1% amplitude error will occur at 500kHz. If input to output phase shift is a criterion, then the 1% "vector" error occurs at 50kHz.



Figure 1. Feedthrough vs Frequency



Figure 2. Typical Amplitude and Phase vs Frequency

#### **OPTIONAL TRIM – MULTIPLY MODE**

As shipped, the multiplier meets its listed specifications without use of any external trim potentiometers. Terminals are provided for optional feedthrough and offset adjustments. Using these adjustments overall static multiplication error may be reduced to only 0.2%. The  $20k\Omega$  trim potentiometers should be connected across the  $\pm$  supply voltage terminals with the arm of each potentiometer connected to the desired balance terminal (see Specifications page).

#### ADJUSTMENT PROCEDURE FOR OFFSET

- 1. Jumper X input and Y input to ground.
- 2. Adjust  $R_0$  for an output of zero volts.
- 3. Remove jumper from X and Y inputs.

#### ADJUSTMENT PROCEDURE FOR FEEDTHROUGH

- 1. Jumper Y input to ground and apply 20V p-p at 1kHz to X input.
- 2. Adjust Ry for minimum output voltage.
- 3. Remove jumper from Y input.
- 4. Jumper X input to ground and apply 20V p-p at 1kHz to Y input.
- 5. Adjust  $R_X$  for minimum output voltage.
- 6. Remove jumper from X terminal.

### Applying the Fast Multiplier

#### DIVISION

The high bandwidth and excellent linearity of model 429 allows it to be used in divider applications achieving high performance in the dc to 8MHz region. Restrictions imposed on divide operation, and the contribution of error terms are illustrated in the error analysis below.



Figure 3. Divider Circuit

Shown in Figure 3 is a typical multiplier/divider which has been connected for divide operation by inserting the multiplier cell, M, in the op amp's feedback loop. Errors associated with the op amp, A<sub>1</sub>, are incorporated in  $\epsilon$ , which represents all errors. In order to insure negative feedback, the X input range is restricted to negative values.

Summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{\frac{XY}{10} + \epsilon}{R}$$

Solving for Y, which is also  $\epsilon_0$ :

or,

$$Y = \frac{10 (Z - \epsilon)}{X}$$

$$\epsilon_0 = \frac{10Z}{Y} - \frac{10\epsilon}{Y}$$

And now breaking  $\epsilon$  into its constituents

<i>c</i> .	_10Z	10E <sub>NV</sub>	10E <sub>OS</sub>	10E <sub>OS</sub> /°C	$10E_{NLX}$	10E <sub>NLY</sub>
c0 ·	<u>x</u>	X	x	x	x	x
	ideal divider	noise error	offset error	offset drift error	X non- linearity	Y non- linearity

These errors can be broken down into two categories, static errors and signal dependent errors. All of the static errors associated with the divide mode are inversely proportional to the denominator signal level. The signal dependent errors are the X and Y nonlinearities. For model 429B nonlinearity errors are 0.2% for both the X and Y inputs. Substituting these values in the error terms yields:

$$\frac{10 (0.2\%) X}{X} - \frac{10 (0.2\%) Y}{X}$$

The importance of using the terminal with largest nonlinearity for the denominator is revealed by the above expression. Effects of X nonlinearity are virtually independent of signal level and may be trimmed out. Nonlinearities of Y typically contribute 200mV for X = Z = 1V i.e., (10 [0.2%] 10V) = 200mV. This error can be reduced if external trims are used to optimize divider performance.

Bandwidth is also degraded with a decrease in denominator level, due to the increase in system gain;

i.e.) for 
$$X = Z = 1V$$
,  $\epsilon_0 = 10V$ 

and 
$$\frac{\epsilon_0}{Z} = \frac{10}{1} = 10$$

Since the gain bandwidth product is constant, a bandwidth of 1/10 of that obtained for full scale denominator levels will be obtained for division at 1V levels.

For other denominator levels, bandwidth is determined by:

B. W. = 
$$\frac{\text{Denominator Level}}{\text{Full Scale Denominator}} \times (\text{Multiplier B.W.}) \times K$$

where  $\dot{K}$  is a constant having a value less than unity. It is introduced due to a combination of stray capacitance paralleling the multiplier cell and effects of feedthrough. For model 429

B.W. = 
$$\left(\frac{X}{10}\right)$$
 8MHz

Before selecting a multiplier/divider for divide applications, errors resulting from the lowest anticipated denominator signal should be considered. After such considerations have been made, one can further appreciate the importance of starting with an accurate, high speed multiplier such as model 429. It is also highly recommended that the optional trim procedure for division be performed.

#### **OPTIONAL TRIMMING – DIVIDE MODE**

Connections are made as shown on Specifications page.

The suggested trim procedure is (starting with centered adjust adjustments):

- \*1. With Z = 0, trim R<sub>0</sub> to hold output constant, as X is varied from -10V toward -1.0V.
  - 2. With Z = 0, trim  $R_Y$  for zero at X = -10V.
  - With Z = X and/or Z = -X, trim R<sub>X</sub> for minimum worst-case variation as X is varied from -10V to -1.0V.
  - 4. Repeat 1 and 2 if step 3 required large initial adjustment.

\*For best accuracy X should be allowed to vary from -10V to lowest expected denominator.

#### SQUARE ROOTING

When connected as shown on Specifications page, the model 429 will provide the square root of  $Z_{IN}$ .

By summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{XY}{10R} + \frac{\epsilon}{R} = \frac{Y^2}{10R} + \frac{\epsilon}{R}$$

where  $\epsilon$  represents all errors associated with the multiplier. Solving for the output voltage, Y.

$$\epsilon_0 = \pm \sqrt{10 (Z - \epsilon)}$$

There are two values of  $\epsilon_0$  for every value of Z. However, only negative values of  $\epsilon_0$  will provide the negative feedback necessary for circuit stability. To restrict the output from going positive, a diode is connected as shown on Specifications page. The output is then:

$$\epsilon_0 = -\sqrt{10 (Z - \epsilon)}$$

Errors,  $\epsilon$ , associated with the multiplier, are inside the square root and consequently their effect, for large values of Z, is

reduced. The reason for the improved performance can be seen by inspecting the circuit. The output is fed back to both the X and Z terminals, resulting in twice the feedback as would be obtained for the divide mode. An alternative method of considering error performance is to consider errors as being at the Z terminal. By differentiating the ideal transfer function with respect to Z, errors for various values of Z may be determined:

$$\frac{\mathrm{d}\mathbf{e}_0}{\mathrm{d}\mathbf{Z}} = \frac{\mathrm{d}}{\mathrm{d}\mathbf{Z}} \sqrt{10\mathbf{Z}} = \frac{1}{2}\sqrt{\frac{10}{\mathbf{Z}}}$$

The factor of  $\frac{1}{2}$  has the advantage of reducing errors by a factor of 2 for Z = 10, but also introduces the potential problem of instability. Since the feedback gain is the reciprocal of the forward gain, the slope of the forward gain is 2. Additional phase margin is required to support the increased gain in the feedback path. Model 429 is optimized for phase margin in the multiply and divide modes producing minimum vector errors at high frequencies. To avoid the potential problem of instability, the RC network shown previously is recommended. This network restricts the bandwidth and guarantees stability for all positive values of Z.

#### **OPTIONAL ADJUSTMENT PROCEDURE – SQUARE ROOT**

- 1. Apply a voltage to the Z terminal equal to the lowest anticipated input voltage.
- 2. Adjust  $R_0$  such that  $e_0 = -\sqrt{10Z}$ , where Z is the voltage applied in step 1.

#### DIVISION SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	.10(Z)/X
Numerator Range	±10V
Denominator Range,	
1% Accuracy	-1 to -10V
Denominator Range,	
5% Accuracy	,-0.2V to -10V
Bandwidth Formula,	
(Hz, -3dB)	.(8MHz)(X)/10

#### SQUARE ROOTING SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	$-\sqrt{10(Z)}$
Dynamic Range	1000 to 1
	(+0.010V ≤Z≤+10V)
Accuracy (% of Full Scale)	. 0.5%
Bandwidth Formula,	
(Hz, -3dB)	$(5 \mathrm{MHz}) \sqrt{ \mathbf{X} /10}$

Table 1. Division & Square Rooting Specifications



Figure 3. Typical Error Performance of Model 429 in Divide Mode for Worst Case of  $|e_0| = 10V$ 

VOL. II, 6-12 ANALOG MULTIPLIERS/DIVIDERS

# **RMS-to-DC Converters**

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442J/K/L 8MHz-Bandwidth rms-to-dc Converters	7-7

# Selection Guide RMS-to-DC Converters





### AD536A

True rms-to-dc Conversion Laser-Trimmed to High Accuracy 0.2% max Error (AD536AK) 0.5% max Error (AD536AJ) Wide Response Capability: Computes rms of ac and dc Signals 300kHz Bandwidth: V<sub>rms</sub>>100mV 2MHz Bandwidth: V<sub>rms</sub>>100mV 2MHz Bandwidth: V<sub>rms</sub>>10 Signal Crest Factor 7 for 1% Error dB Output with 60dB Range Low Power: 1mA Quiescent Current Single or Dual Supply Operation Monolithic Integrated Circuit -55°C to +125°C Operation (AD536AS) Page Vol. I 6-43

### AD636

True rms-to-dc Conversion 200mV Full Scale Laser-Trimmed to High Accuracy 0.5% max Error (AD636K) 1.0% max Error (AD636J) Wide Response Capability: Computes rms of ac and dc Signals 1MHz – 3dB Bandwidth: V<sub>rms</sub>>100mV Signal Crest Factor of 6 for 0.5% Error dB Output with 50dB Range Low Power: 800µA Quiescent Current Single or Dual Supply Operation Monolithic Integrated Circuit Vol. I 6–71





### AD637

High Accuracy 0.02% Max Nonlinearity, 0 to 2V rms Input 0.10% Max Error to Crest Factor of 3
Wide Bandwidth
8MHz at 2V rms Input
600kHz at 100mV rms
Computes:
True rms
Square
Mean Square
Absolute Value
dB Output (-60dB Range)
Chip Select-Power Down Feature Allows:
Analog "3-State" Operation
Quiescent Current Reduction from 2.2mA to 350μA

**MODEL 442** 

to Meet Specifications

DC to 8MHz Response (-3dB) High Accuracy: With No Ext. Trim: ±2mV ±0.15% of Rdg., max With Ext. Trim: ±1mV ±0.05% of Rdg., max Low Drift: ±(35µV ±0.01% of Reading)/°C max, 442L Fast Settling Time: 5ms to 1% All Hermetically Sealed Semiconductors No External Components Required Vol. II 7-7

Page

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# Orientation RMS-to-DC Converters

The 442 is a high-accuracy wide-bandwidth true-rmis-to-dcconversion module. As the Selection Guide indicates, additional devices to perform rms-to-dc conversion, employing IC technology, may be found in Volume I. Devices of this class compute the instantaneous square of the input signal, average it, and take the square root of the result, to provide a dc voltage that is proportional to the rms of the input (and, in the case of the AD536A and AD636 ICs, an auxiliary dc voltage that is proportional to the *log* of the rms, for dB measurements).

Excellent pre-trimmed performance, improvable by simple optional trims, makes these devices ideal for all types of laboratory and OEM rms instrumentation where amplitude measurements must be made with high accuracy, independently of waveshape.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolutedeviation, or "ac average." It is performed by taking the absolute value of (i.e., full-wave or half-wave rectifying) a signal, filtering it, and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform and will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

Examples of applications include noise measurement - for example, thermal noise, transistor noise, and switch-contact noise. True-rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties. True-rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise, and acoustical noise. The electrical signals produced by these mechanical actions are often noisy, non-periodic, nonsinusoidal, and superimposed on dc levels, and require true-rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

The basic approach used in these converters for computing the rms is to take the absolute value, square it, and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$E_{o} = Avg.\left[\frac{V_{in}^{2}}{E_{o}^{2}}\right] \cong \sqrt{Avg.(V_{in}^{2})}$$

is valid if the averaging time-constant is sufficiently long compared with the periods of the lowest-frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter, using an external filtering capacitance. Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, an additional stage of 2pole filtering is useful. The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of  $C_{ext}$ .

WAVEFORM			RMS	MAD	MAD	CREST FACTOR
		SINE WAVE	Vm √2 0.707 Vm	$\frac{2}{\pi} V_m$ 0.637 V_m	$\frac{\pi}{2\sqrt{2}} = 1.111$	√2 = 1.414
		SYMMETRICAL SQUARE WAVE OR DC	Vm	Vm	1	1
-	Vm	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	<u>V</u> m 2	$\frac{2}{\sqrt{3}}$ = 1.155	√3 = 1.732
CREST FACTOR		GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED.q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F.         q           1         32%           2         4.6%           3         0.37%           3.3         0.1%           3.9         0.01%           4         63ppm           4.4         10ppm           6         2x10.9
-	0 +T +T 	PULSE TRAIN 7 MARK/SPACE 1 00 0.25 0.0625 0.0156 0.0159 0.015 0.0159	V <sub>m</sub> √ η V <sub>m</sub> 0.5V <sub>m</sub> 0.125V <sub>m</sub> 0.125V <sub>m</sub> 0.1V <sub>m</sub>	V <sub>m</sub> η V <sub>m</sub> 0.25V <sub>m</sub> 0.0156V <sub>m</sub> 0.0156V <sub>m</sub>	$ \frac{1}{\sqrt{\eta}}, $ 1 2 4 8 10	$ \frac{1}{\sqrt{\eta}} $ 1 2 4 8 10

#### VOL. II, 7-4 RMS-TO-DC CONVERTERS

#### PERFORMANCE SPECIFICATIONS

Considerable information regarding rms-to-dc converter circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK.<sup>1</sup> In addition, useful applications information on auxiliary filtering can be found in the article "Measure RMS with Less Ripple in Less Time."<sup>2</sup>

The most-salient feature of a true rms-to-dc converter is that it ideally has no error due to an indirect approximation to the rms. Static errors are due only to scale-factor, linearity, and offset errors; dynamic errors are due to insufficient averaging time at the low end and finite bandwidth and slewing rate at the upper end. Linearity errors affect crest factor in midband. Dynamic errors are also a function of signal amplitude, due in part to the variation of bandwidth of the "log" transistors with signal level.

Total Error A specification for quick reference, this is the maximum deviation of the dc component of the output voltage from the theoretical output value over a specified range of signal amplitude and frequency. It is shown as the sum of a fixed error and a component proportional to the theoretical output ("% of reading"). It is specified for a sinusoidal input in a given frequency and amplitude range. The fixed error-component includes all offset errors and irreducible nonlinearities; the %-of-reading component includes the linear scale-factor error.

Total Error, external adjustment is the amount by which the output may differ from the theoretical value when the output offset and scale factor have been trimmed. Note that the fixed error-component cannot be reduced to zero, even though the output offset can be nulled at zero input. This is because of residual input offsets and inherent nonlinearities in the converter. *Total Error vs. Temperature* is the average change of %-of-fullscale error component plus the average change of percent of reading error component per degree Celsius, over the rated temperature range.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for -3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal -30% of reading. It is a function of amplitude.

Crest Factor (a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case - rectangular pulse - input signal.

Filter Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per  $\mu$ F of added external capacitance.

*Input:* The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

*Output:* The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Power Supply: Power-supply range for specified performance, power-supply range for operation, and quiescent current drain.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements ( $T_H - 25^{\circ}C$ ), ( $25^{\circ}C - T_L$ ), when measured.

 <sup>1</sup>Nonlinear Circuits Handbook, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold.
 <sup>2</sup>ANALOG DIALOGUE 9-3, 1975, pp 21-22 7

# 

# Wideband, High Accuracy True rms-to-dc Converter

**MODEL 442** 

FEATURES

DC to 8MHz Response (-3dB) High Accuracy:

With No Ext. Trim:  $\pm 2mV \pm 0.15\%$  of Rdg., max With Ext. Trim:  $\pm 1mV \pm 0.05\%$  of Rdg., max Low Drift:  $\pm (35\mu V \pm 0.01\%$  of Reading)/<sup>o</sup>C max, 442L Fast Settling Time: 5ms to 1% Small Size: 1.5" x 1.5" x 0.4" All Hermetically Sealed Semiconductors

#### APPLICATIONS

Wideband rms Instrumentation Telephone, Telegraph & Modem Test Equipment Vibration Analysis Sound & Noise Level Instrumentation Mean Square Measurements

#### GENERAL DESCRIPTION

Model 442 is a high performance true rms-to-dc converter featuring 8MHz bandwidth, low drift to  $\pm 35 \mu V/^{\circ} C \pm 0.01\%$  of reading/<sup>°</sup>C maximum, and  $\pm 1\%$  reading error to 800kHz. Unlike competing designs, model 442 achieves its high accuracy over a very wide input signal range. With no external adjustment, accuracy is held to within  $\pm 2mV \pm 0.15\%$  of reading for input signals of 0 to  $2V_{rms}$ . If optional adjustments are performed, this accuracy can be improved to  $\pm 1mV \pm 0.05\%$  of reading. Model 442 is designed to be used in high performance instrumentation where response to low level, high speed signals, is of greatest importance.

The compact, log-antilog circuit design of model 442 results in high accuracy measurements on sinewave signals and complex waveforms such as pulse trains. Reading error increases 0.2% for signals with crest factors up to 7. In addition, true rms measurement can be performed directly on signals containing both ac and dc components.

Model 442 is available in three low drift selections offering maximum drift performance over 0 to  $+70^{\circ}$ C range; model 442L:  $\pm(35\mu V \pm 0.01\% \text{ of rdg.})/^{\circ}$ C max; model 442J:  $\pm(50\mu V \pm 0.01\% \text{ of rdg.})/^{\circ}$ C max; model 442J:  $\pm(100\mu V \pm 0.01\% \text{ of rdg.})/^{\circ}$ C max.

#### WHERE TO USE MODEL 442

Excellent untrimmed performance along with simple, optional trims make model 442 the ideal component for all types of laboratory and OEM rms instrumentation where wideband measurements must be made with high accuracy. Model 442 is ideally suited for measuring thermal noise, transistor noise and switch contact noise. True rms measurement is the only technique to accurately measure system noise and thereby assist the designer in reducing this noise. Model 442 is also useful for measuring mechanical phenomena such as strain, stress,



vibration, shock, expansion and contraction. The electrical signals produced by these mechanical actions are often noisy, nonperiodic, nonsinusoidal and superimposed on dc levels, therefore requiring true rms devices for accurate measurements.

Model 442 is also required for accurate measurements on low repetition rate pulse trains. For pulse trains with crest factors of 10, a 3dB bandwidth of 400 times the pulse rate is required to achieve 1% accuracy and 4000 times the pulse rate is needed for 0.1% accuracy.

Model 442 may also be connected (see Figure 3) to measure the MEAN SQUARE of a signal ( $e_0 = e_{in}^2/V_R$ ). The Mean Square of a random signal is equal to the variance ( $\sigma^2$ ).

#### TOTAL ACCURACY

Total output error is specified as the sum of two components; a fixed term plus a percentage of output signal. Model 442 has a rated sinewave accuracy of  $\pm 1 \text{mV} \pm 0.05\%$  max (externally trimmed), which for a one volt rms sinewave, results in a  $\pm 1.5 \text{mV}$  maximum error ( $\pm 1 \text{mV} \text{ fixed error plus } \pm 0.5 \text{mV}$ reading error). The fixed error component is comprised of output offsets and linearity errors. Both of these error terms have been minimized in the model 442 as a result of special output circuit design and sophisticated factory offset trim procedures. Output offset can be adjusted for minimum error by means of an external adjustment (see Figure 2). The % of reading error is attributed to nonlinearity and scale factor errors. Scale factor error may also be reduced by external adjustment of an optional 5k $\Omega$  potentiometer (see Figure 2).

# SPECIFICATIONS\*\*

### (typical @ $+25^{\circ}$ C and V<sub>s</sub> = $\pm 15$ V dc, unless otherwise noted)

MODEL	442]	442K	442L	OUTLINE DIMENSIONS
TRANSFER EQUATION	$c_0 = \sqrt{avg (e_{in})^2}$	•	•	Dimensions shown in inches and (mm).
ACCURACY				
Total Error, Sinewave Input, f ≤ 20kHz				1.51 MAX (38.1)
Input Bange: 0 to 2V	+2mV +0.15% of Bdg max	•	•	0.41 MAX
External Adjustment	sent sources in or Rugs, max			(10.2)
Input Range: 0 to 2Vms	±1mV ±0.05% of Rdg., max	•	•	
10mV <sub>rms</sub> to 2V <sub>rms</sub>	±0.5mV ±0.05% of Rdg., max	•	•	UU
Additional Error, Sinewave Input,				0.04 DIA (1.02)
20RH2 = I = 500KHz With or Without External Adjustment				0.20 TO 0.25 (5 TO 6 4)
For Any Input Range	(±25µV ±0.0025% of Rdg) x			
rorring input times	(f(kHz) - 20kHz)	•	•	┠╆╌┾╼╪╼╪╼╪╼╪╼╪╼╪╼╪┱╋╗
	1kHz , max			
vs. Temperature (0 to +70°C), max	±100µV/°C plus	±50µV/°C plus	±35µV/°C plus	
	±0.01% of Rdg./°C	±0.01% of Rdg./°C	±0.01% of Rdg./°C	4-0-COM -1 [
vs. Supply Voltage	±0.1mV/%	• *	•	
Warm-Up Time	5 minutes	•		GAIN-0-7
FREQUENCY RESPONSE, SINEWAVE INF	UT			<u> </u>
±1% Reading Error	500HU-		•	
input: / V ms	200kHz	•	•	· ┠┼┿┽┼┼┊┽┼╆┽╶╡┽┽┼┥┨
1Vms	800kHz	•	•	
0.2Vms	120kHz	•	•	0.1 GRID
0.1Vms	80kHz	•	•	Mainhas 40 minute
0.01V <sub>ms</sub>	25kHz	•	•	Weight: 40 grams
-3dB Reading Error	6141L		•	
input: / V ms	5MHZ 8MHz	•	•	MATING SOCKET AC1016
1Vms	7MHz	•	•	
0.2V <sub>ms</sub>	3MHz	•	•	5
0.1Vms	2MHz	•	•	
0.01V <sub>ms</sub>	300kHz	•	•	
Internal Filter Time Constant	1.5ms	•	•	442 2 - O BOUT
Total Averaging Time Constant <sup>2</sup>	$15ms/\mu r$ 1 5ms + 15ms/ $\mu F$	•	•	
CREST FACTOR				
±0.2% Additional Reading Error	7	•	•	
±0.5% Additional Reading Error	10	•	. •	
INPUT SPECIFICATIONS				eO = √ eIN.
Voltage				Figure 1. Wiring Connections for
Signal Range	±10V <sub>peak</sub> min	•	•	rms Measurements (No External
Safe Input	$\pm V_{S}$	•	•	Trim
Impedance	2.3832 ±10%	·		
OUTPUT SPECIFICATIONS®				+vsQ
Voltage	+10.0V min	•	•	Ro 2-0-9 5-0+Vs
Current	+5mA min	•		∫ mo 4 - 0 com
Impedance	0.1Ω	•	•	-vs 0 -vs
Offset Voltage, @ +25°C	±2mV max	•	•	
With External 20kΩ Trim Pot	Adjustable to Zero	•	·	
POWER SUPPLY <sup>4</sup>				
Voltage, Rated Specifications	±15V dc	•	•	L ~
voitage, Operating	=(0 to 18)V dc +12mA	•	•	Rst
TEMBER ATURE DANCE	-1400		<u> </u>	SCALE FACTOR
Rated Performance	$0 \text{ to } +70^{\circ} \text{C}$	•		Rs = 5kΩ Ro = 20kΩ
Operating	-25°C to +85°C	•	•	
Storage	-55°C to +125°C	•	•	*SELECT C1 FOR INCREASED AVERAGING TIME CONSTANT.
CASE SIZE	1.5" x 1.5" x 0.4"	•	•	
				Figure 2. Optional External
NOTES				Adjustment for rms Measurements

+VsQ

Ro

\*INO .v.d

VREFO

R<sub>O</sub> = 20kΩ

0 +Vs -О сом

-0 -Vs

O \*0UT

eo = Rep

VREF +10 VOLTS

442

Figure 3. Wiring Connections for Mean Square Measurements with Adjustable Scale Factor (V<sub>REF</sub>)

NOTES \*Specifications same as model 442]. \*Contact sales office for complete 4 page data sheet. 'Error is specified as the sum of two components: a fixed term plus a percentage of output signal (reading), Refer to TOTAL ACCURACY. TOTAL ACCURACY.

CONNEX OCCURACY. <sup>2</sup> Connect optional filter capacitor between pin 1 and pin 2 (see Figure 2). Pin 1 is protected for shorts to ground and the positive supply voltage. Pin 1 is not protected for negative voltage greater than 1 volt. <sup>3</sup> Protected for short circuit to ground and/or either supply voltage. <sup>4</sup> Recommended power supply: Analog Devicest model 904.

Specifications subject to change without notice.

# **Log-Antilog Amplifiers**

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# Selection Guide Log-Antilog Amplifiers



### **MODEL 755, MODEL 759**

High Accuracy: Models 755N, 755P Low Cost: Models 759N, 759P Complete Log-Antilog Amplifiers: External Components not Required Temperature-Compensated Internal Reference 6 Decades Current Operation: 1nA to 1mA 1% max Error: 1nA to 1mA (755) 20nA to 200µA (759) 4 Decades Current Operation: 1mV to 10V 1% max Error: 1mV to 10V (755) 1mV to 2V (759)



### **MODEL 757**

6 Decade Operation – 1nA to 1mA 1/2% Log Conformity – 10nA to 100µA Symmetrical FET Inputs Voltage or Current Operation Temperature Compensated Complete Log Ratio Amplifier: External Components not Required Page Vol. II 8-7

Vol. II 8–11 The devices catalogued in this section are complete, self-contained modules that provide output voltage proportional to the logarithm or the antilogarithm (exponential) of an input quantity. These modules operate on the instantaneous values of inputs from dc to an upper cutoff frequency below 1MHz.

#### LOGS AND LOG RATIOS

In the logarithmic mode, the ideal output equation is

$$E_{o} = -K \log_{10} \left( \frac{l_{in}}{l_{ref}} \right)$$

 $E_o$  can be positive or negative; it is zero when the ratio is unity, i.e.,  $I_{in} = I_{ref}$ . K is the output scale constant; it is equal to the number of output volts corresponding to a decade\* change of the ratio. In the 755 and 759 log amplifiers, K is pin-programmable to be either 1V, 2V, or 2/3V, or externally adjustable to any value  $\ge 2/3V$ ; in the model 757 logratio amplifier, K may be either a preset value of 1V, or an arbitrary value adjustable by an external resistance ratio.

I<sub>in</sub> is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes  $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$ . In models 755 and 759, the magnitude of  $I_{ref}$  is internally fixed at 10 $\mu$ A ( $E_{ref} = 0.1$ V) or externally adjusted; but model 757 is a *log-ratio* amplifier, in which both  $I_{in}$  and  $I_{ref}$  (or  $E_{in}$  and  $E_{ref}$ , using external scaling resistors) are input variables.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive*; "P" indicates that only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 759N, with K = +1V, would produce an output voltage,  $E_o = -1V \log (100) = -2V$ ; on the other hand, -10V applied to model 759P, with K = 1V, would produce an output voltage,  $E_o = -(-1V) \log (100) = +2V$ . The figure shows, in condensed form, the outputs of P and N log-amps, with differing K values, for voltage and current inputs.

Log amplifiers in the log mode are useful for applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the logratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

\*A decade is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1000 (3 decades), the output would change by 6V.

# **Orientation** Log-Antilog Amplifiers







Log of Voltage

Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

#### ANTILOGS

In the *antilogarithmic* (exponential) mode, the ideal output equation is

$$E_0 = E_{ref} \exp_{10} \left(-E_{in}/K\right)$$

 $E_{in}$  can be positive or negative; when it is zero,  $E_o = E_{ref}$ . However,  $E_o$  is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = -2V, if  $E_{in} = +4V$ , and  $E_{ref} = -0.1V$ , then

 $E_0 = -0.1V \cdot 10^{-4/-2}$ , or -10V; if  $E_{in} = -4V$ , then

 $E_0 = -0.1V \cdot 10^{-(-4)/-2} = -1mV$ . The figure on the next page shows, in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring expansion of compressed data, linearization of transducers having logarithmic outputs, analog function fitting or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in analog computing, for such functions as compound multiplication and division of terms having differing exponents.

#### LOG-ANTILOG AMPLIFIERS VOL. II, 8-3



Antilog Operator Response Curves, Semilog Scale  $E_0 = E_{REF} \cdot 10^{V_{IN}/-K}$ 

#### LOG-ANTILOG AMPLIFIER PERFORMANCE

Considerable information regarding log- and antilog-amplifier circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK<sup>1</sup>. Several salient points will be covered here, and specifications will be defined.

A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the opamp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.





<sup>1</sup>Nonlinear Circuits Handbook, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, \$5.95; send check or complete MasterCard data to P.O. Box 796, Norwood MA 02062



b) Log/Antilog Amplifier Connected in the Exponential Mode

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

$$I = I_0(\epsilon q V/kT - 1) \cong I_0 \epsilon q V/kT$$

and  $V = (kT/q) \ln (I/I_0)$ 

where I is the collector current,  $I_0$  is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11605° K/V) is the ratio of charge of an electron to Boltzmann's constant, and T is junction temperature kelvin. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of  $I_0$ 's variation with temperature.

$$\Delta V = (kT/q) \ln (I_{in}/I_0) - (kT/q) \ln (I_{ref}/I_0)$$
  
= (kT/q) (ln I<sub>in</sub> - ln I<sub>ref</sub>) + (kT/q) (ln I<sub>0</sub> - ln I<sub>0</sub>)  
= (kT/q) ln (I<sub>in</sub>/I<sub>ref</sub>)

The temperature-dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic  $59mV/decade (kT/q) \ln 10$  at room temperature) to 1V/decade.

Errors are introduced by the offset current of the amplifier, and the offset voltage, for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called log-conformity error, which is manifested as a "nonlinearity" of the input-output plot on semilog paper. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4decade range from 10nA to  $100\mu$ A. A plot of log conformity error for model 759 is shown here.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at what-



Log Conformity Error for Models 759N and 759P

ever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

- Error = Actual output ideal output
  - =  $1V \cdot \log (1.01 \text{ I/I}_{\text{ref}}) 1V \cdot \log (I/I_{\text{ref}})$
  - $= 1V \cdot \log 1.01 = 0.0043V = 4.3mV$

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

#### LOG OUTPUT ERROR (mV)

% ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17.	5.7
3.0	13.	26.	8.6
4.0	17.	34.	11.
5.0	21.	42.	14.
10.0	41.	83.	28.

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1 $\mu$ A tend to be roughly comparable. However, below 1 $\mu$ A, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction – step changes in the direction of increasing current are responded to more quickly than step decreases of current.

#### DEFINITIONS OF SPECIFICATIONS

Log-Conformity Error When the parameters have been adjusted to compensate for offset, scale-factor, and reference errors, the log-conformity error is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Offset Current  $(l_{os})$  is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Offset Voltage ( $E_{os}$ ) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current-logging operations, with high-impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V<sub>in</sub>. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In antilog operation,  $E_{os}$  appears at the output as an essentially constant voltage; its percentage effect on error is greatest for small outputs.

Reference Current ( $I_{ref}$ ) is the effective internally-generated current-source output to which all values of input current are compared.  $I_{ref}$  tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator, or simply by adding a constant bias at the output's destination.

Reference Voltage ( $E_{ref}$ ) is the effective internally generated voltage to which all input voltages are compared. It is related to  $I_{ref}$  by the equation:  $E_{ref} = I_{ref}R_{in}$ , where  $R_{in}$  is the value of input resistance. Typically,  $I_{ref}$  is less stable than  $R_{in}$ ; therefore, practically all the tolerance is due to  $I_{ref}$ .

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.





# 6-Decade, High Accuracy and Wideband Log, Antilog Amplifiers MODELS 755N, 755P, 759N, 759P

#### **FEATURES**

High Accuracy: Models 755N, 755P Wideband: Models 759N, 759P Complete Log/Antilog Amplifiers: External Components Not Required Temperature-Compensated Internal Reference 6 Decades Current Operation: 1nA to 1mA 1% max Error: 1nA to 1mA (755) 20nA to 200 $\mu$ A (759) 4 Decades Voltage Operation: 1mV to 10V 1% max Error: 1mV to 10V (755) 1mV to 2V (759) Small Size: 1.1" × 1.1" × 0.4"





The models 755N, 755P and 759N, 759P are low cost de logarithmic amplifiers offering conformance to ideal log operation over 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). For high accuracy requirements, models 755N, 755P offer maximum nonconformity of 0.5%, from 10nA to 1mA, and 1mV to 1V. For wideband applications, the models 759N, 759P provide fast response (300kHz @ I<sub>SIG</sub> = 10 $\mu$ A to 1mA) and feature maximum nonconformity of 1% from 20nA to 200 $\mu$ A, and 1mV to 2V. The models 755N and 759N compute the log of positive (+) input signals, while the models 755P, 759P compute the log of negative (-) signals.

Designed for ease of use, the models 755N/P and 759N/P are complete, temperature compensated log/antilog amplifiers packaged in a compact epoxy-encapsulated module. External components are not required for logging currents over the complete 6 decade range of 1 $\mu$ A to 1mA. Both the scale factor (K=2, 1, or 2/3 volt/decade) and log/antilog operation are selected by simple pin connection. In addition, both the internal 10 $\mu$ A reference current as well as the offset voltage may be externally adjusted to improve overall accuracy.

The models 755 and 759 are ideally suited as an alternative to in-house designs of OEM applications. Advanced design techniques and superior performance place the 755 and 759 ahead of competitive designs in terms of price, performance and package design.

#### APPLICATIONS

When connected in the current or voltage logging configuration, as shown in Figure 1, the models 755 and 759 may be used in several key applications. A plot of input current versus output voltage is also presented to illustrate the log amplifier's transfer characteristics.







Figure 1. Functional Block Diagram and Transfer Function

# SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	755N/P	····	759N/P	
TRANSFER FUNCTIONS				
Current Mode	د <sub>ن</sub> = -Ki	<sup>og</sup> 10 1955	•	
		NEF T		
Voltage Mode	e <sub>O</sub> = -Kl	og10 ESIG	•	
		REF		
Antilog Mode	e <sub>O</sub> = E <sub>RE</sub>	$\frac{10}{K} \left( \frac{551G}{K} \right)$	•	
TRANSFER FUNCTION PARAMETERS				
Scale Factor (K) Selections <sup>1, 2</sup>	2, 1, 2/3	Volt/Decade	•	
Error $(0.+25^{\circ}C)$	±1% max +0.04%/	Cmar	:	
Reference Voltage (Engr) <sup>2</sup>	0.1V	Cillax	•	
Error @ +25°C	±3% max	د د	±4% max	
vs. Temperature (0 to $+70^{\circ}$ C)	±0.1%/°C	C max	±0.05%/	С
Error @ +25°C	±3% max	¢	•	
vs. Temperature (0 to +70°C)	±0.1%/°	C max	±0.05%/	°C .
MAXIMUM LOG CONFORMITY ERROR				
ISIG RANGE ESIG RANGE	RTI	RTO (K=1)	RTI	RTO (K=1)
1nA to 10nA -	±1%	±4.3mV	±5%	±21mV
10nA to 20nA -	±0.5%	±2.17mV	±2%	±8.64mV
100µA to 200µA 1V to 2V	±1%	±4.3mV	±1%	±4.3mV
200µA to 1mA 2V to 10V	±1%	±4.3mV	±2%	±8.64mV
INPUT SPECIFICATIONS				
Current Signal Range				
Model 755N, 759N	+1nA to	+1mA min	:	
Max Safe Input Current	±10mA n	-11174 11111 12X	•	
Bias Current @ +25°C	(0, +) 10	pA max	(0, +) 20	0pA max
vs. Temperature (0 to +70°C)	x2/+10°C	2	•	
Model 755N 759N	+1mV to	+10V min	•	
Model 755P, 759P	-1mV to	-10V min	•	
Voltage Signal Range, Antilog Mode	ESI	G < 2	•	
Model 755N, 755P	-2 <b>4</b>	~ ~ 2		
Offset Voltage @ +25°C (Adjustable to 0)	±400μV	max	±2mV m	ax
vs. Supply Voltage	±15µV/ ±15µV/%		±10µv7	ι,
FREQUENCY RESPONSE, Sinewave				
Small Signal Bandwidth, -3dB		*		
$I_{SIG} = 1nA$	80Hz		250Hz	
$L_{SIG} = 10\mu A$ $L_{CIG} = 10\mu A$	40kHz		200kHz	
$I_{SIG} = 1mA$	100kHz		200kHz	
Increasing Input Current				
10nA to 100nA	100µs		20µs	
100nA to 1µA	7μs		3µs	
Decreasing Input Current	4μs		2.5µs	
1mA to 1µA	7μs	`	3μs	
1µA to 100nA	30µs		10µs	
ToonA to TonA	400µs	· · · · · · · · ·	80µs	· · ·
Voltage 10Hz to 10kHz	2uV rms		10uV	
Current, 10Hz to 10kHz	2pA rms		10pA m	is
OUTPUT SPECIFICATIONS <sup>3</sup>				
Rated Output				
Voltage	±10V mi	n	•	
Log Mode	+5m 4		•	
Antilog Mode	±4mA		•	
Resistance	0.5Ω		•	
POWER SUPPLY <sup>4</sup>				
Rated Performance	±15Vdc +(12+c	18)Vdc	•	
Current, Quiescent	±7mA		±4mA	
TEMPERATURE RANGE				
Rated Performance	0 to +70	°c	.•	
Operating	-25°C to	+85°C		
CASE SIZE <sup>5</sup> (W = 1 = 11)	-33 C to	F" 0 4"		
CASE SIZE (W X L X H)	1.5 X 1. (38 x 38	5 x 0.4 x 10.4)	. 1.125" x (70 x 70	x 10 4)

NOTES

\*Specifications same as 755N/P.

Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 or 2 (shorted together) for K = 2/3V/decade. Specification is for models 75387, 75391, = for 75587, 75992. No damage due to any pin being shorted to ground. Recommended power supply, model 904, ±15V @ ±50mA output. Case size in inches (mm).

Specifications subject to change without notice.

**OUTLINE DIMENSIONS** 





\*Optional 100k $\Omega$  external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±0.4mV (755) or ±2mV (759) maximum.

#### **MATING SOCKET AC1016**



Plot of Output Voltage vs Input Current for Model 755 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Models 755, 759 Connected in the Log Mode

Figure 2. Transfer Curves

### **Understanding the Log Amplifier Performance**

#### PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

 $e_{OUT} = 1V \log_{10} I_{SIG} / I_{REF}$ 

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current,  $I_{REF}$ , the ratio being dimensionless. For this purpose a temperature compensated reference of  $10\mu A$  is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

#### **REFERRING ERRORS TO INPUT**

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

 $e_{OUT} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01)$  which is equivalent to:

$$e_{OUT} = \underbrace{\frac{1 V \log_{10} (I_{SIG}/I_{REF})}{\text{Initial Value}}}_{\text{Change}} \underbrace{\frac{\pm 1 V \log_{10} (1.01)}{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of  $\pm 4.3$ mV. Conversely, a dc error at the output of  $\pm 4.3$ mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

	ERROR R.T.O.			
ERROR R.T.I.	K = 1	K = 2	K = 2/3	
0.1%	0.43mV	0.86mV	0.28mV	
0.5	2.17	4.34	1.45	
1.0	4.32	8.64	2.88	
3.0	12.84	25.68	8.56	
4.0	17.03	34.06	11.35	
5.0	21.19	42.38	14.13	
10.0	41.39	82.78	27.59	

Table I. Converting Output Error in mV to Input Error in %

#### SOURCES OF ERROR

Log Conformity Error – Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated to taken into account. The best linearity performance for the models 755, 759 are obtained in the 5 decades from 10nA to 1mA. To obtain optimum performance, the input data should be scaled to this range.

Offset Voltage – The offset voltage,  $E_{os}$ , of models 755, 759 is the offset voltage of the internal FET amplifier. This voltage appears as a small de offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

**Bias Current** – The bias current of models 755, 759 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nano-amp region. For this reason, the bias current for model 755 is 10pA, maximum, and 200pA maximum for model 759.

Reference Current –  $I_{REF}$  is the internally generated current source to which all input currents are compared.  $I_{REF}$  tolerance errors appear as a dc offset at the output. The specified value of  $I_{REF}$  is ±3% referred to the input, and, from Table I, corresponds to a dc offset of ±12.84mV for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage –  $E_{REF}$  is the effective internally generated voltage to which all input voltages are compared. It is related to  $I_{REF}$  through the equation:

 $E_{REF} = I_{REF} \times R_{IN}$ , where  $R_{IN}$  is an internal  $10k\Omega$ , precision resistor. Virtually all tolerance in  $E_{REF}$  is due to  $I_{REF}$ . Consequently, variations in  $I_{REF}$  cause a shift in  $E_{REF}$ .

Scale Factor – Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

#### **OPTIONAL EXTERNAL ADJUSTMENTS FOR LOG OPERATION**

Trimming  $E_{OS}$  – The amplifier's offset voltage,  $E_{OS}$ , may be trimmed for improved accuracy with the models 755, 759 connected in its log circuit. To accomplish this, a  $100k\Omega$ , 10 turn pot is connected as shown in Figure 3. The input terminal, Pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{OUT} = -K \log_{10} E_{OS}/E_{REF}$$

To obtain an offset voltage of  $100\mu V$  or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for models 755N, 759N, and -3V to -4V for models 755P, 759P.

For other values of K, the trim pot should be adjusted for an output of  $e_{OUT} = 3 \times K$  to  $4 \times K$  where K is the scale factor.



Figure 3. Trimming E<sub>OS</sub> in Log Mode

Reference Current or Reference Voltage - The reference current or voltage of models 755, 759 may be shifted by injecting a constant current into the unused scale factor terminal (Pin 1 or Pin 2). The current injected will shift the reference one decade, in accordance with the expression:  $I_I = 66\mu A \log A$  $10\mu A/I_{REF}$  (755),  $I_{I} = 330\mu A \log 10\mu A/I_{REF}$  (759), where  $I_I$  = current to be injected and  $I_{REF}$  = the desired reference current.

By changing  $I_{REF}$ , there is a corresponding change in  $E_{REF}$ since,  $E_{REF} = I_{REF} \times R_{IN}$ . An alternate method for rescaling  $E_{REF}$  is to connect an external  $R_{IN}$ , at the  $I_{IN}$  terminal (Pin 5) to supplant the  $10k\Omega$  supplied internally (leaving it unconnected). The expression for  $E_{REF}$  is then,  $E_{REF} = R_{IN} I_{REF}$ . Care must be taken to choose RIN such that (eSIG max)/RIN ≤1mA.

Scale Factor (K) Adjustment - Scale factor may be increased from its nominal value by inserting a series resistor RS between the output terminal, Pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

RANGE OF K	CONNECT SERIES R TO PIN	VALUE OF R <sub>S</sub>	NOTE
2/3V to 1.01V	1	R x (K - 2/3)	use pins 1, 2
1.01V to 2.02V	1	R x (K – 1)	use pin 1
>2.02V	2	R x (K – 2)	use pin 2

 $R = 15k\Omega$  (755);  $3k\Omega$  (759)

Table 2. Resistor Selection Chart for Shifting Scale Factor ANTILOG OPERATION

The models 755 and 759 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

 $e_{OUT} = E_{REF} 10^{-e_{IN}/K}$ [-2≤e<sub>IN</sub>/K≤2] VOL. II, 8-10 LOG-ANTILOG AMPLIFIERS



Figure 4. Functional Block Diagram

Principle of Operation - The antilog element converts the voltage input, appearing at terminal 1, to a current which is proportional to the antilog of the applied voltage. The currentto-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

A more complete expression for the antilog function is:

$$e_{OUT} = E_{REF} 10^{-CIN/K} + E_{OS}$$

The terms K,  $E_{OS}$ , and  $E_{REF}$  are those described previously in the LOG section.

Offset Voltage (EOS) Adjustment - Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to e<sub>OUT</sub>/100. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external  $100\Omega$  resistor, and the jumper from Pin 1 to +15V. For 755P, 759P use the same procedure but connect Pin 1 to -15V.



Figure 5. Trimming EOS in Antilog Mode

Reference Voltage (EREF) Adjustment - In antilog operation, the voltage reference appears as a multiplying constant. EREF adjustment may be accomplished by connecting a resistor, R, from Pin 5 to Pin 3, in place of the internal  $10k\Omega$ . The value of R is determined by:

 $R = E_{REF}$  desired/10<sup>-5</sup> A

Scale Factor (K) Adjustment - The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

 $R_1/R_c = (1/K - 1)$  where K = desired scale factor



Figure 6. Method for Adjusting K<2/3V

# 

# 6-Decade, High Accuracy Log Ratio Amplifiers MODEL 757N, 757P

#### FEATURES

6 Decade Operation – 1nA to 1mA 1/2% Log Conformity – 10nA to 100µA Symmetrical FET Inputs Voltage or Current Operation Temperature Compensated

#### APPLICATIONS

Absorbence Measurements Log Ratios of Voltages or Currents Data Compression Transducer Linearization



#### **GENERAL DESCRIPTION**

Model 757 is a complete, temperature compensated, dc-coupled log ratio amplifier. It is comprised of two input channels for processing signals spanning up to 6 decades in dynamic range (1nA to 1mA). By virtue of its symmetrical FET input stages, the 757 can accommodate this 6 decade signal range at either channel. Log conformity is maintained to within 1/2% over 4 decades of input (10nA to 100 $\mu$ A) and to within 1% over the full input range. Unlike other log ratio designs, model 757 does not restrict the relative magnitude of the two signal inputs to achieve rated performance. Either input can be operated within the specified range regardless of the signal level at the other channel.

The model 757 log-ratio amplifier design makes available both input amplifier summing junctions. As a result, it can directly interface with photo diodes operating in the short-circuit current mode without the need of additional input circuitry.

The excellent performance of model 757 can be further improved by means of external scale factor and output offset adjustments. A significant feature of model 757 not found on competing devices is that, when the offset adjustment is used to establish a fixed bias at the output, the output offset level does not vary as a function of input signal magnitude. On other designs, the sensitivity of output offset to input levels results in output effects resembling log conformity errors.

Model 757 can operate with either current or voltage inputs. Its excellent performance makes it ideally suited for log ratio applications such as blood analysis, chromatography, chemical analysis of liquids and absorbence measurements.

#### CURRENT LOG RATIO

Current log ratio is accomplished by model 757 when two currents,  $I_{SIG}$  and  $I_{REF}$ , are applied directly to the input terminals (see Figure 1). The two log amps process these signals providing



#### Figure 1. Functional Block Diagram of Model 757

voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, higher scale factors may be achieved by connecting external scale factor adjusting resistors. (See section on optional adjustments and trims.)

#### **VOLTAGE LOG RATIO**

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external resistor is attached from the voltage signal to the appropriate input current terminal of the 757. Input currents are then determined by:

$$I_{SIG} = \frac{e_1 - e_{os_1}}{R_1}$$
,  $I_{REF} = \frac{e_2 - e_{os_2}}{R_2}$ 

e<sub>os1</sub> = Input Offset Voltage (I<sub>SIG</sub> Channel) e<sub>os2</sub> = Input Offset Voltage (I<sub>REF</sub> Channel)

# **SPECIFICATIONS**

### (typical @ $+25^{\circ}$ C and V<sub>s</sub> = $\pm 15$ V dc unless otherwise noted)

MODEL		757N/P	
TRANSFER FUNCTION <sup>1</sup>		_	-
Current Mode		eov= -K log10 ISIG	
		IREF	
		$(e_1 - e_{os_1})$ R <sub>2</sub>	
voltage Mode		$e_0 = -K \log_{10} \left( \frac{1}{(e_2 - e_{})} \right) \times \frac{1}{R_1}$	
			•
ACCURACY			
Log Conformity		10.5%	
$I_{SIG}$ , $I_{REF} = 10nA$ to $100\mu A$		±0.5%, max	
$S_{Cale} = InA to ImA$		$\pm 1\%$ , max (+0, -2%) max	
vs. Temperature (0 to $\pm 70^{\circ}$ C)		(+0, -2.%) max $+0.04\%/^{\circ}C$ max	
vis. Temperature (0 to +70 C)		20.04%/ C max	-
INPUT SPECIFICATIONS - Both I	nput Channels		
Signal Range Rated Performa			
Model 757N	iice .	$\pm 1$ nA to $\pm 1$ mA min	
Model 757P		$-\ln A$ to $-\ln A$ min	
Max Safe		±10mA max	
Bias Current, @ +25°C		(0, +) 10pA max	
vs. Temperature (0 to +70°C)		x2/+10°C	
Offset Voltage, @ +25°C		±1mV max	
vs. Temperature (0 to +70°C)			
Isic Channel		$\pm 25 \mu V/^{\circ} C max$	
INFE Channel		$\pm 25 \mu V/^{\circ} C max$	
vs. Supply Voltage		±5µV/%	
EPEQUENCY PEEDONCE C		· · · · · · · · · · · · · · · · · · ·	-
Small Signal Response (-2dP)	n.		
Signal Channel			
Isic = 1nA		250Hz	
$I_{SIG} = 1\mu A$		25kHz	
$I_{SIG} = 100 \mu A$		40kHz	
Reference Channel			
$I_{REF} = 1nA$		100Hz .	
$I_{REF} = 1\mu A$		25kHz	
$l_{\rm REF} = 100 \mu A$		40kHz	
RISE TIME 4	Signal Channel	Beference Channel	-
Increasing Input Current	$(I_{REF} = 10 \mu A)$	$(I_{SIC} = 10\mu A)$	
InA to 10nA	250µs	80µs	
10nA to 100nA	50µs	40µs	
100nA to 1µA	30µs	30µs	
1µA to 100µA	25µs	25µs	
Decreasing Input Current			
100µA to 1µA	25µs	25µs	
1µA to 100nA	30µs	30µs	
100nA to 10nA	100µs	40µs	
10nA to 1nA	600µs	70µs	-
INPUT NOISE			
Voltage (10Hz to 10kHz)		3μV rms	
Current (10Hz to 10kHz)		0.1pA rms	-
OUTPUT SPECIFICATIONS			
Rated Output			
Voltage		±10V min	
Current		±5mA min	
Resistance		0.112	
Uttset Voltage" (K = 1V/Decade	:)	$\pm 10 \text{ mV} \text{ max}$	
vs. Temperature (0 to +70°C)		±0.5mv/ C +5//V/V	
			-
POWER SUPPLY		11 F 1 1	
Rated Performance		113 V dc	
Operating		±(12 (0 18)V dc	
Current, Quiescent	<u>,</u>	TOWV	-
TEMPERATURE RANGE		0	
Rated Performance		0 to +/0 C	
Operating		-23 C 10 +83 C	
Storage		55 G (0 +125 G	-
MECHANICAL		15" x 15" x 0 4"	
Lase Size Weight		21 grams	
		D	-

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



TRANSFER CURVES



Log mode output voltage vs. input current for  $I_{REF} = 10 \mu A.$ 



Figure 2. Scale Factor Adjustment



Figure 3. Output Voltage Offset Adjustments

NOTES <sup>1</sup> For model 757N, K = +1V/Decade and input currents must be positive. For model 757P, K = -IV/Decade and input currents must be negative. (Input currents are defined as positive when flowing into the input terminals, 4 and 5. Refer to TRANSFER CURVES.)

<sup>2</sup> The log conformity error is referred to input (RTI). 1% error RTI is equivalent to 4.3 mV of error at the output for K = 1V/Dec.

<sup>3</sup>Externally adjustable to zero.

\* Recommended power supply: Analog Devices model 904, ±15V @ 50mA.

Specifications subject to change without notice.

### Applying the Log Ratio Amplifier

#### **OPTIONAL ADJUSTMENTS AND TRIMS**

Scale Factor – A one volt per decade scale factor is available when pin 1 is tied to 3 and pin 7 is connected to 9. Higher scale factors are possible by using a potentiometer,  $R_1$ , between pins 1 and 3 and a resistor,  $R_2$ , between pins 7 to 9 as shown in Figure 2. The value of the required resistor is  $(13.2k\Omega)$ (K-1) where K is the desired scale factor. The approximate potentiometer value is also  $(13.2k\Omega)$  (K-1). The scale factor adjustment procedure is as follows:

- 1. Connect the appropriate value of resistor between pins 7 and 9.
- 2. Set  $I_{REF} = 1\mu A$ ,  $I_{SIG} = 10\mu A$ . Measure  $e_0$ .
- Set I<sub>REF</sub> = 1µA, I<sub>SIG</sub> = 100µA. Adjust R<sub>1</sub> until the difference in e<sub>0</sub> corresponding to steps 2 and 3 is K volts.
- 4. Repeat steps 2 and 3 until the change in  $e_0 = K$  volts.

Output Voltage Offset – Output voltage offset must be adjusted after the desired scale factor is established as indicated above. To adjust the offset, inject equal dc input currents into the reference and signal channels. The value of the input currents should approximate the average input current levels expected to be encountered in normal operation. Adjust the potentiometer shown in Figure 3 until the output voltage is zero.

#### LOG CONFORMITY

Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the theoretical value of the log of a ratio and the actual value that appears at the output of the log-ratio module after scale factor errors have been eliminated. Measurement of this error is made after initially zeroing the module at unityratio and adjusting the desired scale factor.

Figure 4 shows the log conformity performance of model 757 over a 6 decade input range. Log conformity for each channel does not vary noticeably as the current is varied in the other channel.



Figure 4. Log Conformity Error for Model 757. Curve is for Either Input Channel with Current Held Constant at 10µA On Other Channel.

#### FREQUENCY CHARACTERISTICS

Figure 5 shows a plot of small signal response (-3dB) as a function of input signal current. The graph demonstrates the frequency response performance for each input channel over the range of 1nA to 1mA, independent of current on the other channel.

As shown in the graph, the reference channel is faster than the signal channel at low input levels. If an application requires higher speed in the input signal channel than in the reference channel, then the channels can be interchanged with a resulting polarity reversal of the output signal

 $\log \frac{I_{SIG}}{I_{REF}} = \log I_{SIG} - \log I_{REF} = -\log \frac{I_{REF}}{I_{SIG}} .$ 



Figure 5. Small Signal Bandwidth (-3dB) vs. Input Signal Level

#### APPLICATIONS

Data Compression – Processing signals with wide dynamic range is a common problem in instrumentation and data transmission. For example, digitizing an analog signal with a range of 10nA to 100 $\mu$ A with 1% accuracy requires a 20 bit A/D converter. (Required resolution = 1/100 x 1/10,000 = 1/10<sup>6</sup>  $\cong$  1/2<sup>20</sup>).

By using the 757 with I<sub>REF</sub> adjusted to 10nA and K set for 5/4 V/decade, the input data can be compressed into a 5 volt output range. For a 1% resolution of any signal, the allowable output error is 4.32mV x K. Log conformity contributes 2.17mV x K (0.5%) over this range. The remaining error with K = 5/4 is 2.69mV and should correspond to less than the LSB of the converter. With a 5 volt output range 2.69mV corresponds just over the LSB of an 11-bit converter. Thus the 757 module can compress the data for use with a 12 bit A/D (such as Analog Devices AD574JD) to obtain the desired 1% resolution.

Absorbence Measurements – Critical properties of materials which are of particular interest in the fields of chemistry, medicine, spectrometry and pollution control are characterized by absorbence. The relationship between absorbence, A, and light intensity, I, is:  $A = \log I_0/I_T$  where  $I_0 =$  intensity of incident light, and  $I_T =$  intensity of transmitted light.

Figure 6 shows the 757 log-ratio module used in such a photometer application. Two inputs represent the intensities of light transmitted through space and through a medium that absorbs light. The absorbence of the medium is given by the formula

$$A = \log \frac{I_{SIGNAL}}{I_{REFERENCE}}$$

where I<sub>SIGNAL</sub> and I<sub>REFERENCE</sub> are the currents representing the light intensities.

The transducers used in this application are photodiodes, which provide a short-circuit current proportional to the intensity of applied light. The lowest value of absorbence is determined by the value of I<sub>REF</sub>, since when I<sub>SIG</sub> = I<sub>REF</sub>, A = 0. The output of the log-ratio module is externally trimmed to 1V/decade and applied to the input of a 3½-digit DPM through the scaling network R1 and R2.

Model 757 was chosen for this design because it makes available both amplifier summing junctions. When the photodiodes are connected to the summing junctions, they are operated in the short-circuit mode, that is, with zero volts across the diodes. Short-circuit loading is necessary, because accuracy of the photodiodes can be degraded several percent when operated with as little as 100mV across the diode junction.



Figure 6. Model 757N Applied to Absorbence Measurements

#### INTERCONNECTION GUIDELINES

Model 757 is a complete log ratio amplifier that requires no additional frequency compensation for proper operation.

Input Capacitance – Model 757 is able to operate with 1000 pF at both input terminals. Therefore, the 757 can be used in applications requiring long cable lengths between the module and the signal transducers.

Input-to-Output Capacitance — When using a log ratio module the user should take care in system configurations to avoid excessive stray capacitance between input and output terminals. Such precautions include avoiding running input and output signal lines close together. If long cable runs are required where inputs and output are closely bundled together, it is advisable to enclose the inputs and/or output in separate, grounded electrostatic shields. By observing simple rules of good circuit layout, problems with oscillations that may result from excessive input-to-output capacitance can easily be avoided. Model 757 can accommodate up to 33pF of input-to-output capacitance without oscillation.

Leakage Resistance – Since model 757 can operate at extremely low input current levels, precautions must be taken to prevent current leakage into the input terminals. Such leakage can cause errors when small input or reference currents are used. This problem may arise on printed circuit layouts if the inputs are run too close to the power supply busses. Providing an etched guard around the input lines, connected to analog signal ground will also reduce unwanted current leakage.

# **Temperature Transducers & Signal Conditioners**

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•New product since publication of 1982–1983 Databook Update

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# Selection Guide Temperature Transducers



### AD590

Linear Current Output: 1µA/K Vol. I Wide Range: -55°C to +150°C 8-15 Probe Compatible Ceramic Sensor Package Two-Terminal Device: Voltage In/Current Out Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M) Excellent Linearity: ±0.3°C Over Full Range (AD590M) Wide Power Supply Range: +4V to +30V Sensor Isolation from Case

### AD592

High Precalibrated Accuracy: 0.5°C max @ 25°C Excellent Linearity: 0.2°C max (0 to +70°C) Wide Operating Temperature Range: -25°C to +105°C

Single Supply Operation: +4V to +30V Excellent Repeatability and Stability

High Level Output Signal: 1µA/°C

Two Terminal Monolithic IC: Temperature In/Current Out

Minimal Self-Heating Errors Low Cost Plastic Package

### AC2626

Linear Current Output: 1µA/K Wide Range: -55°C to + 150°C Laser Trimmed Sensor (AD590) to ±0.5°C Calibration Accuracy (AC2626M) Excellent Linearity: ±0.3°C Over Full Range (AC2626M) 6 Inch or 4 Inch Standard, Stainless Steel Sheath 3/16 Inch in Outside Diameter 3 Feet Teflon Coated Lead Wire Wide Power Supply Range +4V to +30V Fast Response: 2 Seconds (In Stirred Water) Sensor Isolated from Sheath Vol. I 8-23

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# **Signal Conditioners**

# **Temperature Transducer Signal Conditioners**





### AD594/AD595

Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples Can Be Used with Type T Thermocouple Inputs Low Impedance Voltage Output: 10mV/°C Built-In Ice Point Compensation Wide Power Supply Range: +5V to ±15V Low Power: <1mW typical Thermocouple Failure Alarm Laser Wafer Trimmed to 1°C Calibration Accuracy Set-Point Mode Operation Self-Contained Celsius Thermometer Operation High Impedance Differential Input

### AD596

Low Power: ±1mW typ

Monolithic Temperature Set-Point Controller	Vol. I
Built-In Ice Point Compensation for Type J	8-39
Thermocouples	
Self-Contained Temperature Sensor for Stand-Alone Operation	
Programmable Dead Band	
Wide Power Supply Range +5V to ±15V	
4°C Calibration Accuracy	

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# **Selection Guide Signal Conditioners**

### **Voltage-to-Current Converters**







#### 2B20

Complete, No External Components Needed Small Size: 1.1"×1.1"×0.4" Module Input: 0 to +10V; Output: 4 to 20mA Low Drift: 0.005%/°C max; Nonlinearity: 0.005% max (2B20B)

Wide Temperature Range: -25°C to +85°C

Single Supply: +10V to +32V

Meets ISA Std. 50.1 for Type 3, Class L and U, **Nonisolated Current Loop Transmitters** 

#### 2B22

Wide Input Range: 0 to +1V to 0 to +10V Standard Output Range: 4 to 20mA High CMV Input/Output Isolation: 1500V dc Continuous

Low Nonlinearity: 0.05% max, 2B22L

Low Span Drift: 0.005%/°C max, 2B22L

Single Supply: +14V to +32V

Meets IEEE Std. 472: Transient Protection (SWC)

Meets ISA Std. 50.1: Isolated Current Loop Transmitters

### 2B23

Wide Input Range, Resistor Programmable Pin Programmable Output: 4 to 20mA or 0 to 20mA High CMV Input/Output Isolation: ±1500V pk Continuous

Low Nonlinearity: ±0.05% max (2B23K) Low Span Drift: ±0.005%/°C max (2B23K) Single Supply Operation: +14V to +28V Small Size: 1.8" × 2.4" × 0.6"

Meets IEEE Std. 472: Transient Protection (SWC) Meets ISA ST. 50.1: Isolated Current Loop

Transmitters

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### Strain Gage/RTD Conditioners







### 2B30

- **Complete Signal Conditioning Function** Low Drift: 0.5µV/°C max ("L"); Low Noise: 1µV p-p max Wide Gain Range: 1 to 2000V/V Low Nonlinearity: 0.0025% max ("L") High CMR: 140dB min (60Hz, G = 1000V/V) Input Protected to 130V rms Adjustable Low Pass Filter: 60dB/Decade Roll-Off
- (from 2Hz)

#### 2B31

**Complete Signal Conditioning Function** Low Drift: 0.5µV/°C max ("L"); Low Noise: 1µV p-p max Wide Gain Range: 1 to 2000V/V

Low Nonlinearity: 0.0025% max ("L")

High CMR: 140dB min (60Hz, G = 1000V/V)

Input Protected to 130V rms

Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)

Programmable Transducer Excitation: Voltage (4V to 15V.@ 100mA) or Current (100µA to 10mA)

#### 2B34

Low Input Offset Drift: ±1.0µV/°C Vol. II Low Gain Drift: ±25ppm/°C 9-35 Low Nonlinearity: ±0.01% max (±0.005% typ) Differential Input Protection: ±130V rms Channel Multiplexing: 3000 chan/sec Scanning Speed Solid State Reliability Internal RTD Excitation/Lead Wire Compensation

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# Selection Guide Signal Conditioners

# **Isolated Transducer Signal Conditioners**







### 2B50

Accepts J, K, T, E, R, S or B Thermocouple Types Internally Provided Cold Junction Compensation High CMV Isolation:  $\pm 1500V \text{ pk}$ High CMR: 160dB min @ 60Hz Low Drift:  $\pm 1\mu V/^{\circ}C \max (2850B)$ High Linearity:  $\pm 0.01\% \max (2850B)$ Input Protection and Filtering Screw Terminal Input Connections

#### 2B54

Low Cost	Vol. U
Wide Input Span Range: ±5mV to ±100mV	9-47
12-Bit Systems Compatible	
High CMV Isolation: ±1000V dc; CMR = 156dB min @ 60Hz	
Low Input Offset Voltage Drift: ±1µV/°C max (2B54B)	
Low Gain Drift: ±25ppm/°C max (2B54B)	
Low Nonlinearity: ±0.02% max (±0.012% typ)	
Normal Mode Input Protection (130V rms) and Filtering	
Channel Multiplexing: 400 chan/sec Scanning Speed	
Solid State Reliability	
2B56	

Universal Thermocouple Compensation	Vol. II
Internally Provided: Types J, K, T	9-53
User Configurable: Types E, R, S, B	
Digitally Programmable	
High Accuracy: ±0.8°C max over +5°C to +45°C	
High Ambient Rejection: 50 to 1 min	
Low Cost	
Small Size: 1.5" × 2" × 0.4"	

### 2B55

Low CostVol. IIWide Input Span Range:  $\pm 50 \text{mV}$  to  $\pm 5 \text{V}$ 9-4712-Bit Systems Compatible9-47High CMV Isolation:  $\pm 1000 \text{V}$  dc; CMR = 145dB min@@ 60Hz60HzLow Input Offset Voltage Drift:  $\pm 5 \mu \text{V/°C}$  maxLow Gain Drift:  $\pm 25 \text{ppm/°C}$  maxLow Nonlinearity:  $\pm 0.02\%$  max (G = 1 to 100)Normal Mode Input Protection (130V rms) and<br/>FilteringChannel Multiplexing: 400 chan/sec Scanning SpeedSolid State Reliability

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### 2B24

Self-Powered Wide Input Range: 1-50mA (2B24B) High CMV Isolation: ±1500V pk; CMR: 120dB High Accuracy: ±0.1% RFI/EMI Immunity Low Cost Page Vol. II 9–27

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### 2B52

Accepts Type J, K or T Thermocouple Inputs Compatible with Standard 4-20mA Loops High Accuracy: ±0.1% High CMV Isolation: 600V rms; CMR = 160dB High Noise Rejection and RFI Immunity Internal Cold Junction Compensation Open Thermocouple Detection Millivolt Signal Transmission Low Cost FM Approved

#### 2B53

Accepts Type J, K or T Thermocouple Inputs Compatible with Standard 4-20mA Loops High Accuracy: ±0.1% High Noise Rejection and RFI Immunity Internal Cold Junction Compensation Open Thermocouple Detection Millivolt Signal Transmission Low Cost Vol. II 9-45

# Selection Guide Signal Conditioners

# **Two-Wire Transmitters**







### 2B57

Low Cost Compatible with Standard 4-20mA Loops Low Span Drift: ±0.005%/°C max Low Nonlinearity: ±0.05% max RFI Immunity Small Size: 1.5" × 1.5" × 0.4" Page Vol. 11 9-57

2B58

Platinum RTD Input Linearized 4-20mA Output High Accuracy: ±0.1% Low Drift: ±0.01°C/°C max RFI Immunity Low Cost FM Approved

#### 2B59

Low Cost Standard RTD Input Linearized 4-20mA Output High Accuracy: ±0.1% Small Size Ease of Installation Vol. II 9-61

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#### VOL. II, 9-8 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS



# **3B Series I/O Subsystems**

Input Module Selection

Input Type/Span	Voltage Output	Current Output	Nonisolated Modules	Isolated Modules
dc, $\pm 10$ mV, $\pm 50$ mV, $\pm 100$ mV	$\pm 10V$	4-20mA/0-20mA	3B10	3B30
dc, $\pm 1V$ , $\pm 5V$	±10V	4-20mA/0-20mA	3B10	3B31
dc, ± 10V	$\pm 10V$	4-20mA/0-20mA	3B11	3B31
dc, 4-20mA, 0-20mA	0 to +10V	4-20mA/0-20mA	3B12	3B32
Thermocouple Types J, K, T, E, R, S, B	0 to + 10V	4-20mA/0-20mA		3B37
100 $\Omega$ Platinum RTD, 2-, 3-, 4-Wire $\alpha = 0.00385$ (linearized)	0 to + 10V	4-20mA/0-20mA	3B14	3B34
100 $\Omega$ Platinum RTD, Kelvin 4-Wire $\alpha = 0.00385$ (linearized)	0 to + 10V	4-20mA/0-20mA	3B15	
Strain Gage ± 30mV, ± 100mV	±10V	4-20mA/0-20mA	3B16	
AD590/AD592/AC2626 Solid State Temperature Transducer	0 to + 10V	4-20mA/0-20mA	3B13	
Wideband Strain Gage	$\pm 10V$	4-20mA/0-20mA	3B18	
Wideband mV, V	$\pm 10V$	4-20mA/0-20mA		3B40/1
ACInput	0 to +10V	4-20mA/0-20mA		3B42/3/4
Frequency Input	0 to +10V	4-20mA/0-20mA	,	3B45/6

**Output Module Selection** 

Input Type/Span	Current Output	Modules	Isolated Modules
$0 \text{ to } + 10 \text{V}, \pm 10 \text{V}$	4-20mA/0-20mA	3B19	3B39

# Selection Guide Signal Conditioners

### **3B Series I/O Subsystems**





## 4B Series Alarm Limit Subsystem



### Input Modules

Wide Variety of Sensor Inputs: Thermocouples, RTD's, Strain Gages, AD590/AD592/AC2626 Dual High Level Outputs Voltage: 0 to +10V or ±10V Current: 4-20mA/0-20mA Mix and Match Input Capability Sensor Signals, mV, V, 4-20mA, 0-20mA High Accuracy: ±0.1% High Noise Rejection and RFI/EMI Immunity Reliable Transformer Isolation: ±1500V CMV Meets IEEE-STD 472: Transient Protection (SWC) Input Protection: 130V or 220V rms Continuous

### **Output Modules**

High Level Voltage Input: (0 to +10V,  $\pm 10V$ ) Process Current Output: (4-20mA/0-20mA) High Accuracy:  $\pm 0.1\%$ Reliable Transformer Isolation:  $\pm 1500V$  CMV.

CMR = 90dB

Meets IEEE-STD 472: Transient Protection (SWC) Output Protection: 130V or 220V rms Continuous

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### **Features/Benefits**

Low Cost, Completely Integrated 12-Channel Modular Alarm Limit Subsystem Selection of Alarm Limit Modules Rugged Industrial Chassis, Rack or Surface Mounted **On-Board Power Supplies Available** Alarm Modules Accept High Level Voltage and Process Current Inputs **Complete Alarm Function per Module** High Accuracy of ±0.1% Two Set Points, Adjustable Over 100% Span Dead Band Adjustment per Set Point, Adjustable Over 0.5%-10.0% Span Alarm Types are Configurable for HI or LO Operation Two Relay Outputs **Display Indicates Set Points and Process Variable** LED per Set Point Provides Local Alarm Indication Input Protection High RFI/EMI Immunity Specifications Valid Over the 0 to +70°C **Temperature Range** Easy to Install Calibrate and Service

VOL. II, 9-10 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS
# **Orientation** Temperature Transducers & Signal Conditioners

In this section are listed a wide variety of cost-effective analogto-analog signal conditioners for laboratory and industrial applications, and a set of linear high-output-level semiconductor temperature transducers, manufactured by Analog Devices.

The signal conditioners are intended to provide a variety of system interfaces for signals originating from input transducers or destined for output transducers.

They accept low or high-level signal inputs from millivolts to volts, low- or high-level current inputs from microamperes to 4-to-20mA loops,' and direct inputs from transducers, such as strain gages and other bridge devices, RTDs, thermocouples, thermistors, and semiconductor temperature sensors. One of these modules (2B35) is a triple-output power supply that accepts ac line voltage and provides voltage and programmable current excitation for transducers and signal conditioners.

Outputs from these devices include 0-to-20mA, 4-to-20mA and 10-to-50mA transmitter loop current, and normalized voltage at  $\pm 5V$  or  $\pm 10V$  levels for inputs to analog and digital data-acquisition systems. Most of the devices that operate with current loops derive their power directly from the loop supply.

The many useful functions of these devices include—and often combine—voltage-to-current conversion; input-to-output and channel-to-channel isolation; current-to-current conversion; amplification, offsetting, and filtering; transducer voltage and current excitation; all-solid-state isolation, gain, filtering, protection, and multiplexing; thermocouple open-input detection and cold-junction compensation; RTD linearizing.<sup>1</sup>

#### **SELECTION GUIDE**

These many functions are sorted out and arranged for easy access in the Selection Guide so that a device having the desired combination of performance characteristics can be readily found. Device types are classified in broad categories, and the key attributes of each device are listed next to a functional block diagram. A quick glance at the Selection Guide allows you to choose the product(s) with your desired functionality. At this point, you may turn to the appropriate data sheet(s) to compare performance, starting the process of considering the specific device(s) for your application.

#### THAT'S NOT ALL

Besides the signal conditioners in this section, this databook has technical data on many other products that perform signalconditioning functions. They are to be found in these sections of this Volume:

Isolation Amplifiers.

*D/A Converters* (DACs having 4-to-20mA output current, isolation, and other useful features).

Data-Acquisition Subsystems (including programmable-gain amplifiers, differential inputs, etc.).

Digital Panel Instruments (with isolation, low-level signalhandling capability, digital readout and BCD system output: scanning multi-channel voltmeters, intelligent thermocouple thermometers, low-cost digital thermometers, etc.).

Microcomputer Interface Boards (with input multiplexing and programmable gain, 4-to-20mA output options, etc.).

µMAC-4000 Single-Board Intelligent Measurement-and-Control Subsystems (with direct sensor inputs, isolation, signal conditioning, microcomputer-based linearization, ASCII 20mA/RS-232C communications, on-board power supply, and digital I/O).

MACSYM Complete BASIC-Programmable Minicomputer-Based Measurement-And-Control SYsteMs (with a wide selection of input signal conditioning cards and direct connection to sensor field wiring).

<sup>1</sup> Many of these issues are discussed in *Transducer Interfacing Handbook, a guide to analog signal conditioning, published by Analog Devices, Inc., 1980, \$14.50, available from P.O. Box 796, Norwood MA 02062.* 

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### **General Purpose Temperature Probe**

#### **FEATURES**

Linear Current Output: 1µA/K Wide Range: -55°C to +150°C Laser Trimmed Sensor (AD590) to ±1.0°C Calibration Accuracy (AC2626L) Excellent Linearity: ±0.4°C Over Full Range (AC2626L) 6 Inch or 4 Inch Standard, Stainless Steel Sheath 3/16 Inch in Outside Diameter 3 Feet Teflon Coated Lead Wire Wide Power Supply Range +4V to +30V Low Cost Fast Response: 2 Seconds (In Stirred Water) Sensor Isolated From Sheath



AC2626

#### PRODUCT DESCRIPTION

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm or 4 inch (101.6mm) lengths. The probe is available in linearity grades of  $0.4^{\circ}$ C,  $0.8^{\circ}$ C or  $1.5^{\circ}$ C.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AC2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

#### **PRODUCT HIGHLIGHTS**

The AC2626 is based on the AD590 temperature transducer, a two terminal integrated circuit which produces an output current linearly proportional to absolute temperature.

Costly linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AC2626.

Due to the high impedance current output of the AD590, the AC2626 is particularly useful in remote sensing applications, because of its insensitivity to voltage drops over lines. The output characteristics also make the AC2626 easy to multiplex.

In addition to temperature measurement, applications include temperature compensation, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry.

#### DIRECT INTERFACE PRODUCTS

For display and/or control applications, two companion products are available. The AD2038, 6 channel digital thermometer, and the AD2040, low cost temperature indicator, were designed to be used in conjunction with the AC2626.

- The AD2038 is a low cost, ac line powered 6 channel digital scanning thermometer designed to interface to printers, computers, serial data transmitters, etc., for display, control, logging or transmission of multi-point temperature data. Channel selection is made via three methods: manual, using the switch provided on the front; auto/scan, where the AD2038 cycling on an internal clock can continually scan the six input channels or external selection, where control inputs provided on the rear connector enable channel selection via external BCD coding.
- 2. The AD2040 is a low cost, 3 digit temperature indicator. An internal precision voltage reference, resistor network and span and zero adjusts allow the AD2040 to read out directly in °C, °F, K or R. User selectable readout as well as all other connections, i.e., +5V dc power and AC2626 interface are all made via the terminal block on the rear.

#### APPLICATION HINTS

- 1. Under all operating conditions, a minimum 4V dc must be present across the AC2626.
- Use of twisted pair wiring is recommended, particularly for remote applications or in high noise environments. Shielded wire is desirable in severe noise environments.
- 3. For the lowest cost, the J and K grades are recommended. Where probe interchangeability is desired, grade L is recommended.

### **SPECIFICATIONS**

(typical @ +25°C and +5V unless otherwise specified)

MODEL	AC2626J	AC2626K	AC2626L
ABSOLUTE MAXIMUM RATINGS <sup>1</sup>			
Forward Voltage (Vs)	+44V	•	•
Reverse Voltage (Vs)	-20V	•	•
Breakdown Voltage (Case to Leads)	±200V	•	•
Rated Performance Temp. Range	-55°C to +150°C	•	•
Storage Temperature Range	-60°C to +160°C	•	•
POWER SUPPLY			
Operating Voltage Range	+4V to +30V	•	•
OUTPUT			•
Nominal Current Output @ +25°C			
(298.2°K)	298.2µA	•	•
Nominal Temperature Coefficient	1µA/°C	•	•
Calibration Error @ +25°C	±5.0°C max	±2.5°C max	±1.0°C max
Absolute Error (over rated performance			
temperature range)			
Without External Calibration			
Adjustment	±10.0°C max	±5.5°C max	±3.0°C max
With +25°C Calibration Error			
Set to Zero	±3.0°C max	±2.0°C max	±1.6°C max
Nonlinearity	±1.5°C max	±0.8°C max	±0.4°C max
Repeatability <sup>2</sup>	0.1°C	•	•
Long Term Drift <sup>3</sup>	0.1°C max/month	•	•
Time Constant <sup>4</sup> (in stirred water)	2 sec.	•	•
Current Noise	40pA√Hz	•	•
Power Supply Rejection			
+4V≤Vs≤+5V	0.5µA/V	•	•
+5V≤V <sub>S</sub> ≤+15V	0.2µA/V	•	*
+15V≤V5≤+30V	0.1µA/V	•	•
Electrical Turn-On Time	20µs	•	•
+ Lead Color	yellow	orange	blue
ORDERING GUIDE			
AC2626			

GRADE ENTER LENGTH ENTER AC2629 BRASS в ENTER **TYPE 316** SS STAINLESS

NOTES

<sup>1</sup> Maximum safe recommended pressure: 7500psi (5.17 × 10<sup>4</sup> Kpa).
<sup>2</sup> Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed,

not tested.

<sup>3</sup>Conditions: constant +5V, constant +125°C; guaranteed, not tested.

\*The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

\*Specifications same as AC2626J. Specifications subject to change without notice.

#### CALIBRATION



For most applications, a single point calibration is sufficient. With the probe at a known temperature, adjust RT so that Vo corresponds to the known temperature.

If more detailed information is desired, see the AD590 data sheet and application note.



Dimensions shown in inches and (mm).



See Note 1 ±0.06(1.58) AC2629

STAINLESS STEEL TYPE 316 COMPRESSION FITTING (See Note 3)

3/16 (4.76)

t



NOTE 1 Probes are available in 4-inch or 6-inch lengths. NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue. NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

.

### **ANALOG** DEVICES

# High Performance, 4-20mA Output Voltage-to-Current Converter



#### FEATURES

Complete, No External Components Needed Small Size: 1.1" x 1.1" x 0.4" Module Input: 0 to +10V; Output: 4 to 20mA Low Drift: 0.005%/°C max; Nonlinearity: 0.005% max (2B20B) Wide Temperature Range: -25°C to +85°C Single Supply: +10V to +32V Meets ISA Std 50.1 for Type 3, Class L and U, Nonisolated Current Loop Transmitters Economical APPLICATIONS Industrial Instrumentation and Control Systems D/A Converter – Current Loop Interface Analog Transmitters and Controllers

Remote Data Acquisition Systems

GENERAL DESCRIPTION

Model 2B20 is a complete, modular voltage-to-current converter providing the user with a convenient way to produce a current output signal which is proportional to the voltage input. The nominal input voltage range is 0 to +10V. The output current range is 4 to 20mA into a grounded load.

Featuring low drift  $(0.005\%)^{\circ}$ C max, 2B20B) over the -25°C to +85°C temperature range and single supply operation (+10V to +32V), model 2B20 is available in two accuracy grades. The 2B20B offers precision performance with nonlinearity error of 0.005% (max) and guaranteed low offset error of ±0.1% max and span error of ±0.2% max, without external trims. The 2B20A is an economical solution for applications with lesser accuracy requirements, featuring nonlinearity error of 0.025% (max), offset error of ±0.4% (max), span error of ±0.6% (max), and span stability of 0.01%/°C max.

The 2B20 is contained in a small  $(1.1'' \times 1.1'' \times 0.4'')$ , rugged, epoxy encapsulated package. For maximum versatility, two signal input (V<sub>IN1</sub> and V<sub>IN2</sub>) and two reference input (REF<sub>IN1</sub> and REF<sub>IN2</sub>) terminals are provided. Utilizing terminals V<sub>IN1</sub> and REF<sub>IN1</sub> eliminates the need for any external components, since offset and span are internally calibrated. If higher accuracy (up to ±0.01%) is required, inputs V<sub>IN2</sub> and REF<sub>IN2</sub> with series trim potentiometers may be utilized.

#### APPLICATIONS

Model 2B20 has been designed for applications in process control and monitoring systems to transmit information between subsystems or separated system elements. The 2B20 can serve as a transmission link between such elements of process con-



trol system as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners.

In a typical application, model 2B20 may act as an interface between the D/A converter output of a microcomputer based system and a process control device such as a variable position valve. Another typical application of the 2B20 may be as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-topneumatic transducers.

#### DESIGN FEATURES AND USER BENEFITS

Process Signal Compatibility: To provide output signal compatibility, the 2B20 meets the requirements of the Instrument Society of America Standard S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 3, Class L and U, nonisolated current loop transmitters.

**External Reference Use:** For increased flexibility, when ratiometric operation is desired, the 2B20 offers a capability of connecting an external reference (i.e., from multiplying D/A converter) to the REF<sub>IN2</sub> terminal.

Wide Power Supply Range: A wide power supply range (+10V to +32V dc) allows for operation with either a +12V battery, a +15V powered data acquisition system, or a +24V powered process control instrumentation.

### **SPECIFICATIONS**

(t	ypical	@ +25	°C and	$V_{S} =$	+15V.	unless	otherwise	noted
• •	,			-0				

Model	2B20A	2B20B
INPUT SPECIFICATIONS		
Voltage Signal Range	0 to +10V	*
Input Impedance	10kΩ	*
OUTPUT SPECIFICATIONS		
Current Output Range <sup>1</sup>	4 to 20mA	*
Load Resistance Range <sup>2</sup>		
$V_S = +12V$	0 to 350Ω max	•
$V_{S} = +15V$	0 to 500 $\Omega$ max	*
$V_{S} = +24V$	0 to 950Ω max	•
NONLINEARITY (% of Span)	±0.025% max	±0.005% max
ACCURACY <sup>3</sup>		
Warm-Up Time to Rated Specs	1 minute	•
Total Output Error @ +25°C <sup>3,4</sup>	· ·	
Offset $(V_{IN} = 0 \text{ volts})$	±0.4% max	±0.1% max
Span ( $V_{IN} = +10$ volts)	±0.6% max	±0.2% max
vs. Temperature (-25°C to +85°C)		
Offset (V <sub>IN</sub> =0 volts)	±0.01%/°C max	±0.005%/°C max
Span (V <sub>IN</sub> = +10 volts)	±0.01%/°C max	±0.005%/°C max
DYNAMIC RESPONSE		
Settling Time – to 0.1% of F.S.		
for 10V Step	25µs	•
Slew Rate	2.5mA/µs	*
REFERENCE INPUT <sup>5</sup>		
Voltage	+2.5V dc	•
Input Impedance	10kΩ	•
POWER SUPPLY		
Voltage, Rated Performance	+15V de	•
Voltage, Operating	+10V to +32V dc max	•
Supply Change Effect (% of Span) <sup>6</sup>		
on Offset	±0.005%/V	•
on Span	±0.005%/V	
Supply Current	6mA + I <sub>LOAD</sub>	•
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	•
Storage	-55°C to +125°C	•
CASE SIZE	1.125" × 1.125"	
	. × 0.4″	•

NOTES

\*Specifications same as 2B20A.

<sup>1</sup> Current output sourced into a grounded load over a supply voltage range of +10V to +32V.

<sup>2</sup> See Figure 1 for the maximum load resistance value over the power supply range.

<sup>3</sup>Accuracy is guaranteed with no external trim adjustments when REF<sub>IN</sub> is connected to REF<sub>OUT</sub>. <sup>4</sup>All accuracy is specified as % of output span where output span is 16mA (±0.1%=±0.016mA output error).

<sup>8</sup>Reference input is normally connected to the reference output (+2.5V dc).

<sup>6</sup> Optional trim pots may be used for calibration at each supply voltage.

Specifications subject to change without notice.

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



**MATING SOCKET: AC1016** 

#### LOAD RESISTANCE RANGE

The load resistance is the sum of the resistances of all connected receivers and the connection lines. The 2B20 operating load resistance is power supply dependent and will decrease by 50 ohms for each 1 volt reduction in the power supply. Similarly, it will increase by 50 ohms per volt increase in the power supply, but must not exceed the safe voltage capability of the unit.



Figure 1. Maximum Load Resistance vs. Power Supply

### Applying the 2B20

#### PRINCIPLE OF OPERATION

The design of the 2B20 is comprised of high performance op amps, precision resistors and a high stability voltage reference to develop biasing and output drive capability. The 2B20 is designed to operate from a single positive power supply over a wide range of +10V to +32V dc and accepts a single ended, 0 to +10V voltage input. The internal reference has nominal output voltage of +2.5V (REF<sub>OUT</sub>) and is used to develop 4mA output current for a zero volts input when REF<sub>IN</sub> is connected to REF<sub>OUT</sub>.

The output stage of the 2B20 utilizes a sensing resistor in the feedback loop, so the output current is linearly related to the voltage input and independent of the load resistance. There is no minimum resistance for the loads driven by the 2B20; it can drive even a short circuit with no damage to the unit. The maximum resistance of the load as seen by the unit (resistance of the load plus the resistance of the connecting wire) is limited. The maximum external loop resistance,  $R_{L_1}$  is given by:

$$R_L(\Omega) \max = \left(\frac{+V_S - 5V}{20mA}\right)$$

Figure 1 shows the operating region of the 2B20. The load must be returned to power supply common. The voltage appearing between  $I_{OUT}$  (pin 5) and COM (pin 2) should not exceed  $V_{max} = +V_S - 5V$ . Exceeding this value (up to +32V dc) will not damage the unit, but it will result in a loss of linearity.

The basic connections of the 2B20 are shown in Figure 2.



Figure 2. Basic Connections Diagram

#### OPTIONAL CALIBRATION AND TRIM PROCEDURE

Model 2B20's factory trimmed offset error is  $\pm 0.1\%$  max and span error is  $\pm 0.2\%$  max (2B20B). In most applications, further trimming will not be required. If it is necessary to obtain calibrated accuracy of up to  $\pm 0.01\%$ , or, if a high signal source resistance (with respect to  $10k\Omega$ ) introduces calibration error, inputs V<sub>IN2</sub> and REF<sub>IN2</sub> and optional trim pots should be used with V<sub>IN1</sub> and REF<sub>IN1</sub> open. To perform external trims, connect 500 $\Omega$  potentiometers in series with V<sub>IN2</sub> (span trim) and REF<sub>IN2</sub> (offset trim) as shown in Figure 3. Adjust span pot, monitoring voltage drop across R<sub>LOAD</sub>, to obtain an output voltage of 5.000V (I<sub>OUT</sub> = 20mA) for a +10V input. Next, with 0 volts input, adjust offset pot to obtain 1.000V output (I<sub>OUT</sub> = 4mA). Check both offset and span and retrim if necessary after each adjustment.



Figure 3. Model 2B20 Connections Using Optional Offset and Span Trims

**CONNECTING THE 2B20 FOR 0 TO 10mA OUTPUT** 

The 2B20 may be utilized in applications requiring 0 to 10mA current output for a 0 to 10V input voltage range. To obtain 0mA output for 0V input, REF<sub>IN1</sub> (pin 6) and REF<sub>IN2</sub> (pin 8) terminals should be left open. A typical output current error for a zero volts input (without trimming) is 0.1mA. The 2B20 span calibration may be adjusted by a 1k $\Omega$  potentiometer in series with the V<sub>IN2</sub> input. Basic connections of the 2B20 used to obtain a 0 to 10mA output are shown in Figure 4a.



### Figure 4a. Model 2B20 Connected for 0 to 10mA Output Range

CONNECTING THE 2B20 FOR 0 TO 20mA OUTPUT The 2B20 may also be configured for use in applications requiring 0 to 20mA output for a 0 to +10 volt input range. REF<sub>IN1</sub> (pin 6) is left open, and REF<sub>IN2</sub> (pin 8) is connected to V<sub>IN2</sub> (pin 1) through a 32.4k $\Omega$  resistor. The typical output current error for 0V input (without trimming) is 0.1mA. The 2B20 span may be adjusted by a 2k $\Omega$  potentiometer in series with the V<sub>IN2</sub> input to provide 9% FSR adjustment range. Basic connections for 0-20mA operation are shown in Figure 4b.



Figure 4b. Model 2B20 Connected for 0 to 20mA Output Range

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#### **OUTPUT PROTECTION**

In many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 5 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.



Figure 5. Output Protection Circuitry Connections

#### APPLICATIONS

Interfacing Voltage Output D/A Converters: The 2B20 is well suited in applications requiring 4 to 20mA output from D/A converters. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 6. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B20 (or the AD DAC80). First, a digital input code of all ones is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all 0s is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA -1LSB = 19.9961mA.



Figure 6. AD DAC80 – 4 to 20mA Current Loop Interface

Interfacing Current Output D/A Converters: To interface current output D/A converters, such as the AD562, a circuit configuration illustrated in Figure 7 should be used. Since the AD562 is designed to operate with an external +10V reference, the same external reference may be utilized by the 2B20 for ratiometric operation. The output of the AD562 is used to drive the summing junction of an operational amplifier to produce an output voltage. Using the internal feedback resistor of the AD562 provides a 0 to +10V output voltage range suitable to drive the 2B20.



Figure 7. 12-Bit – 4 to 20mA Current Loop Interface

Microcomputer – Current Loop Interface: Figure 8 shows a typical application of the 2B20 in a multichannel microcomputer analog output system. When a microcomputer is to control a final control element, such as a valve positioner, servomechanism or motor, an analog output board with 4 to 20MA outputs is often necessary. The output boards typically have from one to eight channels, each with its own D/A converter. The 2B20, in a compact package, allows for an easy installation without any additional components and offers a 12-bit system compatible performance.



Figure 8. Microcomputer Analog Output Subsystem

Pressure Control System: In Figure 9, model 2B20 is used in a proportional pressure control system. The 3-15psi working pressure of a system is monitored with a pressure transducer interfaced by the model 2B31 signal conditioner. The high level voltage output of the 2B31 is converted to a 4 to 20mA to provide signal to the limit alarm and proportional control circuitry. A current-to-position converter controlling a motorized valve completes the pressure-control loop.



Figure 9. Proportional Pressure Control System

Isolated 4 to 20mA Output: For applications requiring up to ±1500V dc input to output isolation, consider using Analog Devices' model 2B22 isolated voltage-to-current converter.



### High Performance, Isolated Voltage-to-Current Converter

MODEL 2B22

#### FEATURES

Wide Input Range: 0 to +1V to 0 to +10V Standard Output Range: 4 to 20mA High CMV Input/Output Isolation: 1500V dc Continuous Low Nonlinearity: 0.05% max, 2B22L Low Span Drift: 0.005%/°C max, 2B22L Single Supply: +14V to +32V Meets IEEE Std 472: Transient Protection (SWC) Meets ISA Std 50.1: Isolated Current Loop Transmitters

#### APPLICATIONS

Industrial Instrumentation and Process Control Ground Loop Elimination High Voltage Transient Protection D/A Converter – Current Loop Interface Analog Transmitters and Controllers Remote Data Acquisition Systems

#### **GENERAL DESCRIPTION**

Model 2B22 is a high performance, compact voltage-to-current converter offering 1500V dc input to output isolation in interfacing standard process signals. The input stage of the model 2B22 is single resistor programmable to accept voltage ranges from 0 to +1V to 0 to +10V. The isolated output current range is 4 to 20mA, and the 2B22 can be operated with 0 to 1000 $\Omega$  grounded or floating loads.

Using modulation techniques with transformer isolation for reliable performance, the 2B22 is available in three accuracy selections offering guaranteed nonlinearity error (2B22L:  $\pm 0.05\%$  max, 2B22K:  $\pm 0.1\%$  max, and 2B22J:  $\pm 0.2\%$  max) and guaranteed low span drift:  $\pm 0.005\%/^{\circ}$ C max,  $\pm 0.01\%/^{\circ}$ C max, and  $\pm 0.015\%/^{\circ}$ C max, respectively. The internally trimmed span and offset errors are  $\pm 0.1\%$  max for the 2B22L and  $\pm 0.25\%$  max for the 2B22J/2B22K. Both span and offset are adjustable by the optional external potentiometers.

Featuring a wide range, single supply operation (+14V to +32V), the 2B22 provides isolated +28V loop power and is capable of delivering rated current into an external 0 to 1000 $\Omega$ load resistance. The unique output stage configuration also allows the user to utilize an optional external loop power supply to interface systems designed for a two-wire operation.

#### APPLICATIONS

Model 2B22 has been specifically designed for high accuracy applications in process control and monitoring systems to offer complete galvanic isolation and protection against damage from transients and fault voltages in transn.itting information between subsystems or separated system elements. The 2B22



meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 4, Class U isolated current loop transmitters.

In the industrial environment, model 2B22 can serve as a transmission link between such system elements as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners. In data acquisition and control systems, the 2B22 may act as an isolated interface between the D/A converter output of a microcomputer and standard 4 to 20mA analog loops.

#### DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 2B22 is a conservatively designed, compact, epoxy encapsulated module capable of reliable operation in harsh environments. To assure high reliability, the 2B22 has a calculated MTBF of over 270,000 hours and has been designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

**Process Signal Compatibility**: The versatile input stage design with a single resistor gain adjustment enables the 2B22 to accept any one of the standard inputs-0-1V, 0-10V, 1-5V; or 1-5mA, 4-20mA, 10-50mA; and provide standard, isolated 4-20mA output.

Isolated Loop Power: Internal 28V dc loop supply, completely isolated from the input power terminals ( $\pm 1500V$  dc isolation), provides the capability to drive 0 to  $1000\Omega$  loads and eliminates the need for an external dc/dc converter.

## **SPECIFICATIONS** (typical @ +25°C and V<sub>S</sub> = +15V unless otherwise noted)

Model	2B22J	2B22K	2B22L
INPUT SPECIFICATIONS			
Voltage Signal Range, G = 1.6mA/V	0 to +10V	•	•
G = 16mA/V	0 to +1V	•	•
Gain Range	1.6 to 16mA/V	•	•
Maximum Safe Input	+15V	•	•
Input Impedance	10MΩ		
OUTPUT SPECIFICATIONS	4 20 4		•
Load Resistance Range Va = +14V to +32V	4 to 20mA		
Internal Loop Power	$0$ to $1000\Omega$ max	•	•
Maximum Output Current.	0 10 100012 11122		
Input Overload	25mA	•	•
Output Ripple, 100Hz Bandwidth			
G = 1.6mA/V	60µA pk-pk	•	•
NONLINEARITY (% of Span)	±0.2% max	±0.1% max	±0.05% max
CMV, INPUT TO OUTPUT			
ac, 60Hz, 1 Minute Duration	1500V rms	•	•
Continuous, ac or de	±1500V pk max	·	• · · · · · · · · · · · · · · · · · · ·
CMR, INPUT TO OUTPUT			
60Hz, 1kΩ Source Imbalance	90dB	•	•
ACCURACY <sup>1</sup> Warm Up Time to Rated Performance 5 Minut	cs		
Total Output Error @ +25°C <sup>1,2</sup>			
Offset $(V_{IN} = 0V)$	±0.25% max	±0.25% max	±0.1% max
$Span (V_{IN} = +10V)$	±0.25% max	±0.25% max	±0.1% max
vs. Temperature (0 to $+70^{\circ}$ C, G = 1.6mA/V)			
Offset $(V_{IN} = 0V)$	±0.01%/°C max	±0.005%/°C max	±0.0025%/°C max
$Span (V_{IN} = +10V)$	±0.015%/ C max	±0.01%/ C max	±0.005%/ C max
Vs. Temperature (0 to $\pm 70$ C) Officient (View = 0V, C = 1.6m A/V to)			
16mA(V)	+0.01%/°C	+0.005%/°C	±0.0025%/°C
$Span (G = 1.6 mA/V to 16 mA/V)^3$	±0.015%/°C	±0.01%/°C	±0.005%/°C
DVNAMIC RESPONSE	······		·
Settling Time - to 0.1% of F.S. for 10V Step	300us	+	•
Slew Rate	0.06mA/µs	•	•
REFERENCE INPLIT	····		
Voltage	+2.5V dc	•	•
Input Impedance	6kΩ	•	•
OSCILLATOR			
Frequency, Internal Oscillator	100kHz ± 10%	•	•
External Sync Input			
Frequency	100kHz ± 10% max	•	•
Waveform	Square wave,	•	• .
	50% duty cycle		
Voltage	20V p-p		
POWER SUPPLY			
Voltage, Rated Performance	+15V dc	•	•
Voltage, Operating	+14V to $+32V$ dc	•	•
Supply Current (at Full Scale Output)	100-	•	•
Using External Loop Power	50mA	*	• ,.
Supply Change Effect (% of Span)	J 511/1		
on Offset (VIN = 0V)	±0.0005%/V	•	•
on Span ( $V_{IN} = +10V$ )	±0.0005%/V	•	•
TEMPERATURE RANGE			······································
Rated Performance	0 to +70°C	•	•
Operating	-25°C to +75°C	•	• • • •
Storage	-55°C to +85°C	• .	•
CASE SIZE	2.2" × 3" × 0.6"	•	•

NOTES

Accuracy is guaranteed at G = 1.6mA/V with no external trim

Activity is got allocated at  $S = 0.001 \text{ J}^{-1}$  with no externation adjustments when connected as shown in Figure 1. All accuracy is % of span where span is 16mA (±0.1% = ±0.016mA error). Span T.C. for gains higher than 1.6mA/V is RG dependent – a low T.C.

(±10ppm/°C) RG is recommended for best performance.

\*Specifications same as 2B221

Specifications subject to change without notice.

### **OUTLINE DIMENSIONS** Dimensions shown in inches and (mm). 3.04 MAX (77.2) MODEL 2B22 (15.1) 0.040 (1.02) -T REF OU 2.23 MA> (56.64) TOUT 12 BOTTOM VIEW - 0.1 (2.54) GRID WEIGHT: 150 ams

**MATING SOCKET: AC1579** 

#### INTERCONNECTION DIAGRAM

Model 2B22 can be applied directly to achieve rated performance as shown in Figure 1 below. The input stage gain of 1.6mA/V, to convert a 0 to +10V signal into a 4 to 20mA output current, is obtained with the values shown. A single polarity power supply (+14V to +32V dc) should be connected to pin 8. To eliminate ground loops, the user should ensure that the signal return (common) lead does not carry the power supply current. Power common (pin 7) and signal common (pin 6) should be tied at the power supply common terminal. The voltage difference between pins 6 and 7 should not exceed 0.2V. An internal dc-dc converter provides isolated output loop power (pins 13 and 14), which is connected externally to the current output terminals (pins 11 and 12) and a load resistance. The standard 4 to 20mA current output signal is delivered into any external load between zero and 1000Ω.



Figure 1. Basic Connections

#### VOL. II, 9-20 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS

### Applying the Isolated Voltage-to-Current Converter

#### FUNCTIONAL DESCRIPTION

The high performance of model 2B22 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier, modulator section and the current output circuitry. The block diagram for model 2B22 is shown in Figure 2 below.

The 2B22 produces an isolated 4 to 20mA output current which is proportional to the voltage input and independent of the load resistance. The input amplifier operates single-ended and accepts a positive voltage within 0 to +10V range. Gain can be set from 1.6mA/V to 16mA/V by changing the gain resistor R<sub>G</sub> to accommodate input ranges from 0 to +1V (G = 16mA/V) to 0 to +10V (G = 1.6mA/V). The transfer function is I<sub>QUT</sub> = (4mA + G × V<sub>IN</sub>).

An internal, high stability reference has nominal output voltage of +2.5V (REF OUT) and is used to develop a 4mA output current for a 0 volts input. The terminals REF OUT (pin 1) and REF IN (pin 2) should be connected via the offset setting resistor  $R_0$ . For ratiometric operation, an external reference voltage can be connected to the REF IN terminal.

The 2B22 is designed to operate from a single positive power supply over a wide range of +14V to +32V dc. An internal dc-dc converter provides isolated +28V loop power which is independent of +V<sub>S</sub>. The maximum resistance of the ioad R<sub>L</sub> (resistance of the receivers plus the resistance of the connecting wire) is 1000 $\Omega$ . Since the loop power is derived from the input side, the current capability of the power supply (+V<sub>S</sub>) must be 100mA min to supply full output signal current.



Figure 2. Block Diagram - Model 2B22

#### **OPTIONAL TRIM ADJUSTMENTS**

Model 2B22 is factory calibrated for a 0 to +10V input range (G = 1.6mA/V). As shipped, the 2B22 meets its listed specifications without use of any external trim potentiometers. Additional trim adjustment capability, to reduce span and offset errors to  $\pm 0.05\%$  max, is easily provided as shown in Figure 3. The span and offset trim pots are adjusted while monitoring the voltage drop across a precision (or known) load resistor. The following trim procedure is recommended:

1. Connect model 2B22 as shown in Figure 3.

2. Apply  $V_{IN}$  = 0 volts and adjust  $R_O$  (Offset Adjust) for  $V_{OUT}$  = +2V  $\pm$  4mV.

3. Apply  $V_{IN}$  = +10.00V and adjust  $R_G$  (Span Adjust) for  $V_{OUT}$  = +10V ± 4mV.



Figure 3. Optional Span and Offset Adjustment

#### GAIN AND OFFSET SETTING

The gain of the 2B22 is a scale factor setting that establishes the nominal conversion relationship to accommodate +1V to +10V full scale inputs (V<sub>IN</sub>). The value of the gain setting resistor R<sub>G</sub> is determined by: R<sub>G</sub>(kΩ) = 6.314SF/(10.1 - SF) where SF is a scale factor equal to the value of V<sub>IN</sub> F.S. Example: to convert a 0 to +1V input to the 4 to 20mA output, SF = 1 and R<sub>G</sub> = 693Ω. Due to device tolerances, allowance should be made to vary R<sub>G</sub> by ±5% using the potentiometer.

The value of the offset resistor  $R_0$  is independent from the gain setting and given by the relationship:  $R_0$  (k $\Omega$ ) = 2.5 ( $V_{REF} - 2.4$ ) where  $V_{REF}$  is the reference voltage applied. For example, the reference provided by the 2B22 is +2.5V and therefore  $R_0 = 250\Omega$ . The accuracy of the R<sub>O</sub> calculation from from the above formula is ±5%. When an external reference operation is desired (i.e. for ratiometric operation), connect the reference voltage via  $R_0$  to pin 2 and leave pin 1 open.

#### EXTERNAL LOOP POWER OPERATION

For maximum versatility, the 2B22's output stage is designed to operate from the optional, isolated external loop power supply. This feature allows the user to interface systems wired for a two-wire operation. As shown in Figure 4, the same wiring is used for loop power and output. The load resistance is connected in series with an external dc power supply (+6V to +32V), and the current drawn from the supply is the 4 to 20mA output signal. The input stage of the 2B22 still requires +V<sub>S</sub> power, but the current drain from +V<sub>S</sub> is limited to 50mA. Use of an external loop power may require gain and offset trimming to obtain specified accuracy. The maximum series load resistance depends on the loop supply voltage as shown in Figure 4.



Figure 4. Optional External Loop Power Operation

#### SYNCHRONIZING MULTIPLE 2B22'S

In applications where multiple 2B22's are used in close proximity, radiated individual oscillator frequencies may cause "beat frequency" related output errors. These errors can be eliminated by synchronizing multiple units by connecting the SYNC OUT (pin 10) terminal to the SYNC IN (pin 9) terminal of the adjacent 2B22. The SYNC OUT terminal of this "slaved" unit can be used to drive another adjacent 2B22 (Figure 5). For best accuracy, each 2B22 should be retrimmed when synchronizing connections are used.



Figure 5. Multiple 2B22's Synchronization

#### **OUTPUT PROTECTION**

The current output terminals (pins 11 and 12) are protected from shorts up to +32V dc but in many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 6 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.



Figure 6. Output Protection Circuitry Connections

### APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

**Process Signal Isolator:** In process control applications, model 2B22 can be applied to interface standard process signals (e.g. 1 to 5mA, 4 to 20mA, 10 to 50mA, 1 to 5V) and convert them to isolated 4 to 20mA output. A typical hook-up of model 2B22 is illustrated in Figure 7, showing input resistor



Figure 7. Process Signal Current Isolator

 $R_C$  converting the current from a remote loop to a voltage input, and a span adjustment resistor  $R_G$ . A value of  $R_C$  should be selected to develop a minimum of +1V signal with full scale input current applied. For example, a 50 $\Omega$  resistor converts the 4 to 20mA current input to a 200mV to 1V voltage input, which the 2B22 isolates and converts to a 4 to 20mA output. The reference input (pin 2) is not connected since the process signal provides a desired offset.

Isolated D/A Converter: Model 2B22 offers total ground isolation and protection from high voltage transients in interfacing D/A converters to standard 4 to 20mA current loops. This requirement is common in a microcomputer-based control system. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the D/A converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 8. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B22. First, a digital input code of all one's is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all zero's is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA less 1LSB (19.9961mA).



#### Figure 8. D/A Converter – Isolated 4 to 20mA Interface

Pressure Transmitter: In Figure 9, model 2B22 is used in a pressure transmitter application to provide complete inputoutput isolation and avoid signal errors due to ground loop currents. The process pressure is monitored with a strain gage type pressure transducer interfaced by the Analog Devices' model 2B30 transducer conditioner. The bridge excitation and system power is provided by the model 2B35 triple output power supply. The high level voltage output of the 2B30 is converted to the isolated 4 to 20mA current for transmission to a remote recorder or indicator.



Figure 9. Isolated Pressure Transmitter

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### Programmable Output, Isolated Voltage-to-Current Converter

**MODEL 2B23** 

#### FEATURES

Wide Input Range, Resistor Programmable
Pin Programmable Output: 4 to 20mA or 0 to 20mA
High CMV Input/Output Isolation: ± 1500V pk
Continuous
Low Nonlinearity: ±0.05% max (2B23K)
Low Span Drift: ±0.005%/°C max (2B23K)
Single Supply Operation: +14V to +28V
Small Size: 1.8" × 2.4" × 0.6"
Meets IEEE Std. 472: Transient Protection (SWC)
Meets ISA Std. 50.1: Isolated Current Loop
Transmitters

#### **APPLICATIONS**

Industrial Instrumentation and Process Control Ground Loop Elimination Transient Voltage Protection Analog Transmitters and Controllers Remote Data Acquisition Systems

#### **GENERAL DESCRIPTION**

The model 2B23 is a high performance, low cost voltage to current converter featuring  $\pm 1500V$  pk input to output isolation for interfacing with standard process signals. The input stage of the 2B23 may be single resistor programmed to accept voltages within a 0 to + 10V range (+0.1V to + 10V full scale). The isolated output is pin programmable to provide current in the range of 4 to 20mA or 0 to 20mA and can be operated with 0 to 800 $\Omega$  grounded or floating loads.

The 2B23 uses reliable transformer isolation techniques and is available in two accuracy selections offering guaranteed nonlinearity error (2B23K:  $\pm 0.05\%$  max, 2B23J:  $\pm 0.1\%$  max) and guaranteed low span drift (2B23K:  $\pm 0.005\%^{\circ}$ C max, 2B23J:  $\pm 0.01\%^{\circ}$ C max). The internally trimmed span and offset errors are  $\pm 0.1\%$  for the 2B23K and  $\pm 0.25\%$  for the 2B23J. Both span and offset may be adjusted using optional external potentiometers.

Featuring wide range, single supply operation (+14V to +28V dc), the 2B23 provides isolated loop power, thus eliminating the need for an external dc/dc converter.

#### APPLICATIONS

Model 2B23 has been designed to provide high accuracy, versatility and low cost in industrial and laboratory system applications requiring isolated current transmission. The 2B23 meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" and may serve as a transmission link between such system elements as computers, controllers, actuators, recorders and indicators.



In data acquisition and control systems, the 2B23 may act as an isolated interface between the D/A converter output of a microcomputer analog I/O and standard 4 to 20mA or 0 to 20mA analog loops. In process control systems, the 2B23 may be used as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-to-pneumatic transducers.

#### DESIGN FEATURES AND USER BENEFITS

High CMV Isolation: The 2B23 features high input to output galvanic isolation to eliminate ground loops and offer protection against damage from transients and fault voltages. Its isolation barrier will withstand continuous CMV of  $\pm 1500V$  pk and 1500V rms @ 60Hz for 60 seconds.

High Reliability: To assure high reliability in harsh industrial environments, reliable magnetic isolation is used. The 2B23 meets the IEEE Standard for Transient Voltage Protection (472– 1974: Surge Withstand Capability) and offers reliable operation over  $-25^{\circ}$ C to  $+85^{\circ}$ C temperature range.

**Versatility:** The 2B23 can be easily tailored to the user's application, accommodating a wide range of input voltages, providing pin programmable, standard current outputs and offering wide range, single supply operation.

Small Size: To conserve board space, the 2B23 is packaged in a compact,  $1.8'' \times 2.4'' \times 0.6''$  module.

# **SPECIFICATIONS** (typical @ $+25^{\circ}C$ and $V_s = +15V$ unless otherwise noted)

INPUT SPECIFICATIONSDimensions :Input Voltage Range $0$ to $+10V$ *Factory Calibrated $0$ to $+10V$ *Full Scale Input $+0.1V \min$ to $+10V \max$ *Transfer Function (TF) $*$ Factory Calibrated $1.6mA/V$ *User Programmable $1.6mA/V$ *User Programmable $1.6mA/V$ *Input Impedance $10M\Omega$ *OUTPUT SPECIFICATIONS $*$ Current Output Range $10M\Omega$ *User Selectable $4$ to $20mA$ , $0$ to $20mA$ *Load Resistance Range $0$ to $800\Omega$ maxInput Overload $22mA$ typOutput Noise $0$ to $800\Omega$ max100H2 Bandwidth $1.5\muA$ pk-pkISOLATION $*$ CMV, Input to Output $ac_{0}$ 60Hz, 1km Source Imbalance@ 60Hz, 1kM Source Imbalance $86dB$ $ACCURACY^1$ $*$ ManuesWarm Up Time to Rated Performance $5$ Minutes* $*$ $ACCURACY^1$ $5$ Minutes	Model	2B23J	2B23K	OUTLI
Input Voltage Range Factory Calibrated0 to + 10V*Factory Calibrated0 to + 10V max*Transfer Function (TF) Factory Calibrated1.6mA/V*Transfer Function (TF) Factory Calibrated1.6mA/V*Waximum Safe Input $\pm 15V$ *OUTPUT SPECIFICATIONS Current Output Range User Selectable4 to 20mA, 0 to 20mA*User Selectable4 to 20mA, 0 to 20mA*Load Resistance Range Internal Loop Power0 to 800Ω max*Output Noise 100Hz Bandwidth1.5µA pk-pk*NONLINEARITY $\pm 0.1\%$ max $\pm 0.05\%$ max( $\pm 0.02\%$ typ)ISOLATION CMV, Input to Output ac, 60Hz, 1 min C 60Hz, 1kΩ Source Imbalance86dB*@ 60Hz, 1kΩ Source Imbalance86dB* $@$ CCURACY1 Warm Up Time to Rated Performance5 Minutes*	INPUT SPECIFICATIONS		-	Dimensions
Factory Calibrated0 to + 10V*Full Scale Input+0.1V min to + 10V max*Transfer Function (TF)Factory Calibrated1.6mA/VFactory Calibrated1.6mA/V*User Programmable1.6mA/V to 200mA/V*Maximum Safe Input $\pm 15V$ *Input Impedance10MΩ*OUTPUT SPECIFICATIONSCurrent Output Range $1 \pm 0.20 \text{ (Sol)}$ Current Output Range0 to 800Ω max*User Selectable4 to 20mA, 0 to 20mA*Input Overload22mA typ*Output Noise1.5µA pk-pk*100Hz Bandwidth1.5µA pk-pk*NONLINEARITY $\pm 0.1\%$ max $\pm 0.05\%$ max( $\pm 0.02\%$ typ)ISOLATIONCMW, Input to Output ac, 60Hz, 1 kin Source Imbalance86dB*@ 60Hz, 1kΩ Source Imbalance86dB*@ 60Hz, 1kΩ Source ImbalanceSo Minutes*	Input Voltage Range			
Full Scale Input $+0.1V \text{ min to } +10V \text{ max}$ $*$ Transfer Function (TF)1.6mA/V $*$ Factory Calibrated1.6mA/V to 200mA/V $*$ User Programmable1.6mA/V to 200mA/V $*$ Input Impedance10MΩ $*$ OUTPUT SPECIFICATIONS $*$ $\bullet$ Current Output Range4 to 20mA, 0 to 20mA $*$ User Selectable4 to 20mA, 0 to 20mA $*$ Load Resistance RangeInternal Loop Power0 to 800Ω max $*$ Output Noise22mA typ $*$ $\bullet$ set for for the set of the set	Factory Calibrated	0 to + 10V	* .	
Transfer Function (TF) Factory Calibrated1.6mA/V*User Programmable1.6mA/V to 200mA/VMaximum Safe Input $\pm 15V$ Input Impedance10MΩOUTPUT SPECIFICATIONS Current Output Range User Selectable4 to 20mA, 0 to 20mAUser Selectable4 to 20mA, 0 to 20mALoad Resistance Range Internal Loop Power0 to 800Ω maxMaximum Output Current @ Input Overload22mA typOutput Noise 100Hz Bandwidth1.5µA pk-pkNONLINEARITY $\pm 0.1\%$ max $\pm 0.05\%$ max( $\pm 0.02\%$ typ)ISOLATION CMV, Input to Output ac, 60Hz, 1 min @ 60Hz, 1kΩ Source Imbalance@ 60Hz, 1kΩ Source Imbalance86dB*@ 60Hz, 1kΩ Source Imbalance86dB*Warm Un Time to Bated Performance5 Minutes*	Full Scale Input	+0.1V min to $+10V$ max	*	
Factory Calibrated1.6mA/V*User Programmable1.6mA/V to 200mA/V*Maximum Safe Input $\pm 15V$ *Input Impedance10MΩ*OUTPUT SPECIFICATIONS*Current Output Range4 to 20mA, 0 to 20mA*User Selectable4 to 20mA, 0 to 20mA*Load Resistance Range0 to 800Ω max*Internal Loop Power0 to 800Ω max*@ Input Overload22mA typ*Output Noise1.5µA pk-pk*100Hz Bandwidth1.5µA pk-pk*CMV, Input to Outputac, 60Hz, 1 min1500V rmsac, 60Hz, 1 min1500V pk*@ 60Hz, 1kΩ Source Imbalance86dB*@ 60Hz, 1kΩ Source Imbalance86dB*Warm Un Time to Bated Performance5 Minutes*	Transfer Function (TF)			
User Programmable1.6mA/V to 200mA/V $\star$ Maximum Safe Input $\pm 15V$ $\star$ Input Impedance10MΩ $\star$ OUTPUT SPECIFICATIONSCurrent Output RangeUser Selectable4 to 20mA, 0 to 20mALoad Resistance Range0 to 800Ω maxInternal Loop Power0 to 800Ω max@ Input Overload22mA typOutput Noise1.5 $\mu$ A pk-pk100Hz Bandwidth1.5 $\mu$ A pk-pkCMV, Input to Output $\star$ ac, 60Hz, 1 min1500V rmsCMR@ 60Hz, 1kΩ Source Imbalance@ 60Hz, 1kΩ Source Imbalance86dBXaren Un Time to Bated Performance5 MinutesYaren5 Minutes	Factory Calibrated	1.6mA/V	*	+ 1 -
Maximum Safe Input $\pm 15V$ $\star$ Input Impedance10MΩ $\star$ OUTPUT SPECIFICATIONSCurrent Output RangeUser Selectable4 to 20mA, 0 to 20mALoad Resistance RangeInternal Loop Power0 to 800Ω maxMaximum Output Current@ Input Overload22mA typOutput Noise100Hz Bandwidth1.5 $\mu$ A pk-pkNONLINEARITY $\pm 0.1\%$ max± 0.05% max ( $\pm 0.02\%$ typ)ISOLATIONCMW, Input to Outputac, 60Hz, 1 kin Source Imbalance@ 60Hz, 1kΩ Source Imbalance86dB*Warm Un Time to Bated PerformanceS Minutes*	User Programmable	1.6mA/V to 200mA/V	*	. — —
Input Impedance10M11*OUTPUT SPECIFICATIONS Current Output Range User Selectable4 to 20mA, 0 to 20mA*Load Resistance Range Internal Loop Power0 to 800Ω max*Maximum Output Current @ Input Overload22mA typ*Output Noise 100Hz Bandwidth1.5 $\mu$ A pk-pk*NONLINEARITY $\pm$ 0.1% max $\pm$ 0.05% max( $\pm$ 0.02% typ)ISOLATION CMV, Input to Output ac, 60Hz, 1 min @ 60Hz, 1kΩ Source Imbalance1500V rms $\pm$ 1500V pk*@ 60Hz, 1kΩ Source Imbalance86dB*Warm Un Time to Bated Performance5 Minutes*	Maximum Safe Input	±15V	*	0.20 (5.08)
OUTPUT SPECIFICATIONS Current Output Range User Selectable $4 \text{ to } 20\text{mA}, 0 \text{ to } 20\text{mA}$ $4 \text{ to } 20\text{mA}, 0 \text{ to } 20\text{mA}$ $4 \text{ to } 20\text{mA}, 0 \text{ to } 20\text{mA}$ Load Resistance Range Internal Loop Power0 to $800\Omega \text{ max}$ $*$ $4 \text{ to } 20\text{mA}, 0 \text{ to } 20\text{mA}$ @ Input Overload22mA typ $*$ $4 \text{ to } 20\text{mA}, 0 \text{ to } 20\text{mA}$ $4 \text{ to } 20\text{ max}$ @ Input Overload22mA typ $*$ $4 \text{ to } 800\Omega \text{ max}$ $4 \text{ to } 800\Omega \text{ max}$ 0 utput Noise 100Hz Bandwidth $1.5\mu\text{A pk-pk}$ $*$ $6 \text{ sing condition}$ ISOLATION CMV, Input to Output ac, 60Hz, 1 min Continuous, ac or dc $1500V \text{ rms}$ $*$ $2 \text{ condition}$ @ 60Hz, 1k\Omega Source Imbalance $86\text{dB}$ $*$ $6 \text{ single and } 4 \text{ to } 80\text{ condition}$ $6 \text{ single and } 4 \text{ to } 80\text{ condition}$ @ 60Hz, 1k\Omega Source Imbalance $86\text{dB}$ $*$ $6 \text{ single and } 4 \text{ to } 80\text{ condition}$ $6 \text{ single and } 4 \text{ to } 80\text{ condition}$ Warm Un Time to Rated Performance $5 \text{ Minutes}$ $*$ $4 \text{ condition}$	Input Impedance	10ΜΩ	*	<b>HTTT</b>
Current Output Range User Selectable     4 to 20mA, 0 to 20mA     *       Load Resistance Range Internal Loop Power     0 to 800Ω max     *       Maximum Output Current     0 to 800Ω max     *       @ Input Overload     22mA typ     *       Output Noise 100Hz Bandwidth     1.5µA pk-pk     *       NONLINEARITY     ± 0.1% max     ± 0.05% max(± 0.02% typ)       ISOLATION CMV, Input to Output ac, 60Hz, 1 min     1500V rms     *       @ 60Hz, 1kΩ Source Imbalance     86dB     *       @ 60Hz, 1kΩ Source Imbalance     86dB     *	OUTPUT SPECIFICATIONS			
User Selectable 4 to 20mA, 0 to 20mA * Load Resistance Range Internal Loop Power 0 to 800Ω max * Maximum Output Current @ Input Overload 22mA typ * Output Noise 100Hz Bandwidth 1.5µA pk-pk * NONLINEARITY ±0.1% max ±0.05% max(±0.02% typ) ISOLATION CMV, Input to Output ac, 60Hz, 1 min 1500V rms * CMR @ 60Hz, 1kΩ Source Imbalance 86dB * ACCURACY <sup>1</sup> Warm Un Time to Bated Performance 5 Minutes *	Current Output Range			
Load Resistance Range Internal Loop Power 0 to 800Ω max * Maximum Output Current @ Input Overload 22mA typ * Output Noise 100Hz Bandwidth 1.5µA pk-pk * NONLINEARITY ±0.1% max ±0.05% max (±0.02% typ) ISOLATION CMV, Input to Output ac, 60Hz, 1 min 1500V rms * Continuous, ac or dc ±1500V pk * Transient Protection - CMR @ 60Hz, 1kΩ Source Imbalance 86dB * ACCURACY <sup>1</sup> Warm Un Time to Bated Performance 5 Minutes *	User Selectable	4 to 20mA, 0 to 20mA	*	
Internal Loop Power0 to $800\Omega$ max*Maximum Output Current0 in put Overload $2mA$ typ* $@$ Input Overload $2mA$ typ*Output Noise $1.5\muA$ pk-pk*100Hz Bandwidth $1.5\muA$ pk-pk*NONLINEARITY $\pm 0.1\%$ max $\pm 0.05\%$ max ( $\pm 0.02\%$ typ)ISOLATIONCMV, Input to Outputac, 60Hz, 1 min1500V rms*Continuous, ac or dc $\pm 1500V$ pk*Transient Protection -IEEE Std. 472 (SWC)* $@$ 60Hz, 1k\Omega Source Imbalance86dB*ACCURACY1Warm Un Time to Bated Performance5 MinutesWarm Un Time to Bated Performance5 Minutes*	Load Resistance Range			
Maximum Output Current (@ Input Overload $22mA typ$ *Output Noise 100Hz Bandwidth $1.5\muA pk-pk$ *NONLINEARITY $\pm 0.1\% max$ $\pm 0.05\% max (\pm 0.02\% typ)$ ISOLATION CMV, Input to Output $ac, 60Hz, 1 min$ $1500V rms$ *Continuous, ac or dc $\pm 1500V pk$ *Transient Protection - CMR (@ 60Hz, 1k\Omega Source Imbalance $86dB$ *ACCURACY1 Warm Un Time to Bated Performance5 Minutes*	Internal Loop Power	$0$ to $800\Omega$ max	*	A SIG COM
@ Input Overload     22mA typ     *       Output Noise     1.5μA pk-pk     *       100Hz Bandwidth     1.5μA pk-pk     *       NONLINEARITY     ± 0.1% max     ± 0.05% max(± 0.02% typ)       ISOLATION     CMV, Input to Output     ac, 60Hz, 1 min       Continuous, ac or dc     ± 1500V pk     *       Transient Protection ~     IEEE Std. 472 (SWC)     *       @ 60Hz, 1kΩ Source Imbalance     86dB     *       ACCURACY <sup>1</sup> Warm Un Time to Bated Performance     5 Minutes	Maximum Output Current			
Output Noise 100Hz Bandwidth1.5 $\mu$ A pk-pkNONLINEARITY $\pm$ 0.1% max $\pm$ 0.05% max( $\pm$ 0.02% typ)ISOLATION CMV, Input to Output ac, 60Hz, 1 min Continuous, ac or dc $\pm$ 1500V rms $\star$ Transient Protection - CMR @ 60Hz, 1k\Omega Source ImbalanceBottom Kar 86dBDimensionsMax $\Delta CCURACY^1$ Warm Un Time to Bated PerformanceS Minutes $\star$	@ Input Overload	22mA typ	*	OT GAIN AD
100Hz Bandwidth     1.5μA pk-pk     *     BOTTOM VIEW       NONLINEARITY     ± 0.1% max     ± 0.05% max (± 0.02% typ)     MA       ISOLATION     CMV, Input to Output     ac, 60Hz, 1 min     1500V rms     *       Continuous, ac or dc     ± 1500V pk     *     Dimensions       Transient Protection -     IEEE Std. 472 (SWC)     *     •       @ 60Hz, 1kΩ Source Imbalance     86dB     *     •     •       ACCURACY1     Warm Un Time to Bated Performance     5 Minutes     *     •	Output Noise			Him
NONLINEARITY     ± 0.1% max     ± 0.05% max (± 0.02% typ)       ISOLATION     ISOLATION     MA       CMV, Input to Output     ac, 60Hz, 1 min     1500V rms     *       Continuous, ac or dc     ± 1500V pk     *       Transient Protection -     IEEE Std. 472 (SWC)     *       @ 60Hz, 1kΩ Source Imbalance     86dB     *       ACCURACY1     Warm Un Time to Rated Performance     5 Minutes	100Hz Bandwidth	1.5μA pk-pk	*	BOTTOM VIEW
ISOLATION MA CMV, Input to Output ac, 60Hz, 1 min 1500V rms * Dimensions Continuous, ac or dc ± 1500V pk * Transient Protection - IEEE Std. 472 (SWC) * @ 60Hz, 1kΩ Source Imbalance 86dB * ACCURACY <sup>1</sup> Warm Up Time to Bated Performance 5 Minutes *	NONLINEARITY	$\pm 0.1\%$ max	$\pm 0.05\% \max(\pm 0.02\% \text{ typ})$	36.4
CMV, Input to Output     ac, 60Hz, 1 min     1500V rms     *       Continuous, ac or dc     ± 1500V pk     *       Transient Protection -     IEEE Std. 472 (SWC)     *       CMR     @ 60Hz, 1kΩ Source Imbalance     86dB     *       ACCURACY <sup>1</sup>	ISOLATION	•	· ·	MA
ac, 60Hz, 1 min     1500V rms     *       Continuous, ac or dc     ± 1500V pk     *       Transient Protection -     IEEE Std. 472 (SWC)     *       CMR     @ 60Hz, 1kΩ Source Imbalance     86dB     *       ACCURACY <sup>1</sup>	CMV, Input to Output		4	
Continuous, ac or dc     ± 1500V pk     *       Transient Protection -     IEEE Std. 472 (SWC)     *       CMR     @ 60Hz, 1kΩ Source Imbalance     86dB     *       ACCURACY <sup>1</sup>	ac, 60Hz, 1 min	1500V rms	*	Dimensions
Transient Protection -     IEEE Std. 472 (SWC)     *       CMR     @ 60Hz, 1kΩ Source Imbalance     86dB     *       ACCURACY <sup>1</sup>	Continuous, ac or dc	±1500V pk	* .	
CMR @ 60Hz, 1kΩ Source Imbalance 86dB * ACCURACY <sup>1</sup> Warm Up Time to Rated Performance 5 Minutes *	Transient Protection -	IEEE Std. 472 (SWC)	*	0.52
@ 60Hz, 1kΩ Source Imbalance     86dB     *       ACCURACY <sup>1</sup> Image: Constraint of the second	CMR			(13.2)
ACCURACY <sup>1</sup> Warm Up Time to Rated Performance 5 Minutes *	@ 60Hz, 1kΩ Source Imbalance	86dB	*	0.52(13.2)
Warm Up Time to Rated Performance 5 Minutes *	ACCURACY <sup>1</sup>			
	Warm Up Time to Rated Performance	5 Minutes	*	
Total Output Error @ + 25°C <sup>2,3</sup>	Total Output Error @ + 25°C <sup>2,3</sup>			U REP O
Offset (V <sub>IN</sub> = 0V) $\pm 0.25\%$ max $\pm 0.1\%$ max $\bigcirc$ Ref M	Offset $(V_{IN} = 0V)$	$\pm 0.25\%$ max	± 0.1% max	@REF IN
Span ( $V_{IN} = +10V$ ) $\pm 0.25\%$ max $\pm 0.1\%$ max $\bigcirc$ Solution	$\text{Span}(V_{IN} = +10V)$	$\pm 0.25\%$ max	$\pm 0.1\%$ max	O SIG CI
vs. Temperature (0 to $+70^{\circ}$ C)	vs. Temperature (0 to + 70°C)			GAIN
Offset, 4-20mA Mode $\pm 0.01\%^{\circ}$ C max $\pm 0.005\%^{\circ}$ C max	Offset, 4-20mA Mode	±0.01%/°C max	$\pm 0.005\%$ /°C max	
0-20mA Mode $\pm 0.01\%$ °C typ $\pm 0.005\%$ °C typ	0-20mA Mode	±0.01%/°C typ	$\pm 0.005\%$ /°C typ	
Span, Both Modes $\pm 0.01\%$ °C max $\pm 0.005\%$ °C max	Span, Both Modes	± 0.01%/°C max	$\pm 0.005\%$ /°C max	(8.4)
DYNAMIC RESPONSE	DYNAMIC RESPONSE			·
Settling Time to 0.1% of FS for 10V Step 5ms *	Settling Time to 0.1% of FS for 10V Step	5ms	*	
Small Signal Bandwidth 400Hz *	Small Signal Bandwidth	400Hz	*	
POWER SUPPLY	POWER SUPPLY	······································	······	
Voltage, Rated Performance $(+V_0)$ + 15V dc *	Voltage, Rated Performance $(+V_c)$	+ 15V dc	*	
Voltage, Operating + 14V min to + 28V max *	Voltage, Operating	$+ 14V \min to + 28V \max$	* 1	
Supply Current (@ 20mA Output) 75mA *	Supply Current (@ 20mA Output)	75mA	*	
Supply Change Effect	Supply Change Effect			
on Offset and Span ±0.0015%/V *	on Offset and Span	±0.0015%/V	*	
ENVIRONMENTAL	ENVIRONMENTAL			
Temperature Range	Temperature Range	1		
Bated Performance $0$ to $+70^{\circ}$ C *	Rated Performance	$0$ to $+70^{\circ}$ C	*	
Observating $-25^{\circ}$ C to $+85^{\circ}$ C *	Operating	$-25^{\circ}$ C to $+85^{\circ}$ C	*	
Relative Humidity	Relative Humidity			
per MIL-STD 202, Method 103B ± 0.2% Error *	per MIL-STD 202. Method 103B	±0.2% Error	* *	
RFIImmunity	RFIImmunity			
27MHz @ 5W @ 3ft ± 0.1% Error *	27MHz @ 5W @ 3ft	± 0.1% Error	· · ·	
CASE SIZE 1.8" × 2.4" × 0.6" *	CASESIZE	1.8" × 2.4" × 0.6"	*	

### NE DIMENSIONS

shown in inches and (mm).



#### TING SOCKET: AC1586

shown in inches and (mm).



#### NOTES

<sup>1</sup>Accuracy is guaranteed (a, TF = 1.6mA/V with no external trim adjustments when connected in the basic configuration.

 $^2$  All accuracy is % of span where span is 16mA (i.e.,  $\pm 0.1\% = 0.016mA$  error).  $^3$  Span T.C. for transfer functions higher than 1.6mA/V is R<sub>G</sub> dependent – low T.C. ( $\pm 10ppm/^{\circ}C)$ R<sub>G</sub> recommended for best performance.

\*Specifications same as 2B23J.

Specifications subject to change without notice.

#### VOL. II, 9-24 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS

### Applying the Isolated Voltage-to-Current Converter

#### FUNCTIONAL DESCRIPTION

The high performance of model 2B23 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier stage, modulator, and current output circuitry. A block diagram of the 2B23 is shown in Figure 1.



Figure 1. 2B23 Functional Block Diagram

The model 2B23 produces an isolated 4 to 20mA or 0 to 20mA output current which is proportional to the input voltage and independent of the output load resistance. The input amplifier accepts a positive voltage within the range of 0 to + 10V. The transfer function of the input stage may be set from 1.6mA/V to 200mA/V (dependent upon the output current range desired) by changing the gain resistor  $R_G$  connected between pins 5 and 7.

An internal, high stability reference having a nominal output voltage of +5V (REF OUT) is used to develop a 4mA output current for a 0 volts input. REF OUT (Pin 3) and REF IN (Pin 4) should be connected via the offset scaling resistor R<sub>O</sub>. An output current bypass section allows scaling of the nominal 4 to 20mA output current to a range of 0 to 20mA. This is accomplished by connecting the output range select pin (Pin 12) to the I<sub>OUT</sub> pin (Pin 10) thereby providing a bypass for the 4mA. For 4-20mA operation, the bypass pin is connected to I<sub>OUT</sub> COMMON (Pin 11).

The 2B23 is designed to operate from a single positive power supply  $(+V_S)$  over a range of +14V to +28V dc. The power supply section consists of an input voltage regulator, a dc/dc converter, plus associated rectifying and filtering circuitry. The dc/dc converter generates isolated loop power which is independent of V<sub>S</sub> and capable of driving the maximum load resistance (resistance of receivers plus the resistance of connecting wire) of 800 $\Omega$ . The current capability of the power supply  $(+V_S)$  must be 75mA minimum to supply full output signal current.

#### **BASIC INTERCONNECTIONS**

The 2B23 may be applied to achieve rated performance as shown in Figure 2. The transfer function of 1.6mA/V, for conversion of the 0 to + 10V input signal into a 4 to 20mA output current, is obtained using the values shown ( $R_O = 10k\Omega$ ,  $R_{SC} = 301\Omega$ ,  $R_G$  open). For best performance,  $R_{SC}$  should be a metal film,  $\pm 0.1\%$  tolerance, 25ppm/°C resistor and  $R_O$  should be  $\pm 1\%$ , 100ppm/°C.



Figure 2. Basic Interconnections

A power supply  $(+V_S)$  is connected to Pin 1. To avoid ground loops, the user should ensure that the input signal return (SIG COM) does not carry the power supply return current. Power common (Pin 2) and signal common (Pin 5) should be tied at the power supply common terminal.

#### **OPTIONAL TRIM ADJUSTMENTS**

Model 2B23 is factory calibrated for a 0 to +10V input range and an output of 4 to 20mA, meeting its listed specifications without use of any external trim potentiometers. If desired, optional span and zero trim adjustments may be easily accomplished as described in the following sections.

Input Gain Adjustment: The input gain of the 2B23 is a scale factor setting that establishes the nominal conversion relationship to accommodate + 1V to + 10V full scale inputs (V<sub>IN</sub>). In addition, full scale inputs as low as 100mV may be accommodated.

The value of the gain setting resistor  $R_G$  is determined by:  $R_G$ ( $k\Omega$ ) = 10 $k\Omega/(G-1)$  where G represents a ratio of 10V/ $V_{IN}(V)$ F.S. For example, to convert a 0 to +1V input to 4 to 20mA output,  $V_{IN}$  F.S. = +1V and G = 10V/1V = 10, therefore  $R_G$ = 10 $k\Omega/9$  = 1.1 $k\Omega$ . Due to resistor tolerances, allowance should be made to vary  $R_G$  by using a series cermet type potentiometer (Figure 3). For best performance,  $R_G$  should be a metal film, 1% tolerance, 25ppm/°C resistor.



Figure 3. Input Gain Adjustment

Offset and Output Scaling Adjustments: After selecting the required input stage gain, the 2B23 must then be configured for either 4 to 20mA or 0 to 20mA output current range. Figures 4a and 4b illustrate the respective methods for each. The value of the offset resistor  $R_O$  is independent from the gain setting and may be adjusted by a series cermet pot.

For fine adjustment of the output current,  $R_{SC}$  value should be trimmed as shown in Figure 3.





#### **USING MULTIPLE 2B23s**

Unlike other transformer-based isolators, the 2B23 does not require any synchronizing circuits to eliminate beat frequency related output errors in multichannel applications. This is due to the use of pulse-width modulation technique in the 2B23. Radiated individual oscillator frequencies will have no effect upon performance, even in situations requiring multiple 2B23s to be located in close proximity to one another. For this reason, no provisions for external synchronization are necessary.

#### **OUTPUT PROTECTION**

The current output terminals (Pins 10 and 11) are protected for reverse voltage and shorts up to +32V dc but in many industrial applications it may be necessary to protect the 4 to 20mA from accidental shorts to ac line voltages. The circuit shown in Figure 5 may be employed for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.



Figure 5. Output Protection Circuitry

#### APPLICATIONS

In Figure 6, model 2B23 is used in multiloop application of the data acquisition and control system to provide isolated current interface to a recorder, indicator and a valve positioner.



Figure 6. Multiloop Isolation

In applications requiring current to voltage conversion, the 2B23 may be used as shown in Figure 7. An external -10V reference is used to provide necessary input offset. This circuit will provide  $\pm 1500V$  isolation in converting 4-20mA into a 0 to +10V output. The output measurement device must have a high input impedance to avoid loading errors.



Figure 7. 4-20mA to 0 to +10V Isolated Converter



# **Loop Powered Isolator**

**MODEL 2B24** 

### \_\_\_\_\_

#### **FEATURES**

Self-Powered Wide Input Range: 1-50mA (2B24B) High CMV Isolation: ±1500V pk; CMR: 120dB High Accuracy: ±0.1% RFI/EMI Immunity Low Cost

#### APPLICATIONS Ground Loop Elimination Transient Voltage Protection



#### **GENERAL DESCRIPTION**

The model 2B24 is a low cost, loop-powered isolator designed to accept input current in the range of 1-50mA and provide an isolated output current proportional to the input. The 2B24 is powered by the input signal and does not require an external power supply.

Two basic models are available for signal ranges of 4-20mA (2B24A) and 4-20mA or 10-50mA (2B24B). Both feature high accuracy ( $\pm 0.1\%$ ), high input to output isolation ( $\pm 1500V$  pk, continuous), and high CMR (120dB). Other features include low input signal loop burden, low sensitivity to variations in load, as well as excellent stability ( $\pm 0.01\%$ / °C) over a wide ambient temperature range ( $-30^{\circ}C$  to  $+85^{\circ}C$ ).

A rugged metal enclosure, suitable for field mounting, offers environmental protection and screw terminal input and output connections. This enclosure may be either surface or relay track mounted.

#### APPLICATIONS

The 2B24 is designed to eliminate ground loop problems and high common mode noise interference in process control, monitoring and factory automation systems. It is especially useful for providing individual isolation of many current loop outputs operating from a common source of dc power.

#### OPERATION

The 2B24 is factory calibrated to accuracy of  $\pm 0.1\%$  of span. A user accessible span trim potentiometer providing  $\pm 3\%$  adjustment range permits precise field calibration. This may be accomplished by connecting normal operating load resistance and adjusting SPAN for a 20.00mA output when an input is 20.00mA.

A wide range of load resistance (up to  $600\Omega$  @ 20mA and 240 $\Omega$  @ 50mA) may be accommodated by the 2B24. The transmitter supplying power to the 2B24 must be capable of furnishing the necessary input voltage for the given load and desired maximum output current.

#### **DESIGN FEATURES AND USER BENEFITS**

High Isolation: Input to output isolation eliminates ground loops and allows  $\pm 1500V$  potential difference between the input and the output.

Loop Powered: All power required for the 2B24 is derived from the process loop, eliminating the need for an external supply and therefore reducing installation cost.

High Noise Rejection: The 2B24 features internal filtering to eliminate errors caused by EMI/RFI and line noise pickup.

### SPECIFICATIONS (typical @ +25°C and IIN = 20mA unless otherwise noted)

Model	2B24A	2B24B
INPUT SPECIFICATIONS		
Input Signal	4-20mA	4-20mA, 10-50mA
Maximum Input Range	1-30mA	1-50mA
Input Voltage Requirement <sup>1</sup>	3.5V+ I <sub>OUT</sub> RL	•
OUTPUT SPECIFICATIONS		
Output Signal	4-20mA	4-20mA, 10-50mA
Maximum Output Range	1-30mA	1-50mA
Span Adjustment Range	±3% of Span	•
Load Resistance Range	0 to 600Ω @ 20mA	0 to 240Ω @ 50mA
Load Resistance Change Effect		
per 10Ω Change	±0.15% of Span	•
ACCURACY		
Total Output Error <sup>2</sup>	±0.1% @ R <sub>L</sub> = 300Ω	±0.1% @ R <sub>L</sub> = 120Ω
Linearity	±0.05% @ R <sub>L</sub> = 300Ω	±0.05% @ R <sub>L</sub> = 120Ω
Span Stability vs. Temperature	±0.01%/°C	•
ISOLATION		
CMV, Input to Output, Continuous	±1500V pk	•
Common Mode Rejection @ 60Hz	$120 \text{dB} \circledast \text{R}_{\text{L}} = 300 \Omega$	$120$ dB  R <sub>L</sub> = $120\Omega$
ENVIRONMENTAL		
Temperature Range, Operating	-30°C to +85°C	•
Storage Temperature Range	–55°C to +125°C	•
Humidity Effect, Span Error <sup>3</sup>	±0.2% of Span	•
RFI Effect (5W @ 470MHz @ 3 ft.)		
Error	±0,5% of Span	•
PHYSICAL		
Case Size	$4^{\prime\prime}  imes 3.25^{\prime\prime}  imes 1.25^{\prime\prime}$	•
Waight	8.5 oz (240g)	*









Figure 2. Required VINPUT vs. RLOAD (max) - 2B24A & B



Figure 1a. Two-Wire Transmitter Application

<sup>2</sup> Accuracy is specified as a percent of output span and includes

combined effects of repeatibility, hysteresis, and linearity.

Specifications subject to change without notice.

<sup>3</sup>Per MIL-STD-202, Method 103.

\*Specifications same as 2B24A.

#### **BASIC APPLICATIONS**

Figure 1b. Four-Wire Transmitter Application

# 

# High Performance, Economy Strain Gage/RTD Conditioners

### MODELS 2B30 AND 2B31

FEATURES

Low Cost Complete Signal Conditioning Function Low Drift:  $0.5\mu$ V/°C max ("L"); Low Noise:  $1\mu$ V p-p max Wide Gain Range: 1 to 2000V/V Low Nonlinearity: 0.0025% max ("L") High CMR: 140dB min (60Hz, G = 1000V/V) Input Protected to 130V rms Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz) Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100 $\mu$ A to 10mA) APPLICATIONS

Measurement and Control of:

Pressure, Temperature, Strain/Stress, Force, Torque Instrumentation: Indicators, Recorders, Controllers Data Acquisition Systems Microcomputer Analog I/O

#### GENERAL DESCRIPTION

Models 2B30 and 2B31 are high performance, low cost, compact signal conditioning modules designed specifically for high accuracy interface to strain gage-type transducers and RTD's (resistance temperature detectors). The 2B31 consists of three basic sections: a high quality instrumentation amplifier; a three-pole low pass filter, and an adjustable transducer excitation. The 2B30 has the same amplifier and filter as the 2B31, but no excitation capability.

Available with low offset drift of  $0.5\mu V/^{\circ}C \max (RTI, G = 1000V/V)$  and excellent linearity of  $0.0025\% \max$ , both models feature guaranteed low noise performance  $1\mu V$  p-p max, and outstanding 140dB common mode rejection (60Hz, CMV = ±10V, G = 1000V/V) enabling the 2B30/2B31 to maintain total amplifier errors below 0.1% over a 20°C temperature range. The low pass filter offers 60dB/decade roll-off from 2Hz to reduce normal-mode noise bandwidth and improve system signal-to-noise ratio. The 2B31's regulated transducer excitation stage features a low output drift (0.015%/<sup>o</sup>C max) and a capability of either constant voltage or constant current operation.

Gain, filter cutoff frequency, output offset level and bridge excitation (2B31) are all adjustable, making the 2B30/2B31 the industry's most versatile high-accuracy transducer-interface modules. Both models are offered in three accuracy selections, J/K/L, differing only in maximum nonlinearity and offset drift specifications.

#### APPLICATIONS

The 2B30/2B31 may be easily and directly interfaced to a wide variety of transducers for precise measurement and control of pressure, temperature, stress, force and torque. For ap-



TRANSDUCER SIGNAL CONDITIONING USING 2831

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plications in harsh industrial environments, such characteristics as high CMR, input protection, low noise, and excellent temperature stability make 2B30/2B31 ideally suited for use in indicators, recorders, and controllers.

The combination of low cost, small size and high performance of the 2B30/2B31 offers also exceptional quality and value to the data acquisition system designer, allowing him to assign a conditioner to each transducer channel. The advantages of this approach over low level multiplexers include significant improvements in system noise and resolution, and elimination of crosstalk and aliasing errors.

#### DESIGN FEATURES AND USER BENEFITS

High Noise Rejection: The true differential input circuitry with high CMR (140dB) eliminating common-mode noise pickup errors, input filtering minimizing RFI/EMI effects, output low pass filtering ( $f_c=2Hz$ ) rejecting 50/60Hz line frequency pickup and series-mode noise.

Input and Output Protection: Input protected for shorts to power lines (130V rms), output protected for shorts to ground and either supply.

Ease of Use: Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

**Programmable Transducer Excitation:** User-programmable adjustable excitation source-constant voltage (4V to 15V @ 100mA) or constant current (100µA to 10mA) to optimize transducer performance.

Adjustable Low Pass Filter: The three-pole active filter  $(f_c=2Hz)$  reducing noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency.

## **SPECIFICATIONS**

### (typical @ $+25^{\circ}$ C and VS = $\pm 15$ V unless otherwise noted)

MODEL	2B30J 2B31J	2B30K 2B31K	2B30L 2B31L	OUTLINE DIMENSIONS
GAIN <sup>1</sup>		····		Dimensions shown in inches and (mm).
Gain Range	1 to 2000V/V	•	•	2.01 (50.8) MAX
Gain Equation	$G = (1 + 94k\Omega/R_G) [20k\Omega/(R_F +$		. ·	
Gain Equation Accuracy	16.2k\$2)]	•	•	MODELS 2B30/31 (10.41)
Fine Gain (Span) Adjust. Range	±20%	•	•	
Gain Temperature Coefficient	±25ppm/°C max (±10ppm/°C typ)	•	•	0.20 (5.08) MIN
Gain Nonlinearity	±0.01% max	±0.005% max	±0.0025% max	- 0.25 (8.35) MAX
OFFSET VOLTAGES <sup>4</sup> Total Offset Voltage, Referred to Input				<b>916</b> 115 <b>9</b>
Initial, @ +25°C	Adjustable to Zero (±0.5mV typ)	•	•	
Warm-Up Drift, 10 Min., G = 1000	±5µV RTI	•	•	
G = 1V/V	$\pm 150 \mu V/^{\circ} C max$	±75uV/°C max	±50µV/°C max	0 23 (50.8) MAX
G = 1000V/V	±3µV/°C max	±1µV/°C max	±0.5µV/°C max	╞╬┰┼┼┼┼┼┼┼┼┼┼┼╄╡
At Other Gains	$\pm (3 \pm 150/G)\mu V/^{2}C max$	±(1 ± 75/G)µV/°C max	±(0.5 ± 50/G)µV/°C max	
vs. Time, $G = 1000V/V$	±3µV/month	•	•	Ŏ 29 <b>· · · · · · · · · · · · · · · · ·</b> · <b>·</b> · · · ·
Output Offset Adjust. Range	±10V	•	•	<u>╡╡┙┊╪┼┿┽┙</u> ┾╪┽╪┽┼┆ <u>╎┥┥</u> ┥╴ <mark>╿</mark>
INPUT BIAS CURRENT				BOTTOM VIEW
Initial @ +25°C	+200nA max (100nA typ) -0 6nA/°C	•	•	
vs. remperature (0 to +/0 C)		•	· · · · · · · · · · · · · · · · · · ·	PIN DESIGNATIONS
INFOI DIFFERENCE CURRENT Initial @ +25°C	±5nA	•	•	
vs. Temperature (0 to +70°C)	±40pA/°C	•	•	1 OUTPUT 1 (UNFILTERED) 16 EXC SEL 1
INPUT IMPEDANCE	- '			Z FINE GAIN (SPAN) ADJ. 17 I SEL 3 FINE GAIN (SPAN) ADJ. 18 VEXC OUT
Differential	100MΩ  47pF	•	•	4 FILTER OFFSET TRIM 19 VEXC OUT 5 FILTER OFFSET TRIM 20 SENSE HIGH (+)
Common Mode	100M\$2  47pF	•		6 BANDWIDTH ADJ. 3 21 EXC SEL 2 7 DUTPUT 2 (FILTEREC) 22 BEE OUT
INPUT VOLTAGE RANGE	4101/	•	•	BANDWIDTH ADJ. 2 23 SENSE LOW (-)
Maximum Differential Input	-104			10 RGAIN 25 REF IN
Without Damage	130V rms	•	•	11 KGAIN 28 -Vs 12 -INPUT 27 +Vs
Common Mode Voltage	±10V	•	•	13 INPUT OFFSET TRIM 28 COMMON 14 INPUT OFFSET TRIM 29 OUTPUT OFFSET TRIM
G = 1V/V, dc to 60Hz <sup>1</sup>	90dB	•	•	15 + INPUT
G = 100V/V to 2000V/V, 60Hz1	140dB min	•	•	Nota: Pins 10 thru 25 are not connected in Model 2830
dc <sup>2</sup>	90dB min (112 typ.)	·		MOUNTING CARDS
INPUT NOISE	• .			AC1211; AC1213
Voltage, G = 1000V/V	1//V n-n max	•	•	4.5(114.3)
10Hz to 100Hz <sup>2</sup>	1μV p-p	•	•	3
Current, G = 1000				
0.01Hz to 2Hz 10Hz to 100Hz <sup>2</sup>	70pA p-p 30pA rms	•	•	
PATED OUTPUT	**P:1 1018			A BO C -CI- OFFSET
Voltage, 2kΩ Load <sup>3</sup>	±10V min	•	•	29 1
Current	±5mA min	•	:	
Impedance, dc to 2Hz, G = 100V/V	0.1Ω 0.01µE max	•	•	2B30/31
	o.ospir max			
Small Signal Bandwidth			· · ·	· 16 15 次
-3dB Gain Accuracy, G = 100V/V	30kHz	•	:	1 22
G = 1000V/V	SkHz	•	•	
Full Power	15kHz	•	•	3.575 (90.81)
Settling Time, G = 100, ±10V Output				AC1011/AC1012
Step to ±0.1%	30µs	•		AC1211/AC1213
LOW PASS FILTER (Bessel)	•	•	•	CONNECTOR DESIGNATIONS
Number of Poles Gain (Pass Band)	s +1	•	•	PIN FUNCTION PIN FUNCTION
Cutoff Frequency (-3dB Point)	2Hz	•	• •	A REGULATOR +VR IN 1 EXC SEL 1
Roll-Off	60dB/decade	<b>:</b>	•	C REFOUT 3 VEXCOUT
Settling Time, G = 100V/V +10V	IJUNA	-		E 4 IEXC OUT E 5 SENSE HIGH (+)
Output Step to ±0.1%	600ms	•	•	F 6 EXC SEL 2 H 7 OUTPUT OFFSET TRIM
BRIDGE EXCITATION (See Table 1) -	Page 4			и к -Ve
POWER SUPPLY <sup>4</sup>				L +Vs 10 +Vs
Voltage, Rated Performance	±15V dc	•	•	N COMMON 12 COMMON
Voltage, Operating	±(12 to 18)V dc ±15mA	•		P R FINE GAIN ADJ. 14
TEMPERATURE DAVIOR				S FINE GAIN ADJ. 15 T FILTER OFFSET TRIM 16
Rated Performance	0 to +70°C	•	•	U FILTER OFFSET TRIM 17 V OUTPUT 2 (FILTERED) 18 Boum
Operating	-25°C to +85°C	•	•	W -INPUT 19 OUTPUT 1 (UNFILTERED)
Storage	-55°C to +125°C	•	•	Y INPUT OFFSET TRIM 20 BANDWIDTH ADJ. 1 Y INPUT OFFSET TRIM 21 BANDWIDTH ADJ. 3
CASE SIZE	2" x 2" x 0.4" (51 x 51 x 10.2mm)	• :	•	22 BANDW/DTH ADJ. 2
NOTES		1		The AC1211/AC1213 mounting card is available for
*Specifications same as 2B30J/2B31J. *Specifications referred to output at pin 7 with	h 3.75k, 1%, 25ppm/°C			2B30/2B31. The AC1211/AC1213 is an edge connect

card with pin receptacles for plugging in the 2B30/2B In addition, it has provisions for installing the gain resistors and the bridge excitation, offset adjustment ar filter cutoff programming components. The AC1211, AC1213 is provided with a Cinch 251-22-30-160 (or

equivalent) edge connector. The AC1213 includes the adjustment pots; no pots are provided with the

AC1211.

\*Specifications same as 2B30J/2B31J. \*Specifications referred to output at pin 7 with 3.75k, 1%, 23ppm/°C fine span reistor installed and internally set 2Hz filter cutoff frequency. \*Specifications referred to the unfiltered output at pin 1. \*Protected for shorts to ground and/or either supply voltage. Recommended power supply ADI model 902-20 r model 2B35 transducer power supply (for 2B30).

Specifications subject to change without notice

#### VOL. II, 9-30 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS

### Understanding the 2B30/2B31

#### FUNCTIONAL DESCRIPTION

Models 2B30 and 2B31 accept inputs from a variety of full bridge strain gage-type transducers or RTD sensors and convert the inputs to conditioned high level analog outputs. The primary transducers providing direct inputs may be  $60\Omega$  to  $1000\Omega$  strain gage bridges, four-wire RTD's or two- or threewire RTD's in the bridge configuration.

The 2B30 and 2B31 employ a multi-stage design, shown in Figure 1, to provide excellent performance and maximum versatility. The input stage is a high input impedance ( $10^8 \Omega$ ), low offset and drift, low noise differential instrumentation amplifier. The design is optimized to accurately amplify low level (mV) transducer signals riding on high common mode voltages (±10V), with wide (1-2000V/V), single resistor (R<sub>G</sub>), programmable gain to accommodate 0.5mV/V to 36mV/V transducer spans and 5 $\Omega$  to 2000 $\Omega$  RTD spans. The input stage contains protection circuitry for accidental shorts to power line voltage (130V rms) and RFI filtering circuitry.

The inverting buffer amplifier stage provides a convenient means of fine gain trim (0.8 to 1.2) by using a  $10k\Omega$  potentiometer ( $R_F$ ); the buffer also allows the output to be offset by up to  $\pm 10V$  by applying a voltage to the noninverting input (pin 29). For dynamic, high bandwidth measurements—the buffer output (pin 1) should be used.

The three-pole active filter uses a unity-gain configuration and provides low-pass Bessel-type characteristics-minimum overshoot response to step inputs and a fast rise time. The cutoff frequency (-3dB) is factory set at 2Hz, but may be increased up to 5kHz by addition of three external resistors ( $R_{SEL_1} - R_{SEL_3}$ ).

### INTERCONNECTION DIAGRAM AND SHIELDING TECHNIQUES

Figure 1 illustrates the 2B31 wiring configuration when used in a typical bridge transducer signal conditioning application. A recommended shielding and grounding technique for preserving the excellent performance characteristics of the 2B30/ 2B31 is shown.

Because models 2B30/2B31 are direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to  $1M\Omega$  resistance between signal ground and conditioner common (pin 28). The sensitive input and gain setting terminals should be shielded from noise sources for best performance, especially at high gains. To avoid ground loops, signal return or cable shield should never be grounded at more than one point.

The power supplies should be decoupled with  $1\mu$ F tantalum and 1000pF ceramic capacitors as close to the amplifier as possible.

### TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS

Models 2B30/2B31 have been conservatively specified using min-max values as well as typicals to allow the designer to develop accurate error budgets for predictable performance. The error calculations for a typical transducer application, shown in Figure 1 ( $350\Omega$  bridge, 1mV/V F.S., 10V excitation), are illustrated below.

Assumptions: 2B31L is used, G = 1000,  $\Delta T = \pm 10^{\circ}$ C, source imbalance is  $100\Omega$ , common mode noise is 0.25V (60Hz) on the ground return.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources and their effect on system accuracy (worst case) as a % of Full Scale (10V) are listed:

Error Source	Effect on Absolute Accuracy % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.0025	±0.0025
Gain Drift	±0.025	
Voltage Offset Drift	±0.05	
Offset Current Drift	±0.004	
CMR	±0.00025	±0.00025
Noise (0.01 to 2Hz)	±0.01	±0.01
Total Amplifier Error	±0.09175 max	±0.01275 max
Excitation Drift	±0.15 (±0.03 typ)	
Total Output Error (Worst Case)	±0.24175 max (±0.1 typ)	±0.0127 max

The total worst case effect on absolute accuracy over  $\pm 10^{\circ}$ C is less than  $\pm 0.25\%$  and the 2B31 is capable of 1/2 LSB resolution in a 12 bit, low input level system. Since the 2B31 is conservatively specified, a typical overall accuracy error would be lower than  $\pm 0.1\%$  of F.S.

In a computer or microprocessor based system, automatic recalibration can nullify gain and offset drifts leaving noise, nonlinearity and CMR as the only error sources. A transducer excitation drift error is frequently eliminated by a ratiometric operation with the system's A/D converter.



Figure 1. Typical Bridge Transducer Application Using 2B31

#### **BRIDGE EXCITATION (2B31)**

The bridge excitation stage of the model 2B31 is an adjustable output, short circuit protected, regulated supply with internally provided reference voltage (+7.15V). The remote sensing inputs are used in the voltage output mode to compensate for the voltage drop variations in long leads to the transducer. The regulator circuitry input (pin 24) may be connected to  $+V_S$  or some other positive dc voltage (pin 28 referenced) within specified voltage level and load current range. User-programmable constant voltage or constant current excitation mode may be used. Specifications are listed below in Table I.

NÓDEL .	2B31J	2B31K	2B31L
Constant Voltage Output Mode	-		
Regulator Input Voltage Range	+9.5V to +28V	•	•
Output Voltage Range	+4V to +15V	•	•
Regulator Input/Output Voltage			
Differential	3V to 24V	•	•
Output Current <sup>1</sup>	0 to 100mA max	•	•
Regulation, Output Voltage			
vs. Supply	0.05%/V	•	•
Load Regulation, Ir = 1mA to			
$l_r = 50 m A$	0.1%	•	
Output Voltage vs. Temperature	0.015%/°C max	•	•
(0 to +70°C)	0.003%/°C typ	•	•
Output Noise	1mV rms	•	•
Reference Voltage (Internal)	7.15V ±3%	•	•
Constant Current Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	•	· •
Output Current Range	100µA to 10mA	•	•
Compliance Voltage	0 to 10V	•	•
Load Regulation	0.1%	•	•
Temperature Coefficient		•	
(0 to +70°C)	0.003%/°C	•	•
Output Noise	1µA rms	•	•

Output Current derated to 33mA max for 24V regulator input/output voltage differential.

Table I. Bridge Excitation Specifications

#### **OPERATING INSTRUCTIONS**

Gain Setting: The differential gain, G, is determined according to the equation:

 $G = (1 + 94k\Omega/R_G) [20k\Omega/(R_F + 16.2k\Omega)]$ 

where  $R_G$  is the input stage resistor shown in Figure 1 and  $R_F$  is the variable 10k $\Omega$  resistor in the output stage. For best performance, the input stage gain should be made as large as possible, using a low temperature coefficient (10ppm/°C)  $R_G$ , and the output stage gain can then be used to make a ±20% linear gain adjustment by varying  $R_F$ .

Input Offset Adjustment: To null input offset voltage, an optional 100k $\Omega$  potentiometer connected between pins 13 and 14 (Figure 1) can be used. With gain set at the desired value, connect both inputs (pins 12 and 15) to the system common (pin 28), and adjust the 100k $\Omega$  potentiometer for zero volts at pin 3. The purpose of this adjustment is to null the internal amplifier offset and it is not intended to compensate for the transducer bridge unbalance.

**Output Offset Adjustment:** The output of the 2B30/2B31 can be intentionally offset from zero over the  $\pm 10V$  range by applying a voltage to pin 29, e.g., by using an external potentiometer or a fixed resistor. Pin 29 is normally grounded if output offsetting is not desired. The optional filter amplifier offset null capability is also provided as illustrated in Figure 1.

Filter Cutoff Frequency Programming: The low pass filter cutoff frequency may be increased from the internally set 2Hz by the addition of three external resistors connected as shown in Figure 1. The values of resistors required for a desired cutoff frequency,  $f_c$ , above 5Hz are obtained by the equation below:

$$\begin{split} &R_{SEL_1} = 11.6 \times 10^6 / (2.67 f_c - 4.34); \\ &R_{SEL_2} = 27.6 \times 10^6 / (4.12 f_c - 7) \\ &R_{SEL_3} = 1.05 \times 10^6 / (0.806 f_c - 1.3) \end{split}$$

where  $R_{SEL}$  is in ohms and  $f_c$  in Hz. Table II gives the nearest 1%  $R_{SEL}$  for several common filter cutoff (-3dB) frequencies.

f <sub>c</sub> (Hz)	R <sub>SEL1</sub> (kΩ) (Pin 1 to 9)	R <sub>SEL2</sub> (kΩ) (Pin 9 to 8)	R <sub>SEL3</sub> (kΩ) (Pin 8 to 6)
2	Open	Open	Open
5	1270.000	2050.00	383.000
10	523.000	806.00	154.000
50	90.000	137.00	26.700
100	44.200	68.10	13.300
500	8.660	13.30	2.610
1000	4.320	6.65	1.300
5000	0.866	1.33	0.261
			_

Table II. Filter Cutoff Frequency vs. RSEL

Voltage Excitation Programming: Pin connections for a constant voltage output operation are shown in Figure 2. The bridge excitation voltage,  $V_{EXC}$ , is adjusted between +4V to +15V by the 20k $\Omega$  (50ppm/°C)  $R_{VSEL}$  potentiometer. For ratiometric operation, the bridge excitation can be adjusted by applying an external positive reference to pin 25 of the 2B31. The output voltage is given by:  $V_{EXC}$  OUT =  $3.265V_{REF}$  IN. The remote sensing leads should be externally connected to the excitation leads at the transducer or jumpered as shown in Figure 2 if sensing is not required.



Figure 2. Constant Voltage Excitation Connections

Current Excitation Programming: The constant current excitation output can be adjusted between  $100\mu$ A to 10mA by two methods with the 2B31. Figure 3 shows circuit configuration for a current output with the maximum voltage developed across the sensor (compliance voltage) constrained to +5V. The value of programming resistor R<sub>ISEL</sub> may be calculated from the relationship: R<sub>ISEL</sub> = (V<sub>REG IN</sub> - V<sub>REF IN</sub>)/I<sub>EXC OUT</sub>.



Figure 3. Constant Current Excitation Connections (V<sub>COMPL</sub> = 0 to +5V)

A compliance voltage range of 0 to +10V can be obtained by connecting the 2B31 as shown in Figure 4. The  $2k\Omega$  potentiometer  $R_{ISEL}$  is adjusted for desired constant current excitation output.



Figure 4. Constant Current Excitation Connections (VCOMPL = 0 to +10V)

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### Applying the 2B30/2B31

#### APPLICATIONS

Strain Measurement: The 2B30 is shown in Figure 5 in a strain measurement system. A single active gage  $(120\Omega, GF = 2)$  is used in a bridge configuration to detect small changes in gage resistance caused by strain. The temperature compensation is provided by an equivalent dummy gage and two high precision  $120\Omega$  resistors complete the bridge. The 2B35 adjustable power supply is set to a low +3V excitation voltage to avoid the self-heating error effects of the gage and bridge elements. System calibration produces a 1V output for an input of 1000 microstrains. The filter cutoff frequency is set at 100Hz.



Figure 5. Interfacing Half-Bridge Strain Gage Circuit

**Pressure Transducer Interface:** A strain gage type pressure transducer (BLH Electronics, DHF Series) is interfaced by the 2B31 in Figure 6. The 2B31 supplies regulated excitation (+10V) to the transducer and operates at a gain of 333.3 to achieve 0-10V output for 0-10,000 p.s.i. at the pressure transducer. Bridge Balance potentiometer is used to cancel out any offset which may be present and the Fine Span potentiometer adjustment accurately sets the full scale output. Depressing the calibration check pushbutton switch shunts a system calibration resistor ( $R_{CAL}$ ) across the transducer bridge to give an instant check on system calibration.



Figure 6. Pressure Transducer Interface Application

Platinum RTD Temperature Measurement: In Figure 7 model 2B31 provides complete convenient signal conditioning in a wide range ( $-100^{\circ}$ C to  $+600^{\circ}$ C) RTD temperature measurement system. YSI - Sostman four-wire,  $100\Omega$  platinum RTD (PT139AX) is used. The four wire sensor configuration, combined with a constant current excitation and a high input impedance offered by the 2B31, eliminates measurement errors resulting from voltage drops in the lead wires. Offsetting may be provided via the 2B31's offset terminal. The gain is set by the gain resistor for a +10V output at +600°C.



Figure 7. Platinum RTD Temperature Measurement

Interfacing Three-Wire Sensors: A bridge configuration is particularly useful to provide offset in interfacing to a platinum RTD and to detect small, fractional sensor resistance changes. Lead compensation is employed, as shown in Figure 8, to maintain high measurement accuracy when the lead lengths are so long that thermal gradients along the RTD leg may cause changes in line resistance. The two completion resistors (R1, R2) in the bridge should have a good ratio tracking ( $\pm$ 5ppm/°C) to eliminate bridge error due to drift. The single resistor (R3) in series with the platinum sensor must, however, be of very high absolute stability. The adjustable excitation in the 2B31 controls the power dissipated by the RTD itself to avoid self-heating errors.



Figure 8. Three-Wire RTD Interface

Linearizing Transducer Output: To maximize overall system linearity and accuracy, some strain gage-type and RTD transducer analog outputs may require linearization. A simple circuit may be used with the 2B31 to correct for the curvature in the input signal. Consult factory for the application assistance.

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Data Acquisition System: Figure 9 shows a typical application of the 2B30/2B31 in a low level, high speed microcomputer based data acquisition system. The advantages of this configuration are improvement in CMR enhanced by a low pass filter/channel provided by the 2B31, elimination of aliasing errors and crosstalk noise between input channels, improvement in system noise and resolution, and optimized, individual bridge excitation source for each channel.



Figure 9. Use of the 2B30/2B31 in Data Acquisition System

#### PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Models 2B30/2B31 are available in three drift selections:  $\pm 0.5$ ,  $\pm 1$  and  $\pm 3\mu V/^{\circ}C$  (max, RTI, G = 1000V/V). Total input drift is composed of two sources (input and output stage drifts) and is gain dependent. Figure 10 is a graph of the worst case total voltage offset drift vs. gain for all versions.



Figure 10. Total Input Offset Drift (Worst Case) vs. Gain

Gain Nonlinearity and Noise: Nonlinearity is specified as a percent of full scale (10V), e.g. 0.25mV RTO for 0.0025%. Three maximum nonlinearity selections offered are:  $\pm 0.0025\%$ ,  $\pm 0.005\%$  and  $\pm 0.01\%$  (G = 1 to 2000V/V). Models 2B30/2B31 offer also an excellent voltage noise performance by guaranteeing maximum RTI noise of 1 $\mu$ V p-p (G = 1000V/V, R<sub>S</sub>  $\leq$  $5k\Omega$ ) with noise bandwidth reduced to 2Hz by the low pass filter.

Low Pass Filter: The three pole Bessel-type active filter attenuates unwanted high-frequency components of the input signal above its cutoff frequency (-3dB) with 60dB/decade rolloff. With a 2Hz filter, attenuation of 70dB at 60Hz is obtained, settling time is 600ms to 0.1% of final value with less than 1% overshoot response to step inputs. Figure 11 shows the filter response.



Figure 11. Filter Amplitude Response vs. Frequency

Common Mode Rejection: CMR is rated at  $\pm 10V$  CMV and  $1k\Omega$  source imbalance. The CMR improves with increasing gain. As a function of frequency, the CMR performance is enhanced by the incorporation of low pass filtering, adding to the 90dB minimum rejection ratio of the instrumentation amplifier. The effective CMR at 60Hz at the output of the filter ( $f_c = 2Hz$ ) is 140dB min. Figure 12 illustrates a typical CMR vs. Frequency and Gain.



Figure 12. Common Mode Rejection vs. Frequency and Gain

Bridge Excitation (2B31): The adjustable bridge excitation is specified to operate over a wide regulator input voltage range (+9.5V to +28V). However, the maximum load current is a function of the regulator circuit input-output differential voltage, as shown in Figure 13. Voltage output is short circuit protected and its temperature coefficient is  $\pm 0.015\% \text{ V}_{OUT}$ /°C max ( $\pm 0.003\%$ /°C typ). Output temperature stability is directly dependent on a temperature coefficient of a reference and for higher stability requirements, a precision external reference may be used.



Figure 13. Maximum Load Current vs. Regulator Input-Output Voltage Differential

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### **ANALOG** DEVICES

### Four Channel RTD/Strain Gage Conditioner

## MODEL 2B34

#### **FEATURES**

Low Input Offset Drift: ±1.0µV/°C Low Gain Drift: ±25ppm/°C Low Nonlinearity: ±0.01% max (±0.005% typ) Differential Input Protection: ±130V rms Channel Multiplexing: 3000 chan/sec Scanning Speed Solid State Reliability Internal RTD Excitation/Lead Wire Compensation

#### APPLICATIONS

Multichannel Signal Conditioning Data Acquisition Industrial Process Monitoring



#### GENERAL DESCRIPTION

The model 2B34 is a four channel signal conditioner providing input protection, multiplexing, and amplification in a single, low cost package. A multi-purpose device, the 2B34 is designed to effectively condition low level signals ( $\pm 30$ mV to  $\pm 100$ mV) such as those produced by RTD and strain gage sensors. The superior design of the 2B34 provides low input drift ( $\pm 1.0\mu$ V/°C), high common mode rejection (94dB @ 60Hz), and extremely stable gain ( $\pm 25$ pm/°C). Other features include low nonlinearity ( $\pm 0.01\%$  max), excitation and lead wire compensation for RTD inputs, and a wide operating temperature range ( $-25^{\circ}$ C to  $+85^{\circ}$ C).

#### APPLICATIONS

The 2B34 is a superior alternative to the relay multiplexing technique used in multichannel data acquisition systems, computer interface systems, and measurement and control instrumentation. Advantages over relay circuits include functional versatility, superior signal conditioning, and solid state speed and reliability.

#### DESIGN FEATURES AND USER BENEFITS

Solid State Design: Complete solid state construction offers both high performance and reliability.

Ease of Use: The multichannel, functionally complete design in a compact  $(2'' \times 4'' \times 0.4'')$  module, conserves board space and eliminates the need for a number of discrete components that would otherwise be required.

Low Cost: The 2B34 offers the lowest cost per channel for solid state, low level sensor signal conditioning.

Wide Operating Temperature Range: The 2B34 has been designed to operate over  $-25^{\circ}$ C to  $+85^{\circ}$ C ambient temperature range.

#### **FUNCTIONAL DESCRIPTION**

The internal structure of the 2B34 is shown in Figure 1. Four individual input channels are multiplexed into a single, low



Figure 1. 2B34 Functional Diagram

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# **SPECIFICATIONS** (typical @ +25°C, V<sub>S</sub> = ±15V, unless otherwise noted)

Model	2B34J			
Model	Strain Gage Mode	RTD Mode		
ANALOG INPUT				
Number of Channels	4	•		
Input Range	±30mV & ±100mV	25-175Ω & 0-350Ω		
Gain Range ( $R_G = 945\Omega$ )	166.6V/V & 50V/V	•		
Expanded <sup>1</sup>	50V/V to 1000V/V	•		
Transfer Function	N/A	$V_{OUT} = [0.4 \times 10^{-3} \times (R_{RTD}) - 0.04] G$		
Gain Error	±0.6% max (G = 50) ±0.8% max (G = 166.6)	•		
Gain Temperature Coefficient <sup>2</sup>	±25ppm/°C	•		
Gain Nonlinearity	±0.01% of Span, max	•		
Offset Voltage				
Input Offset, Initial <sup>3</sup> (Adj. to Zero)	±150µV	•		
vs. Temperature	±1µV/°C	±0.015 deg/deg		
Channel to Channel Offset	±25μV	•		
Total Offset Drift (RTI)	±1µV/°C	•		
Input Noise Voltage				
$0.01$ Hz-100Hz, Rs = 1k $\Omega$	1.5µV p-p	•		
Common Mode Voltage	±6V	N/A		
Common Mode Rejection				
$R_s = 100\Omega$ , $f = 60Hz$	94dB (@ G = 166.6)	N/A		
$B_c = 1k\Omega$ f = 60Hz	86dB (@ G = 166.6)			
Maximum Safe Differential Input (10 min)	130V rms	•		
Normal Mode Rejection @ 6047	24dB	•		
Inout Resistance	2000	•		
Input Resistance	10n4 max	•		
Land Resistance Effect	N/A	+0.03 deg/Q		
Lead Resistance Effect	N/A			
ANALOG OUTPUT		-		
Output Voltage Swing	±5V @ 1mA	-		
Output Resistance				
Direct Output	0.152	•		
Switched Output	35Ω, +0.5%/°C	•		
Maximum Switched Voltage	±9V, no load	•		
SENSOR EXCITATION				
Excitation Level (per channel)	NA	0.4mA ±1%		
•		(±1.7% max)		
vs. Temperature	NA	±10ppm/°C		
CHANNEL SELECTION				
Channel Selection Time to ±0.01% E S	30000	•		
Channel Scanning Speed	>3000 chan/sec	•		
Channel Scanning Speed	> 5000 chair sec	· · · · · · · · · · · · · · · · · · ·		
DYNAMIC RESPONSE		. •		
Input Settling Time to ±0.01% F.S.	0.4 sec			
Bandwidth	4Hz			
POWER SUPPLY				
Voltage, ±Vs, Rated Performance	±15V dc ±5%	•		
Current	+35mA, -15mA, max	•		
Supply Effect on Offset	±0.003%/%	±0.02%/%		
ENVIRONMENTAL				
ENVIKUNMENTAL				
I emperature	0			
Rated Performance	U to +70 C			
Operating	-25 C to +85 C	•		
Storage	-55 C to +85 C			
CASE SIZE	2" × 4" × 0.4"			

NOTES <sup>1</sup>Gain range may be expanded by use of external amplifier as shown in Figure 3. <sup>3</sup>Does not include effects of sensor excitation drift.

<sup>3</sup>With no induced offset, using circuit shown in Figure 2 (pots centered). \*Specifications same as Strain Gage Mode.

Specifications subject to change without notice.

# - 2.01 (51.1) MAX ŧ 0.41 (10.4) MAX 0.02 (0.5) MAX - 0.2 (5.1) MAX 4.02 (102.1) MAX

**OUTLINE DIMENSIONS** Dimensions shown in inches and (mm).

#### **2B34 PIN DESIGNATIONS**

NOTE: TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS

0.1 (2.54) GRID

вот TOM VIEW

PIN	FUNCTION	PIN	FUNCTION	*******
1	NC	37	н	
2		38		
3	SW'D OUTPUT ENABLE	39	R <sub>G</sub> /OFS	
- 4	SW'D OUTPUT	40	Rg	CHANNEL A
5		41	LO	
· 6	DIRECT OUTPUT	42	сом	
7	SW'D INPUT	43	Vors (+10V)	)
8		44		
9	OUTPUT OFFSET	45		
10		46		
11	-15V	47	н	<u>۱</u>
12	ANA COM	48		
13	+15V	49	R <sub>G</sub> /OFS	
14		50	RG	CHANNEL B
15		51	LO	
16		52	сом	
17		53	Vors (+10V)-	<u> </u>
18		54		
19		55		
20		56	н	)
21		57		
22	ADR1 \ CHANNEL	58	R <sub>G</sub> /OFS	L
23	ADRO J SELECT	59	Rg	CHANNEL C
24	GAIN SELECT	60	LO	
25	RTD ENABLE	61	СОМ	· .
26		62	Vors (+10V)	/
27		63		
28		64		
29		65		
30		66	ні	<u> </u>
31	DIGCOM	67		
32	SYNCIN 2	68	R <sub>G</sub> /OFS	
33	SYNC OUT J	69	Rg	CHANNEL D
34		70	LO	
35		71	сом	· · ·
36		72	Vors (+10V)*	,

\*SHORTED INTERNALLY FOR FEEDTHROUGH FOR 2854/55 MODELS

drift differential instrumentation amplifier, with the desired channel specified by the two digital channel select inputs. This signal is then fed to a digitally controlled programmable gain amplifier (PGA). The appropriate gain for a particular sensor type is selected by the gain select input.

User selectable direct or switched output permits direct output connection of several modules, should more than four channels be required.

An internally selectable constant current excitation source provides direct connection of 2 or 3 wire RTDs, thus eliminating the need for external excitation sources. Each channel contains an input protection and filtering network to preserve signal integrity in the presence of series mode 50/60Hz noise.

#### **OPERATING INSTRUCTIONS**

Connection of the 2B34 with three wire RTD inputs is shown in Figure 2 and will be all that is needed in most cases. The following sections describe the basic application, as well as detail some optional connections that enhance the module's performance in more complex applications. All unused inputs should be shorted to common.



Figure 2. Basic RTD Application

**Channel Selection:** Each channel of the 2B34 is turned on and off by applying the proper binary code to channel select inputs (ADR0, ADR1). Channels may be selected in any order and there are no restrictions on rate other than the  $300\mu s$ settling time for access to a channel (Table I, channel select truth table).

Gain Selection: The 2B34 is designed to provide signal conditioning of both RTD and strain gage sensor inputs. To accommodate both of these sensor types, the 2B34 is precali-

AD1	AD0	Channel
0	0	Α
0	1	В
1	0	С
1	1	D

#### Table I. Channel Selection

brated to provide gains of 50 and 166.6, with gain components shown in Figure 2. This provides proper amplification of input signals over the span of  $\pm 30$ mV to  $\pm 100$ mV. Selection of the desired gain and sensor input mode is achieved by applying the appropriate binary codes shown in Table II. A 200 $\Omega$  pot provides  $\pm 3\%$  full scale span adjustment.

(Pin 24) Gain Select Input	Selected Gain
0	166,6
1	50
(Pin 25)	1.
<b>RTD ENABLE</b>	Selected Mode
. 0	RTD
1	Strain Gage

#### Table II. Gain and Mode Selection

Zero Suppression & Gain: In most instances, the gain capability of the 2B34 will be sufficient. However, in the case of input signals that may require gains greater than 166, the



Figure 3. Zero Suppressed Switched Output RTD Application gain range of the 2B34 may be supplemented by use of an external amplifier (Figure 3). A low drift, operational amplifier (such as the AD741K) should be used to maintain signal integrity.

**Optional Offset Adjustment:** All channels of the 2B34 are typically within  $\pm 150\mu V$  (RTI) offset. For use in more demanding applications, the module has provisions for fine adjustment of the input offset (RTI) of each input as well as the output offset (RTO) of the entire module. None of the offset adjustments will affect drift performance.

In some applications, where  $\pm 25\mu V$  channel-to-channel offset voltage can be tolerated, adjustment of only the output offset will be sufficient. The offset circuit shown in Figure 2 (for channel "A") is required when a potentiometer is not used to adjust input offset. The output offset adjustment may then be used to null the  $150\mu V$  (RTI) offset, leaving an offset difference between channels of  $\pm 25\mu V$ . If input offset adjustment is desired, the input offset circuitry shown in Figure 3 should be used. This provides approximately  $\pm 140m V$  (RTO) of adjustment, and should be adequate, in most cases, for elimination of sensor offset errors.

To calibrate in the mV (strain gage) mode, (Figure 3), short the signal inputs (for example, pins 66, 70 for channel "D") to common and center the input offset adjustment potentiometer. Adjust the output offset potentiometer until the output is nulled for that channel at the appropriate gain. The input offset pots on each channel may then be used to eliminate any errors on subsequent channels that are selected.

To calibrate in the RTD mode, follow the same procedure, but replace the short with a  $100\Omega$  resistance standard.

Channel Expansion: The 2B34 has provisions for directly interconnecting several modules when more than four channels are required. The series switched outputs of the modules are connected together, the channel select inputs are driven in parallel, and the switched output of the desired module is selected using the ENABLE pin. This technique is shown in Figure 4. Channel address and ENABLE (active low) inputs are CMOS/ TTL compatible with an input current of 100 $\mu$ A each.



Figure 4. Channel Expansion

2B34 Strain Gage Application: Figure 5 shows a four channel strain gage input system utilizing the multiplexing feature of the 2B34. Input offset and gain adjustments are used to eliminate inherent sensor errors. The model 2B35 triple output supply may be used to provide power for the 2B34 as well as excitation for the strain gage sensors.







# 

# Precision, Triple Output Transducer Power Supply

MODEL 2B35

#### FEATURES

Resistor Programmable Voltage or Current Output Voltage: +1V dc to +15V dc @ 125mA max Current: 100μA to 10mA (V<sub>COMPL</sub> = +10V) Dual Fixed Output: ±15V dc @ ±65mA max Excellent Regulation: Line ±0.01% max; Load ±0.02% max Low Drift: 0.006%/<sup>°</sup>C max (2B35K) No Derating Over -25<sup>°</sup>C to +71<sup>°</sup>C Operating Range

#### APPLICATIONS

Measurement and Control Instruments and Systems Excitation Source For:

Strain Gages, Pressure Transducers, Load Cells, Torque Transducers, RTD's



#### **GENERAL DESCRIPTION**

The 2B35 is a triple output modular power supply designed to provide regulated excitation to a wide variety of transducers as well as  $\pm 15V$  power for amplifiers and other analog circuits of an instrumentation system. The single-resistor programmable transducer excitation output may be operated in two modes: constant voltage, providing a +1V to +15V output or a constant current, adjustable from 100 $\mu$ A to 10mA.

The programmable output in the voltage mode features current rating of 0 to 125mA, suitable to excite four  $350\Omega$  transducers at 10V. Current limiting protects the output against accidental overload and remote sensing corrects for the transducer cable resistance variations. In the constant current mode, externally set  $100\mu$ A to 10mA output offers a 0 to +10V compliance voltage range. The ±15V outputs feature 0.5% tracking accuracy and current rating of 0 to ±65mA max.

Two accuracy selections are available offering guaranteed low temperature coefficient; 2B35K: 0.006%/°C max and 2B35J: 0.05%/°C max. Line and load regulation are also guaranteed; 2B35K: 0.01% and 0.02%, and 2B35J: 0.08% and 0.1%, max, respectively.

#### APPLICATIONS

The 2B35 is designed for ac powered signal conditioning instrumentation applications used for data acquisition, control, indication or recording. This compact module may be applied as a power source for the model 2B30 strain gage transducer/ RTD signal conditioner in a high accuracy transducer interface application. Some typical applications involve strain gages for stress/strain measurements, pressure transducers, load cells, torque transducers and RTD's.

#### OPERATION

Figure 1 illustrates operation of the 2B35K providing an adjustable voltage output and dual 15V dc outputs. The resistor programmable output (+V<sub>OUT</sub>) is set between +1V to +15V by the R<sub>TRIM</sub>. R<sub>TRIM</sub> may be determined by using either the table shown in Figure 1 or the graph shown in Figure 2. For example, to provide an adjustable range from +1V to +6V, R<sub>TRIM</sub> should be a 5k $\Omega$  pot.

The remote sensing inputs (pins 5 and 8) are connected at the transducer (load) to the voltage output (SENSE HIGH to +V<sub>OUT</sub> and SENSE LOW to COMMON).



Figure 1. Model 2B35K Connection Diagram for Dual 15V dc and Adjustable +1V to +15V Output

For optional input voltage ranges, see note 1, next page.

### **SPECIFICATIONS**

(typical @ +25°C and 115V ac 60Hz unless otherwise noted)

Model	2B35J	2B35K
INPUT		
Input Voltage Range <sup>1</sup>	105V ac to 125V ac	•
Input Frequency Range	50Hz to 400Hz	•
ADJUSTABLE OUTPUT		
Voltage Mode		
Output Voltage Range	+1V to +15V dc	•
Output Voltage Stability		
vs. Temperature – % V <sub>OUT</sub> /°C max	±0.05	±0.006
vs. Time – % V <sub>OUT</sub> /month	±0.01	•
Output Current (-25°C to +71°C) <sup>2</sup>	0 to 125mA max	•
Output Impedance – @ dc, max	0.1Ω	•
Noise and Ripple (dc to 1MHz) – mV p-p max	1	•
- mV rms max	0.25	•
Regulation		
Line (full range) - % Vour max	±0.08	±0.01
Load (no load to full load) - % Vour max	±0.1	±0.02
Remote Sensing Impedance	30kΩ	•
Short Circuit Current Limit <sup>3</sup> (-25°C to +71°C)	200mA	•
Current Mode		
Output Current Range	100µA to 10mA	•
Output Current Stability		
vs. Temperature $-\%$ lour/°C max	±0.05	±0.006
vs. Time – % lour/month	±0.01	•
Compliance Voltage Range	0 to +10V	•
Noise and Ripple (dc to $1 \text{MHz}$ ) $-\mu \text{A p-p}$	0.1	•
Line Regulation (full range) - % IOUT max	±0.08	±0.01
DUAL FIXED OUTPUTS		
Output Voltage	±15V dc	•
Voltage Error – mV max	-0. +300	٠
Accuracy Tracking (-15V Ref to +15V) - % max	±0.5	•
Stability vs. Temperature $-\%/^{\circ}C$ max	±0.02	±0.006
Output Current <sup>4</sup>	0 to ±65mA max	*
Output Impedance – @ dc. max	0.1Ω	•
Noise and Ripple (dc to $1MHz$ ) – mV p-p	1	•
- mV rms	0.25	•
Regulation		
Line (full range) – % max	±0.08	±0.01
Load (no load to full load) - % max	±0.1	±0.02
Short Circuit Current Limit <sup>3</sup> (-25°C to +71°C)	±180mA	•
INPUT TO OUTPUT ISOLATION		
Breakdown Voltage - Continuous ac or de	±500V pk max	•
Isolation Resistance	50MΩ	•
TEMPERATURE RANGE		
Operating, Rated Performance	-25°C to +71°C	
Storage	-25 C to +85 C	
MECHANICAL	•	
Case Dimensions – Inches	2.5 x 3.5 x 1.25	
Weight – Grams	550	•.
Mating Socket	AC1212	•

NOTES

\*Specifications same as model 2B35J.

<sup>1</sup>Optional input voltage ranges: "E" Option; 205-240V ac, 50 to 400Hz "F" Option; 90-110V ac, 50 to 400Hz "H" Option; 220-260V ac, 50 to 400Hz

Order option desired as a suffix to model number.

<sup>2</sup>Maximum output current available over the entire output voltage and temperature range without derating.

<sup>3</sup>Output protected for continuous short circuit over the temperature range. <sup>4</sup>Unbalanced load operation is permissible for any combination of +10 and

Hol which does not exceed a total of 130mA.

Specifications subject to change without notice.



RTRIM - Ohms

Figure 2. Voltage Output vs. RTRIM

ADJ USTABLE CURRENT OUTPUT WITH DUAL 15V dc OUTPUTS Pin connections to provide dual 15V dc and a constant current output are shown in Figure 3. The current output is adjusted from 100 $\mu$ A to 10mA via R<sub>TRIM</sub>. The value of programming resistor R<sub>TRIM</sub> may be calculated from the relationship: R<sub>TRIM</sub> = 2.46/I<sub>OUT</sub> where R<sub>TRIM</sub> is in k\Omega and I<sub>OUT</sub> in mA.



Figure 3. Model 2B35 Connection Diagram to Provide Dual 15V dc and Adjustable 100µA to 10mA Current Output

# 

## Isolated, Thermocouple Signal Conditioner

## MODEL 2B50

#### FEATURES

Accepts J, K, T, E, R, S or B Thermocouple Types Internally Provided Cold Junction Compensation High CMV Isolation:  $\pm 1500V \text{ pk}$ High CMR: 160dB min @ 60Hz Low Drift:  $\pm 1\mu V/^{\circ}$  C max (2B50B) High Linearity:  $\pm 0.01\%$  max (2B50B) Input Protection and Filtering Screw Terminal Input Connections

#### APPLICATIONS

Precision Thermocouple Signal Conditioning For: Process Control and Monitoring Industrial Automation Energy Management Data Acquisition Systems

#### GENERAL DESCRIPTION

The model 2B50 is a high performance thermocouple signal conditioner providing input protection, isolation and common mode rejection, amplification, filtering and integral cold junction compensation in a single, compact package.

The 2B50 has been designed to condition low level analog signals, such as those produced by thermocouples, in the presence of high common mode voltages. Featuring direct thermocouple connection via screw terminals and internally provided reference junction temperature sensor, the 2B50 may be jumper programmed to provide cold junction compensation for thermocouple types J, K, T, and B, or resistor programmed for types E, R, and S.

The high performance of the 2B50 is accomplished by the use of reliable transformer isolation techniques. This assures complete input to output galvanic isolation ( $\pm 1500V$  pk) and excellent common mode rejection (160dB @ 60Hz).

Other key features include: input protection (220V rms), filtering (NMR of 70dB @ 60Hz), low drift amplification  $(\pm 1\mu V)^{\circ}$ C max – 2B50B), and high linearity ( $\pm 0.01\%$  max – 2B50B).

#### APPLICATIONS

The 2B50 has been designed to provide thermocouple signal conditioning in data acquisition systems, computer interface systems, and temperature measurement and control instrumentation.



In thermocouple temperature measurement applications, outstanding features such as low drift, high noise rejection, and 1500V isolation make the 2B50 an ideal choice for systems used in harsh industrial environments.

#### **DESIGN FEATURES AND USER BENEFITS**

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, the 2B50 has been conservatively designed to meet the IEEE Standard for transient voltage protection (472-1974: SWC) and provide 220V rms differential input protection.

High Noise Rejection: The 2B50 features internal filtering circuitry for elimination of errors caused by RFI/EMI, series mode noise, and 50Hz/60Hz pickup.

Ease of Use: Internal compensation enables the 2B50 to be used with seven different thermocouple types. Unique circuitry offers a choice of internal or remote reference junction temperature sensing. Thermocouple connections may be made either by screw terminals or, in applications requiring PC Board connections, by terminal pins.

Small Package:  $1.5'' \times 2.5'' \times 0.6''$  size conserves board space.

# **SPECIFICATIONS** (typical @ +25°C and VS = ±15V unless otherwise noted)

MODEL	2B50A	2B50B	OUTLINE DIMENSIONS
NPUT SPECIFICATIONS			Dimensions shown in inches and (mm).
Thermocouple Types	· · · · · · · · · · · · · · · · · · ·		
Jumper Configurable Compensation	J, K, T, or B	•	
Resistor Configurable Compensation	R, S, or E	*	DEVICES
Input Span Range	±5mV to ±100mV	•	81-
Gain Range	50V/V to 1000V/V	•	1.51 (38.35) <b>72</b> 56 <b>8</b>
Gain Equation	$1 + (200 k \Omega / R_G)$	•	
Gain Error	±0.25%	•	ISOLATED THERMOCOUPLE
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max	MADE IN USA
Gain Nonlinearity <sup>1</sup>	±0.025% max	±0.01% max	
Offset Voltage			
Input Offset (Adjustable to Zero)	±50μV	+	0.00 (5.00)
vs. Temperature	$\pm 2.5 \mu V /^{\circ} C max$	±1µV/°C max	
vs. Time	±1.5µV/month	•	
Output Offset (Adjustable to Zero)	±10mV	•	
vs. Temperature	±30μV/°C	+	
Total Offset Drift	$\pm (2.5 + \frac{30}{C}) \mu V/^{\circ}C$	$\pm \left(1 + \frac{30}{G}\right) \mu V/^{\circ}C$	
Input Noise Voltage	( 3)	( G/	
$0.01$ Hz to 100 Hz. Rs = 1k $\Omega$	1µV p-p	•	0.020 (0.508)
Maximum Safe Differential Input Voltage	220V rms. Continuous	•	DIA
CMV. Input to Output	· · · · · · · · · · · · · · · · · · ·		
Continuous, ac or de	±1500V pk max	•	0.605
Common Mode Rejection	1		(15.36)
@ 60Hz, 1k $\Omega$ Source Unbalance	160dB min	•	
Normal Mode Rejection @ 60Hz	70dB min	- <b>14</b> - 17	
Bandwidth	dc to 2.5Hz (-3dB)	•	
Input Impedance	100ΜΩ	•	
Input Bias Current <sup>2</sup>	±5nA	*	
Open Input Detection	Downscale	•	
Response Time <sup>3</sup> , $G = 250$	1.4sec	+	
Cold Junction Compensation			
Initial Accuracy <sup>4</sup>	±0.5°C	*	BOTTOM VIEW 0.100 (2.54) GRID WEIGHT: 45 G TYP
vs. Temperature <sup>5</sup> (+5°C to +45°C)	±0.01°C/°C	•	NOTE: TERMINAL PINS INSTALLED ONLY IN
DUTPUT SPECIFICATIONS			
Output Voltage Range <sup>6</sup>	±5V @ ±2mA	*	PIN DESIGNATIONS
Output Resistance	0,1Ω	*	
Output Protection	Continuous Short to Ground	•	PIN FUNCTION PIN FUNCTION
POWER SUPPLY			2 INPUT HI 24
Voltage			<u>4</u> <u>26</u>
Output $\pm V_S$ (Rated Performance)	±15V dc ±10% @ ±0.5mA	•	5 R <sub>G</sub> /COM 27 6 28 +V OSC
(Operating)	±12V to ±18V dc max	•	7 29 OSC COM 8 +V ISO OUT 30
Oscillator +VOSC (Rated Performance)	+13V to +18V @ 15mA	•	9 -V ISO OUT 31 10 32
ENVIRONMENTAL			11 <u>33</u> 12 34
Temperature Range Rated Performance	$0 to +70^{\circ}C$	•	13 35
Operating	$-25^{\circ}$ C to $+85^{\circ}$ C	•	15 OUTPUT OFFSET 37
Storage Temperature Range	$-55^{\circ}C$ to $+85^{\circ}C$	•	16 OUTPUT SCALE 39 OPEN INPUT DET.
DEI Effect (5W @ 470MHz @ 3ft)			17 OUTPUT 40 X 18 41 K, T TYPE PROCRAMMING
Frior	+0.5% of Span	•	19 OUTPUT COM 42 J J PROGRAMMING 20 +Vs 43 CJC SENSOR IN
			21 -Vs 44 CJC SENSOR OUT
PHYSICAL	1 =" > 2 =" > 0 <"	•	
Lase Size	1.3 × 2.3 × 0.0		MATING SUCKET:
			A/1/18

NOTES

\*Specifications same as 2B50A.

Specifications same as 2B50A.
Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line; e.g., nonlinearity at an output span of 10V pk-pk (±5V) is ±0.01% or ±1mV.
Does not include open circuit detection current of 20nA (optional by jumper connection).
Open input response time is dependent upon gain.
When used with internally provided CJC sensor.
Compensation error contributed by ambient temperature changes at the module.
Output swing of ±10V may be obtained through output scaling (Figure 5).

Specifications subject to change without notice.

### Applying the 2B50

#### **FUNCTIONAL DESCRIPTION**

The internal structure of the 2B50 is shown in Figure 1. An input filtering and protection network precedes a low drift, high performance amplifier whose gain is set by a user supplied resistor ( $R_G$ ) for gains of 50 to 1000V/V. Isolated power is brought out to permit convenient adjustment of the input offset voltage, if desired.



Figure 1. 2B50 Functional Block Diagram

Internal circuitry provides reference junction compensation. An integral reference junction sensor is provided for direct thermocouple connections, or an external reference sensor (2N2222 transistor) may be used in applications having remote thermocouple termination. Compensating networks for thermocouple types J, K, and T are built into the 2B50. A fourth compensation (X) may be programmed with a single resistor for any other thermocouple type. The 2B50 can be programmed for uncompensated output when used with inputs other than thermocouples.

Transformer coupling is used to achieve stable, reliable input to output galvanic isolation, as well as elimination of ground loop error effects.

Normally, the full scale output of the 2B50 is  $\pm 5V$ . However, with the addition of an external resistive divider, the output buffer amplifier may be scaled for a gain of up to 2, providing a full scale output swing of  $\pm 10V$ .

#### **OPERATING INSTRUCTIONS**

The connections shown in Figure 2 are common to most applications using the 2B50, and, in many cases, will be all that is required.



Figure 2. Basic 2B50 Application

Two sets of parallel thermocouple input connections are provided. The thermocouple input may be connected by screw terminals (Input +, Input -) or to terminal pins 1 (-) and 2 (+) in cases where thermocouples are to be remotely terminated. The following sections describe a basic thermocouple application, as well as detail some optional connections to enhance performance in more demanding applications. Jumper A (Figure 2) is used to disconnect cold junction compensation circuitry during offset adjustments.

#### INTERCONNECTION GUIDELINES

All power supply inputs should be decoupled with  $1\mu$ F capacitors as close to the unit as possible. Any jumpers installed for programming purposes should also be installed as close as possible to minimize noise pickup effects.

Since the oscillator section of the 2B50 accounts for most of the power consumption but can accept a wide range of voltages (+13V to +18V), it may be desirable to power this section from a convenient source of unregulated power.

If the same supply is to be used for both amplifier and oscillator circuitry, the power supply returns should be brought out separately so that oscillator power supply currents do not flow in the low lead of the signal output. In either case, a  $1\mu$ F capacitor must be connected from +V<sub>OSC</sub> (Pin 28) to Oscillator COM (Pin 29).

The oscillator and amplifier sections are completely isolated; therefore, a dc power return path is not required between the two power supply commons.

#### GAIN SETTING

The gain of the 2B50 is set by a user-supplied resistor ( $R_G$ ) connected as shown in Figure 2. Gain will normally be selected so that the maximum output of the signal source will result in a plus full scale output swing. The resistor value required is determined by the equation:  $R_G = 200k\Omega/(G-1)$ .

A series trim on the gain setting resistor can be used to trim out the resistor tolerance and module gain error (Figure 3). Since addition of a series resistance will always decrease gain, the value of the gain-setting resistor should be selected to provide a gain somewhat higher than the desired trimmed gain. A good quality (e.g., 10ppm/°C), metal-film resistor should be used for R<sub>G</sub>, since drift of R<sub>G</sub> will add to the overall gain drift of the 2B50. A cermet pot is suitable for the trim. Note that a minimum gain of 50 is required for guaranteed operation.



#### Figure 3. Gain Adjustment

#### INPUT AND OUTPUT OFFSET ADJUSTMENTS

The 2B50 has provisions for adjusting input and output offset errors of the module. None of the offset adjustments will affect drift performance, and adjustments need not be used unless the particular application calls for lower offsets than those specified.

Connections for offset adjustments are shown in Figure 4. Isolated supply voltages are brought out for input trimming convenience only and are not for use as a power supply for external components.



Figure 4. (A) Input and (B) Output Offset Adjustment

#### **OFFSET CALIBRATION**

- 1. Short Input + and Input together.
- 2. Disconnect cold junction compensation circuitry by removing Jumper "A" (Figure 2).
- 3. Adjust input offset trim pot (±250µV range, RTI) to zero output while operating at the desired gain. In most
- applications, adjustment of the input offset alone will be sufficient. Output offset adjustment (±30mV range) may be performed if it is desired to adjust output offset on the nonisolated side.

#### **OPEN INPUT DETECTION**

Connecting the open input detection pin (PIN 39) to input high (PIN 2) creates a 20nA bias current which will provide a negative overscale response if the input is opened, or in case of thermocouple "burn out". The speed at which this occurs is dependent on gain, with a typical response time of 1.4sec @ G = 250.

#### **OUTPUT SCALING**

With the output scale (PIN 16) connected to the output (PIN 17), the full scale output range is  $\pm 5V$  and the total gain is equal to the gain set by  $R_G$ . For applications requiring a full scale output of  $\pm 10V$ , a resistive divider may be connected to provide a gain of 2 at the output amplifier (see Figure 5). In this configuration, total gain will be twice the gain set by  $R_G$ . Output gains greater than 2 cannot be used.



Figure 5. Output Scaling Connections

#### COLD JUNCTION COMPENSATION

The 2B50 may be programmed to provide cold junction compensation for types J, K and T thermocouples by connecting a jumper from input low (PIN 1) to the appropriate programming points (PIN 42 for J, PIN 41 for K or T). To compensate other thermocouple types, a resistor ( $R_X$ ) is connected from the "X" programming point (PIN 40) to Input Low (PIN 1). Table I shows the appropriate  $R_X$  values for types E, R, and S.  $R_X$  should be a 50ppm/°C, 1% tolerance resistor. Type B thermocouples are unique, in that they have almost no output in the  $+5^{\circ}$ C to  $+45^{\circ}$ C range, and, therefore, do not require cold junction compensation at all. To accommodate a type B thermocouple, resistor  $R_X$  must be left open. Error due to cold junction temperature will be less than  $\pm 1^{\circ}$ C for any measurement above 260°C. In the measurement range above 1000°C (where type B thermocouples are normally used) the error will be less than  $\pm 0.3^{\circ}$ C.

<b>Т</b> уре	$R_X$ (k $\Omega$ )
E	1.87
R,S	19.6
В	Open

Table I. Compensation Values for Thermocouple Types E, R, S and B

#### **REMOTE REFERENCE SENSING**

In applications requiring termination of thermocouple leads at a point located remotely from the 2B50, with connections brought to the 2B50 (PINS 1,2) by copper wires, reference temperature sensing at the remote location will be necessary. The 2B50 has provisions for connection of a 2N2222 transistor (metal can version) for use as a reference junction sensor. The connections are shown in Figure 6. The remote sensing transistor is calibrated by adjusting  $R_{CAL}$  to obtain the value of  $V_{CAL}$  as specified in Table II.

(Example:  $V_{CAL} = 570.0 \text{ mV} @ 25^{\circ}C$ )



Figure 6. Remote Reference Junction Sensing

V <sub>CAL</sub> (mV)
616.5
604.9
593.3
581.6
570.0
558.4
546.8
535.1
523.5

(Values may be interpolated)

#### Table II. Calibration Voltages vs. Sensor Temperature

Proper sensor placement is important. Close thermal contact of the sensor and thermocouple termination point (reference junction) is essential for accurate operation of the 2B50. The sensor may be placed any distance from the 2B50. When the sensor leads are more than ten feet long, or in the presence of strong noise signal sources, shielded cable should be used.

# 

# Two-Wire, Thermocouple Temperature Transmitters

## MODELS 2B52 and 2B53

#### FEATURES

Accept Type J, K or T Thermocouple Inputs Compatible with Standard 4–20mA Loops High Accuracy: ±0.1% High CMV Isolation: 600V rms; CMR = 160dB (2B52) High Noise Rejection and RFI Immunity Internal Cold Junction Compensation Open Thermocouple Detection Millivolt Signal Transmission Low Cost, FM Approved (2B52)

#### APPLICATIONS

Thermocouple Temperature Monitoring and Control In: Process Control Factory Automation

Energy Management

#### **GENERAL DESCRIPTION**

Models 2B52 and 2B53 are high performance, low cost temperature transmitters designed to accept a thermocouple input from types J, K or T and produce a standard 4–20mA output current proportional to the measured temperature.

Two basic models are available. The 2B52 features high input to output isolation (600V rms) and high CMR (160dB @ 60H2). The 2B53 offers a functionally equivalent design without input to output isolation. Both models were designed to operate as two-wire transmitters and are compatible with standard 4–20mA loops. The 2B52 is approved by Factory Mutual for intrinsically safe use in hazardous locations.

The 2B52 and 2B53 offer high noise rejection, RFI immunity and automatic cold junction compensation to assure accurate operation in noisy industrial environments over a wide ambient temperature range. Other features include open thermocouple detection, fast response time and a low bias current to minimize errors induced by thermocouple extension wires.

A rugged metal enclosure, suitable for field mounting, offers environmental protection and screw terminal input and output connections. This enclosure may be either surface or standard relay track mounted.

#### APPLICATIONS

The 2B52 and 2B53 have been specifically designed to provide low cost, reliable and accurate thermocouple temperature measurement and transmission in a wide array of industries, including chemical, petrochemical, power generation and food processing.

These models are especially useful in process control and monitoring applications where the process sensor is located remotely



from the receiver. The 2B52 and 2B53 may then be used to provide signal conditioning near the point of temperature measurement and to transmit an accurate, noise immune, high level current signal over conventional copper wires, resulting in improved performance and reduced cost.

#### DESIGN FEATURES AND USER BENEFITS

Low Cost: Low transmitter cost, two-wire operation and the use of inexpensive copper wire for transmission result in lower total installation cost.

High Isolation (2B52): Input to output isolation eliminates ground loop errors in installations requiring grounded sensors and permits direct transmission of signal to a receiver where common mode voltages up to 600V rms may exist.

High Noise Rejection: The 2B52 and 2B53 feature internal filtering circuitry to eliminate errors caused by RFI/EMI and line frequency pickup.

Environmental Protection: High quality electronic components, protective coating and mechanical packaging combine to provide a high degree of reliability and protection against temperature, humidity and noise interference.

Millivolt Transmission: Unique circuitry of the 2B52 and 2B53 allows both models to be used as mV signal transmitters.

Ease of Calibration: Both models can be quickly, easily and accurately calibrated in the field to operate over any input span between 5 and 100 millivolts.

### **SPECIFICATIONS** (typical @ +25°C and Vs = +24V dc unless otherwise noted)

Model	2B52A	2B53A
INPUT SPECIFICATIONS		
Thermocouple Types	J, K, T	•
Input Span Range	5mV min, 100mV max	•
Input Impedance	5ΜΩ	•
Input Bias Current <sup>1</sup>	85nA	30nA
Zero and Span Adj. Range	±5% of Span	•
Open Input Detection	Upscale	•
OUTPUT SPECIFICATIONS		
Output Span	4-20mA	•
Minimum Output Current	3.3mA, typ	2mA, typ
Maximum Output Current	42mA, typ	28mA, typ
Load Resistance Range Equation	$R_{I} max = (+V_{S} - 12V)/20mA$	•
@ +24V Supply	0 to 600Ω max	•
Output Protection <sup>2</sup>	+60V	•
ACCUBACY		
Total Output Error <sup>3</sup>	±0.1%	•
Stability vs. Ambient Temperature		
Zero, for Ambient 0 to $+50^{\circ}C^{4}$	±0.015°C/°C	
$0 \text{ to } +85^{\circ}\text{C}^4$	±0.025°C/°C	•
$-30^{\circ}$ C to $0^{\circ}$ C <sup>4</sup>	±0.06°C/°C	•
Span, for Ambient -30°C to +85°C	±0.005%/°C	•
Warm-up Time to Rated Performance	5 min	3 min
CMV Input to Output Continuous	600V mmc	NA
Common Mode Rejection @ 60Hz	160dB	NA
Normal Mode Rejection, @ 60Hz	60dB	NA
RESPONSE TIME		
to 90% of Span	0.3 sec	0.1 sec
INTRINSICALLY SAFE OPERATION		
Use in Class I, Division 1,		
Groups A,B,C, and D Hazardous		
Locations	FM Approved	NA
POWER SUPPLY		
Voltage, Operating Range	+12V to +60V dc	•
Supply Change Effect, % of Span		
on Zero	0.005%/V	•
on Span	0.001%/V	•
ENVIRONMENTAL		
Temperature Range Rated		
Performance	~30°C to +85°C	•
Storage Temperature Range	-55°C to +125°C	•
Relative Humidity, Noncondensing <sup>5</sup>	0 to 90%	•
RELEFFECT (5W @ 470MHz @ 3 ft )	0.00 / 0.0	
Error. % of Span	±0.5%	*
PHVSICAL		
Case Size	A" × 2.25" × 1.25"	•
Weight	$7 \land 3.23 \land 1.23$ 8 5 oz (240g)	8 07 (227-)
	0.0 02, (2408)	0 02. (227g)

#### NOTES

<sup>1</sup> Includes thermocouple burnout detection current.

<sup>3</sup> Protected for reverse polarity and for any combination of input and output pins, <sup>3</sup> Accuracy is specified as a percent of output span (16mA). Accuracy spec includes combined effects of transmitter repeatability, hysteresis and linearity. Does not

include sensor error.

<sup>4</sup>Includes combined effects of cold junction compensation and amplifier offset drift.

<sup>s</sup>Per MIL-STD-202E method 103.

\*Specifications same as 2B52A.

Specifications subject to change without notice.

### OUTLINE DIMENSIONS (MAX)

Dimensions shown in inches and (mm).



2B53A (Nonisolated)	· · · ·	
Select Housing 1 – Standard Enclosu	are}	
Select Thermocouple Ty J, K or T }	pe	_
Select Temperature Ran 01 through 06	ge }	
Range in °C(°F)	ТС Туре	No.
-100 to +300		
(-148 to +572)	J, K, T	01
0 to +200		
(+32 to +392)	Т	02
0 to +500		
(+32 to +932)	J	03
0 to +600		
(+32 to +1112)	К	04
0 to +750	•	
(+32 to +1382)	J	05
0 to +1000		
(+32 to +1832)	К	06

#### STANDARD RELAY TRACK MOUNTING



Both 2B52 and 2B53 may be conveniently mounted in a standard relay mounting channel (3.25" wide) such as Reed Devices Inc. (RDI) model 3TK2-6 or equivalent.


# Four-Channel, Isolated Thermocouple/mV Conditioners

# MODELS 2B54 AND 2B55

#### FEATURES

Low Cost Per Channel Wide Input Span Range:  $\pm 5mV$  to  $\pm 100mV$  (2B54)  $\pm 50mV$  to  $\pm 5V$  (2B55)

12-Bit Systems Compatible

High CMV Isolation:  $\pm 1000V dc$ ; CMR = 156dB min @ 60Hz Low Input Offset Voltage Drift:  $\pm 1\mu V/^{\circ}C$  max (2B54B) Low Gain Drift:  $\pm 25ppm/^{\circ}C$  max (2B54B) Low Nonlinearity:  $\pm 0.02\%$  max ( $\pm 0.012\%$  typ) Normal Mode Input Protection (130V rms) and Filtering Channel Multiplexing: 400 chan/sec Scanning Speed Solid State Reliability

#### APPLICATIONS

Multichannel Thermocouple Temperature Measurements Low and High Level Data Acquisition Systems Industrial Measurement and Control Systems

#### **GENERAL DESCRIPTION**

Models 2B54 and 2B55 are low cost, high performance, fourchannel signal conditioners. Both models are functionally complete, providing input protection, isolation and common mode rejection, multiplexing, filtering and amplification.

The 2B54 has been designed to condition low level signals ( $\pm 5$ mV to  $\pm 100$ mV), like those generated by thermocouples or strain gages, in the presence of high common mode voltages. The 2B55 is optimized to condition  $\pm 50$ mV to  $\pm 5$ V or 4 to 20mA transmitter signals as inputs. The four-channel structure of both models results in significant cost and size reduction.

The high performance of the 2B54 and 2B55 is accomplished by the use of reliable transformer isolation techniques and an amplifier-per-channel architecture. Each of the input channels is galvanically isolated ( $\pm 1000V$  dc) from the other input channels and from output ground. The amplifier-per-channel structure is used to obtain low input drift ( $\pm 1\mu V/^{\circ}$ C max, 2B54B), high common mode rejection (156dB @ 60Hz), and very stable gain ( $\pm 25ppm/^{\circ}$ C max). Other key features include low input noise ( $1\mu V$  p-p), low nonlinearity ( $\pm 0.02\%$  max) and open-thermocouple detection (2B54).

#### APPLICATIONS

Models 2B54 and 2B55 were designed to serve as a superior alternative to the relay multiplexing circuits used in multichannel data acquisition systems, computer interface systems, process signal isolators, and temperature measurement and control instrumentation. Advantages over relay circuits include functional versatility, superior performance, and solid state reliability.



In thermocouple temperature measurement applications, outstanding low drift, high noise rejection, high throughput and 1000V isolation make the 2B54 a natural choice over flying capacitor multiplexers in conditioning any thermocouple type. When cold junction compensation is required in measurement of temperature with thermocouples, the 2B54 may be used directly with the model 2B56 Universal Cold Junction Compensator.

#### **DESIGN FEATURES AND USER BENEFITS**

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, reliable transformer isolation and solid state switching are used. Both models have been conservatively designed to meet the IEEE standard for Transient Voltage Protection (472-1974:SWC) and offer 130V rms normal mode input protection.

High Noise Rejection: To preserve high system accuracy in electrically noisy industrial environments, the 2B54 and 2B55 provide excellent common mode noise rejection, RFI/EMI immunity, and low pass filtering for rejection of series mode noise and 50Hz/60Hz pickup.

Ease of Use: The multichannel, functionally complete design in a compact  $(2'' \times 4'' \times 0.4'')$  module, assures ease of use, conserves board space and eliminates the need for a number of discrete components necessary in relay multiplexing circuits.

Low Cost: The 2B54 and 2B55 offer the lowest cost per channel for isolated, solid state, low level signal conditioners.

# **SPECIFICATIONS** (typical @ +25°C, Vs = ±15V and VOSC = +15V, unless otherwise noted)

Model	2B54A	2B54B	2B55A	OUTLINE DIMENSIONS
ANALOG INPUTS				Dimensions shown in inches and (mm)
Number of Channels	4	•	•	201/61 11 MAX
Input Span Range	±5mV to ±100mV	•	±50mV to ±5V	20101.1/ #44
Gain Equation	$G = 1 + 10k\Omega/R_G$	•	•	9.41 (19.4)
Gain Error	±0.2% max (G = 50 to 300)	•	±0.2% max (G = 1 to 100)	MAX
	±1% max (G = 1000)	•	NA	0.02 (0.5)
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max	±25ppm/°C max	
Gain Nonlinearity <sup>1</sup>	±0.03% max (G = 50 to 300)	±0.02% max(±0.012% typ)	$\pm 0.02\%$ max (G = 1 to 100)	- 0.2 (5.1) MAX
	±0.03% (G = 1000)	•	NA	
Offset Voltage				<u>∳</u> Ţ <u></u> <u></u> <u></u> <u></u> <u></u>
Input Offset, Initial (Adj. to Zero)	±20μV max		$\pm 50\mu V$ max	Ĭ <u>╋</u> ╪┥┽╞ <u>┧</u> ╪┽╎┼╞┼╪╎┼┼┼ <mark>╋</mark> ┨
vs. Temperature	±2.5µV/°C max	$\pm 1\mu V/C max(\pm 0.5\mu V/C typ)$	$\pm 5\mu V/C max$	
vs. Time	±1.5µV/month	•	•	
Output Offset (Adjustable to Zero)	±12mV max	•	•	8++++++++++++++81
vs. Temperature	±50µV/°C max	•	•	
Total Officer Drife (BTI) man	+ (2 5, 50)	$+(1+\frac{50}{2})wy/^{\circ}C$	$+(5_{11}V+\frac{50}{2})_{11}V^{2}C$	<b>₩</b> ₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩
Total Offset Drift (KTI), max	$\frac{1}{G}$		- (child g)hill c	ŀ <u>₹</u> +↓↓↓↓↓↓↓↓↓↓↓↓↓↓ <mark>₹</mark>
Input Noise Voltage				
$0.01 \text{Hz} - 100 \text{Hz}, \text{R}_{\text{S}} = 1 \text{k}\Omega$	1µV p-p	•	•	
CMV, Channel-to-Channel or				• 18 • • • • • • • • • • • • • • • • • •
Channel-to-Ground				
Continuous, ac, 60Hz	750V rms	•	•	ŀ <mark>∑</mark> ┼┾┽┼┤ <u>┽</u> ┽┼┼┼┼┼┼┼┼┼ <mark>┿</mark> ┥
Continuous, ac or dc	±1000V pk max	•	•	
Common Mode Rejection				
$R_S \leq 100\Omega, f \geq 50Hz$	156dB min (G = 1000)	•	145dB min (G = 100)	
$R_S \leq 100\Omega, f \geq 50Hz$	128dB min (G = 50)	•	110dB min (G = 1)	
Normal Mode Input, Without Damage	130V rms, 60Hz	•	•	
Normal Mode Rejection, @ 60Hz	55dB min (G = 1000)	•	55dB min (G = 100)	
Input Resistance, Power On	100MΩ	•	•	
Power Off	35kΩ min	•	74kΩ min	
Input Bias Current	+8nA max	•	•	WEIGHT: 2 QZ 0.1 (2.54) GRID
ANALOG OUPUT				(57G)
Output Voltage Swing <sup>2</sup>	±5V @ ±5mA	•	•	NOTES: TERMINAL PINS INSTALLED ONLY IN SHADED
Output Noise, dc - 100kHz	0.8mV p-p	•	• .	HOLE LOCATIONS.
Output Resistance	••			
Direct Output	0.1Ω	•	•	
Switched Output	35Ω	•	•	2B54/2B55 PIN DESIGNATIONS
CHANNEL SELECTION				
Channel Selection Time to ±0.01% FS	2.5ms max	•	•	
Channel Scanning Speed	400 chan/sec min	•	•	PIN FUNCTION PIN FUNCTION
Channel Select Input Reverse Voltage				2 + SELECT CH. D 38
Rating	3V max	•	•	3 SWID OUTPUT ENABLE 39 RG 4 SWITCHED 40 RG/COM CHANNELA
POWER SUPPLY				5 41 LO/OFS
Voltage				7 SENSE 42 V-OUT
Output +Ve (Bated Performance)	+15V dc +10%	•	•	B OFF ADI YOUTPUT
(Operating)	±12V to ±18V dc max	•	•	10 46
Oscillator +Vosc				11 -Vs 47 Hi 12 COM 48
(Rated Performance)	+13.5V to +24V	•.	•	13 +Vs 49 Rg
Absolute max +Vosc	+26V	•	•	14 50 Rg/COM CHANNEL B
Current				16 SELECT CH. C 52 V-OUT
Output $\pm V_{c} = \pm 15V$	+4mA max	•	•	17 53 V+ OUT /
Oscillator + Vosc = +15V	40mA max	•	•	19 55
Supply Effect on Offset	Tour t max			20 - 21 + SELECT CH. B 57 )
Output ±Ve	1000V/V RTO	•	•	22 58 Rg
Oscillator +Vosc	1µV/V RTI	•	•	23 59 Rg/COM CHANNEL C
ENVIRONMENTAL				25 61 V-OUT
Temperature				27 63
Pated Performance	$0 t_0 + 70^{\circ} C$	•	•	28 64
Operating	-25°C to +85°C	•	•	29 65 30 +Vosc 66 Ht
Storage	-25 C to +85°C	•	•	31 COM OSC. POWER 67
Belative Humidity	-55 C 10 +65 C			33 OUT SYNC 68 Hg B9 Rg/COM CHANNEL D
Non-Condensing to +40°C	0 to 85%	•	•	34 70 LO/OFS
	a"V 4"V 6 4"			36 + SELECT CH. A 72 V+ OUT
CASE SIZE	2 × 4 × 0.4	-	-	
NOTES	······································			· · · · ·

**AC1215 OUTLINE DIMENSIONS** 

Dimensions shown in inches and (mm),

6.0 (153

2854/2855

Cinch 251-22-30-160 or equivalent.

ADJ. POTS

Mating Connector:

4.5

DECODER

0.375 (9.53)

3 5 75 (90.81)

0.462

\*Specifications same as 2B54A.

Operations same as 22. If Gain nonlinearity is a percentage of output signal span representing peak deviation from the best straight line; e.g. nonlinearity at an output span of 10V pk-pk (±5V) is ±0.02% or ±2mV.

<sup>2</sup> Protected for shorts to ground and/or either supply voltage.

Specifications subject to change without notice.

#### MOUNTING CARDS AC1215, AC1216

The AC1215 and AC1216 mounting cards are available to assist in evaluation of the 2B54 and 2B55. These 4  $1/2'' \times 6''$  printed circuit edge connector cards have sockets that allow a 2B54/2B55 and 2B56 to be plugged directly onto them, as well as offset adjustment pots, and address decoding circuitry. The AC1215 and AC1216 differ only in input signal connections: the AC1215 includes a screw terminal block and AC1216 has an edge connector.

#### VOL. II, 9-48 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS

# Understanding the 2B54 and 2B55 Isolated Conditioners

#### FUNCTIONAL DESCRIPTION

The internal structure of the 2B54/2B55 is shown in Figure 1. Four individually isolated input channels are multiplexed into a single output buffer, with the desired channel selected by control inputs SELECT A through SELECT D. Isolated power and timing signals for the input channels are provided by an internal oscillator.

Each channel contains an input protection and filtering network and a low-drift amplifier whose gain is set by a usersupplied resistor ( $R_G$ ). Additional filtering is provided in the amplifier circuit. This structure preserves signal integrity by taking all signal gain ahead of the isolation and multiplexing circuits. The isolated power supply for each channel is brought out to permit convenient fine adjustment of the input offset voltage if desired.

Transformer coupling is used to achieve stable, reliable galvanic isolation of each channel from all other channels and from output ground. Although the bandwidth of the input channels is small (<2Hz at high gains) to provide immunity to normal-mode noise, the multiplexing technique allows the channels to be scanned at a high rate (400 channels/sec). Thus a high revisitation rate is maintained even in systems with a large number of input channels.

The output buffer amplifier operates at unity gain with feedback provided by an external connection from the DIRECT output to the SENSE input. The DIRECT output provides a  $\pm 5V$  swing with low source resistance to permit error-free operation with heavy loads. In addition, a separate seriesswitched output with an active-low enable control is provided so that multiple modules may be combined without the use of external analog multiplexers. An offset trim point which does not affect drift is also provided on the output channel.



Figure 1. 2B54/2B55 Functional Diagram

The internal oscillator has its own power supply pins for enhanced application flexibility, and a sync mechanism is provided to eliminate beat-frequency errors when multiple 2B54/ 2B55's are used or when a system clock is present.

The 2B54 and 2B55 share the same design, differing only in input specifications and filter characteristics.

#### **OPERATING INSTRUCTIONS**

The connections shown in Figure 2 are common to most applications of the 2B54/2B55, and in many cases will be all that is required. The following sections describe this basic application and also detail some optional connections which enhance the module's utility in more complex applications.



Figure 2. Basic 2B54/2B55 Application

#### Interconnection Guidelines

In any high accuracy isolator application it is important to minimize coupling between input and output, and the 2B54/ 2B55 pinout has been designed to make this easy to do. For best results, keep all leads associated with signals on the input edge as far as possible from signals on the output edge. This will minimize the effects of board leakage and capacitance. The use of a guard track on both sides of the board (Figure 2) can also be helpful.

The power supplies should be decoupled with tantalum capacitors as close to the unit as possible. For lowest noise, the output grounding scheme should be as shown in Figure 2. The output signal common is connected directly to pin 12, with power supply returns brought separately to that pin so that power supply currents do not flow in the low lead of the signal output.

Since most of the power taken by the 2B54/2B55 is supplied to the internal oscillator which requires only a positive supply and can accommodate a wide range of supply voltages, it is sometimes desirable to power the oscillator from a convenient source of unregulated power (such as  $\pm 24V - Figure 2$ ). A  $0.1\mu F$  capacitor should be then connected directly from pin 12 to pin 31. Since the output and oscillator circuits are not fully isolated, a dc path must exist between the two power supply commons. A small (one or two volts) potential difference between OUT COM and OSC COM will not affect operation.

#### Gain Setting .

The gain of each channel is independently set by a usersupplied resistor ( $R_G$ ) connected as shown in Figure 2. Channel gain will normally be selected so that the maximum output of the signal source will result in a plus or minus full scale ( $\pm 5V$ ) output swing. The resistor value required is  $R_G =$  $10k\Omega/(G-1)$ . Thus if  $R_G = 101\Omega$ , the gain will be 100, and an input signal swing of  $\pm 50$ mV will yield an output span of  $\pm 5V$ .

A parallel trim on the gain-setting resistor can be used to trim out the resistor's tolerance and the module's gain error (Figure 3). Since a parallel trim will always increase the gain, the value of the gain-setting resistor should be chosen to give an untrimmed gain somewhat lower than the desired trimmed gain. Good quality metal-film resistors should be used for  $R_G$ since gain accuracy and drift are a direct function of  $R_G$ 's characteristics. Cermet pots are suitable for the trim.



Figure 3. Input Offset and Gain Adjustments

#### **Optional Offset Adjustment**

The 2B54/2B55 has provision for fine adjustment of the input offset of each channel and the output offset of the entire module. None of the offset adjustments affect offset drift, and there is no need to make any adjustment unless the application calls for tighter offsets than those specified for the module type.

Connections for input offset adjustment are shown in Figure 3. This is a fine trim with a limited range  $(\pm 250\mu V - 2B54)$  and  $\pm 1mV - 2B55$ , RTI), used to adjust each channel for zero offset while operating at the desired gain. Since the range of the input offset trim is small, it will usually be necessary to adjust output offset first. This can be conveniently done by operating one channel with zero input at unity gain (by disconnecting the gain resistor) and adjusting the output offset adjustment are shown in Figure 4.



#### Figure 4. Output Offset and Master Gain Adjustments

An alternative offset adjustment procedure is appropriate in applications where the channel gains are field-selected by switching the gain-setting resistor. Here it is desirable to set the input offset so that there is no zero shift at the output when the gain is changed. To make the adjustment, switch back and forth from low to high gain with zero input and adjust the input offset control until no shift occurs at the output when changing gains. Then adjust the output offset control for zero output at the lower gain. Stable components (a metal film resistor and a cermet pot) should be used for the input offset adjustment to avoid compromising drift. Output offset adjustment components are not critical and may be omitted altogether when a single 2B54/ 2B55 is followed by an A to D Converter that has a zero adjustment.

#### **Channel Selection**

Each channel in the 2B54/2B55 is turned on and off by a SELECT input. As indicated in Figure 1, each SELECT input consists of an LED in series with a resistor, and is not connected to any other circuits in the module. Turning the LED of  $(1 \ge 50 \mu A)$  turns the channel off. This allows considerable flexibility of connection, but the easiest way to use the SELECT inputs is to tie all four SELECT + pins to +5V and drive the SELECT – inputs from TTL logic (either open-collector or totem-pole outputs can be used), as shown in Figure 2.

It is also possible to use CMOS logic to drive the SELECT inputs (Figure 5). With a +15V logic supply a standard CMOS decoder or gate can supply enough current to drive the SE-LECT inputs directly, but at lower supply voltages it is advisable to use a buffer such as that shown in Figure 5b. The power taken by the SELECT inputs is small, since only one is on at a time, but at the higher CMOS supply voltages more current than the required 2.5mA will flow. This does not affect operation, but if desired the current can be brought back to the minmum value with series resistors as shown in Figure 5. Use  $2k\Omega$ for 10V operation, and  $3.9k\Omega$  at 15V.

The maximum reverse voltage applied to any SELECT input must be limited to 3V to avoid damage to the LED. Maximum forward current should be kept below 25mA. Each SELECT input is isolated from all other circuits in the module and may be operated up to  $\pm 50V$  away from output and power ground.

Channels may be selected in any order, and there are no restrictions on rate or duty cycle except the 2.5ms settling time for access to a channel. It should be noted, however, that selecting two or more channels simultaneously for more than a few microseconds will result in a very long settling time when the conflict is resolved. Timing overlaps should therefore be avoided.







Figure 5. CMOS Channel Selection

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#### **Channel Expansion**

The 2B54/2B55 has provision for directly interconnecting several modules when more than four channels are needed. The series-switched outputs of a group of modules are connected together, the SELECT inputs are driven in parallel, and the output of the desired module is selected using the Output Enable pin. This is shown in Figure 6. A single 74LS139 decoder is used to drive the SELECT inputs of up to four modules, and also provides address expansion so that the binary coded channel address word selects the appropriate module output via the Output Enable pins. The overall operation of the series-switched outputs is analogous to three-state logic, and the output rail is thus an analog bus.

It is possible to operate up to sixteen modules in parallel, for a total of 64 input channels. Note that it will be necessary to break up the SELECT inputs into several groups to avoid overloading the decoder when many modules are used. The settling time of the output switches is  $<50\mu$ s to  $\pm0.01\%$  and is thus negligible in comparison to the channel selection times.

The Output Enable signal is active low, and is compatible with both TTL and CMOS logic. The switching threshold is +1.8V; input current at 0V is typically -0.4mA.

The output resistance of the Switched Output (typically  $35\Omega$  +0.5%/°C) is low enough to provide fast switching times but will cause gain errors when driving a heavy load. A single buffer isolating the Switched Outputs from the load will solve this problem in an "analog bus" application (Figure 6). In single-module applications the DIRECT (low impedance) output should be used. Note that in all cases the SENSE pin *must* be connected to the DIRECT output to provide feedback for the output amplifier.



Figure 6. Expansion to More than Four Channels

#### Synchronization

In applications where multiple 2B54/2B55's are used in close proximity or when system clock signals are present near the isolator, differences in individual oscillator frequencies may cause "beat frequency" related output errors. To eliminate these errors, multiple units may be synchronized by connecting the SYNC OUT (pin 33) terminal to the SYNC IN (pin 32) terminal of the adjacent 2B54/2B55 (Figure 7). The first of a group of modules may be synchronized to an external source via the SYNC IN pin. To minimize noise pickup, sync wiring should be separated from analog signal runs.

The frequency of the external sync source, when used, will have a small effect on the gain and output offset of the 2B54/2B55. Thus any adjustments should be made with the module synchronized.



#### Open Input Detection

The 2B54 can be programmed to respond to an open-circuit condition on a channel input with either an upscale or downscale response when the affected channel is selected. The response time to detect an open input can be in the tens of seconds, since only a few nA of input bias current are available to charge the input filter. The circuits in Figure 8 indicate the selection of either downscale or upscale response and can be used to provide shorter open-circuit response times. Either circuit will produce a bias current of approximately 20nA which can be used to aid or oppose the 3nA typically supplied by the module, as shown. The circuit of Figure 8A has the advantage of simplicity, but the highvalue resistor may not be readily available. Figure 8B shows how to solve the problem at the expense of complexity. The values shown may be modified to give an optimum trade of bias current for response time in a given application. A 2 to 5 second response is typical for the values shown.

If a downscale response is desired, a resistor divider circuit like Figure 8B may be desired to prevent a negative overscale. If a negative overscale condition occurs (typically -7V), the output will saturate on all channels.



### Figure 8. High Speed or Reversed Open Input Detection

#### **Output Filtering**

In most applications, no output filtering will be required since the effect of the small carrier-related noise spikes on the output (<1mV p-p, 100kHz B.W.) drops off rapidly as bandwidth decreases and in many cases will be negligible. In some applications (e.g., when driving a successive-approximation A to D) the effective system bandwidth may be large enough to pass the noise. To eliminate the carrier noise (without any effect on switching times), a simple R-C filter may be used at the output (Figure 9A). Only one filter is needed even when multiple modules are used, as shown in Figure 9B. If the load to be driven has an input resistance of less than 10M $\Omega$ , a buffer will be needed.



Figure 9. Output Filtering

#### CMR AND NMR PERFORMANCE

Common mode rejection is a result of both isolation and filtering and indicates ability to reject common mode inputs while amplifying differential signal inputs. CMR is dependent on source impedance imbalance, signal frequency and conditioner gain.

Normal mode rejection is also a function of the 2B54/2B55 gain. Figures 10 and 11 illustrate typical CMR and NMR performance. Note that any additional low pass filtering (e.g., an integrating A to D converter) at the output of the 2B54/ 2B55 will further improve both CMR and NMR performance.



Figure 10. Common Mode and Normal Mode Response – Model 2B54



Figure 11. Common Mode and Normal Mode Response – Model 2855

#### APPLICATIONS

Thermocouple Temperature Measurement: Figure 12 shows a four-channel thermocouple input system with isolation, amplification, and multiplexing provided by the 2B54. Several different thermocouple types are used, and the gain-setting resistors on each channel have been chosen to take the standard ANSI range for each type to a 5V output span. Since thermocouples must be compensated for the temperature of the reference junction which is formed where the thermocouple leads are terminated, the 2B56 Universal Cold Junction Compensator is used. The 2B56 monitors the temperature of the reference junction (terminal block) via an external sensor and corrects the signal at the output of the 2B54 for reference temperature. Compensation for several thermocouple types is selectable via digital control inputs. Thermocouple linearization, if needed, would be typically performed in system's software.



Figure 12. Four-Channel Thermocouple Temperature Measurement with Cold Junction Compensation

**Process Signals Interface:** In Figure 13, the 2B55 is used to provide floating inputs for four 4-20mA process signal loops. The use of floating inputs in this type of application gives protection from common-mode voltages and greatly simplifies system configuration, since additional loads in series with the loop can be connected on either side of the isolator input.

Each current input is converted into a 1 to 5 volt signal by a 250 $\Omega$  resistor. The 2B55 is operated at unity gain (no gainsetting resistors) so that a 1 to 5 volt signal appears at the output. Since no gain-setting resistors are used, gain adjustment, if required, is done by connecting trims directly across the input resistors. Other current ranges can be accommodated by changing the value of the input resistors.

When there are several loads on the loop, compliance voltage at the transmitter may be at a premium. In this case it will be advantageous to reduce the voltage swing at the isolator inputs by using smaller resistors (perhaps  $25\Omega$ ) and scaling the output back to a 5V span by taking an appropriate gain in the isolator.



Figure 13. Isolated 4-20mA Loop Signals Interface

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# High Accuracy, Thermocouple Cold Junction Compensator

#### FEATURES

Universal Thermocouple Compensation: Internally Provided: Types J, K, T User Configurable: Types E, R, S, B Digitally Programmable Type Select High Accuracy: ±0.8°C max over +5°C to +45°C High Ambient Rejection: 50 to 1 min Low Cost: Small Size: 1.5" × 2" × 0.4"

#### APPLICATIONS

Thermocouple Signal Conditioning Temperature Measurement and Control Systems Temperature Data Acquisition and Logging Temperature Controllers

#### **GENERAL DESCRIPTION**

Model 2B56 is a high accuracy, universal thermocouple cold junction compensator. Designed to operate with an external temperature sensor in thermal contact with the cold junction, the 2B56 provides an automatic compensation for amplified thermocouple signals over wide ambient temperature variations. The 2B56 is calibrated to compensate the cold junction to a reference temperature of 0°C. The total compensation error is  $\pm 0.8^{\circ}$ C max over  $+5^{\circ}$ C to  $+45^{\circ}$ C.

Designed to compensate seven different thermocouple types, the 2B56 may be digitally programmed to select compensation for types J, K and T, and one user programmed type (E, R, S, B or none). This feature makes the 2B56 especially suitable for multichannel applications involving several thermocouple types.

#### COLD JUNCTION COMPENSATION PRINCIPLES

In thermocouple measurements, temperature is determined by measuring the potential difference between the measurement (hot) junction of two dissimilar metals and the reference (cold) junction which is formed when thermocouple leads are connected to a measuring circuit. Since this potential difference is proportional to the temperature difference between the measurement temperature and the temperature at the reference junction, the reference junction temperature must be known. Changes in reference junction temperature influence the output voltage and, therefore, cold junction compensation is required to eliminate measurement errors.

Two methods may be used to reduce errors introduced at the thermocouple connections: keep the reference junction at a known constant temperature, or measure the reference junction temperature and cancel the changes by the appropriate





correction to the thermocouple output signal. The first method, accomplished by immersing the reference junction in an ice bath maintained at  $0^{\circ}$ C is not very practical. The 2B56 employs the second method and has been specifically designed to eliminate the need for ice baths by electronically simulating the desired reference point. Digital programmability, high accuracy and low cost make the 2B56 ideal for single or multichannel thermocouple temperature measurement, indication or control systems.

#### FUNCTIONAL DESCRIPTION

The 2B56 compensates for cold junction temperature by adding a correction signal at the output of the user's thermocouple amplifier, as shown in Figure 1. The value of the correction signal is determined by the cold junction temperature, as measured by a sensor, and the thermocouple type in use, as specified by two digital TYPE SELECT inputs. Since compensation is done at the output of the thermocouple amplifier it is also necessary to scale the correction signal for the gain of the amplifier. This is done by a scaling circuit which has provision for a user-supplied gain-setting resistor for each thermocouple type in use.

Compensating networks for thermocouple types J, K, and T are built into the 2B56. A fourth compensation (X) can be programmed with two external resistors for any other thermocouple type. The X compensation can also be used without programming resistors to obtain an uncompensated output when sensors other than thermocouples are in use.

# SPECIFICATIONS

(typical @  $+25^{\circ}$ C, Vs =  $\pm 15$ V unless otherwise noted)

MODEL	2B56A
COLD JUNCTION COMPENSATION	
Thermocouple Types:	
Internally Compensated	J, K, T
Externally Programmable	B, E, R, S, None
Reference Temperature	0°C .
Compensation Accuracy	
Total Output Error @ +25°C <sup>1</sup>	±0.2°C
vs. Ambient Temperature (+5°C to +45°C) <sup>1</sup>	±0.8°C max
Compensation Error	
vs. Sensor Temperature (+5°C to +45°C) <sup>2</sup>	±0.4°C max (±0.15°C typ)
vs. Compensator Module Temperature	
(0 to +70°C) <sup>3</sup>	±0.02°C/°C max (0.01°C/°C typ)
Cold Junction Temperature Sensing Element	AD590 or 2N2222
INPUT SPECIFICATIONS	
Voltage Signal Range	±10V
Input Impedance	100kΩ
Signal Gain <sup>4</sup>	+1V/V
vs. Temperature	±10ppm/°C
Input Offset Voltage	±1mV max
vs. Temperature	±15µV/°C max
OUTPUT SPECIFICATIONS 5	
Output Voltage	±10V @ ±5mA
Output Impedance	0.1Ω
DYNAMIC RESPONSE	
Selection Settling Time	0.5ms
Signal Settling Time, to ±0.01%	50µs
DIGITAL INPUTS	
Select Inputs A & B	TTL, CMOS Compatible
POWER SUPPLY	
Analog, Rated Performance	±15V dc ±10% @ ±5mA
Operating	±12V to ±18V dc
Digital, V <sub>DD</sub>	+5V to +15V dc @ 2mA max
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
CASE SIZE	1.5" × 2" × 0.4"

NOTES

Total compensation error composed of errors of temperature sensor and module at

Total compensation error contributed by ambient temperature changes at temperature senso Compensation error contributed by ambient temperature changes at the module.

<sup>4</sup> Signal gain of 2 is also available by jumper selection.

<sup>5</sup> Protected for shorts to ground or either supply voltage

Specifications subject to change without notice

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а Туре	Max Gain to +45°C	Max Gain for Sensor Temp to +45°C to +70°C		
3	1000	650		
К, Т	1300	820		
Ε	870	550		
R, S	9000	5500		
В	Any	Any		

Table I. Maximum Gain vs. Sensor Temperature and Thermocouple Type

а Туре	RX1	RX2
E	412kΩ	1.43kΩ
R, S	412kΩ	121Ω
		•

Table II. Resistor for Compensating Types E, R and S

Type Sel. Logic B   A		Compensation
0	0	J
0	1	К
1	0	Т
1	1	x

Sensor	V <sub>CAL</sub> (mV)				
Temp (°C)	2N2222	AD590			
5	616.5	634.5			
10	604.9	645.9			
15	593.3	657.3			
20	581.6	668.7			
25	570.0	680.1			
30	558.4	691.5			
35	546.8	702.9			
40	535.1	714.3			
45	523.5	725.7			

Values may be interpolated

Table IV. Calibration Voltage Table III. Digital Selection vs. Sensor Temperature of Compensation Type

OUTLINE DIMENSIONS Dimensions shown in inches and (mm).





MATING SOCKET: AC1217

A buffer amplifier is provided at the output of the 2B56 to preserve accuracy when driving heavy loads. The gain from  $V_{IN}$  to  $V_{OUT}$  will be +1 when SCALE is connected to  $V_{OUT}$ (see Figure 1). Input and output signal swings of up to ±10V can be accommodated with this connection. When the SCALE pin is left open, the gain from  $V_{IN}$  to  $V_{OUT}$  is +2. This is useful when interfacing a thermocouple amplifier with a ±5V output swing (such as the 2B54) to an A to D converter with a ±10V input range.



Figure 1. 2B56 Functional Block Diagram

It should be noted that the 2B56 is designed for use with noninverting thermocouple amplifiers. Thus a positive voltage change at the input of the 2B56 must indicate increasing temperature.

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# Applying the 2B56

#### **OPERATING INSTRUCTIONS**

Temperature Sensors: The temperature sensor used with the 2B56 can be either the Analog Devices AD590 temperature transducer or the popular 2N2222 transistor. Either sensor type can be used without loss of accuracy, but each has advantages in different applications. The 2N2222 (the metal can version must be used) is widely available at very low cost. However, an adjustment must be made whenever the sensor is replaced. The AD590 is available in several precalibrated accuracy grades, but at somewhat higher cost.

Connections are shown for both sensor types in Figure 2. Resistor  $R_{CAL}$  is the calibration adjustment point. It is used only to adjust for unit-to-unit variations in the sensors. All other adjustments have been made internal to the 2B56.



#### Figure 2. Sensor Connections and Calibration

With either sensor type, proper placement of the sensor is important. Close thermal contact of the sensor and the thermocouple termination point (reference junction) is necessary, particularly when nearby heat sources are present, since these could cause the sensor temperature to differ from the reference junction temperature. In multichannel applications, care should be taken to keep all input terminals at the same temperature to avoid channel-to-channel errors. The sensor may be placed at any distance from the 2B56. When the sensor leads are more than ten feet long, or where strong noise sources are present, shielded cable should be used with the 2N2222 sensor. The AD590 will operate properly with twisted-pair leads at distances up to a few hundred feet.

Gain Selection: Since the 2B56 performs cold junction compensation at the output of the user's thermocouple amplifier, it must take the gain of that amplifier into account. For this purpose, four gain-programming pins are provided: one each for the J, K, and T compensations and one for the X (userselected) compensation. Thus the user's thermocouple amplifiers can have different gains for each thermocouple type in use, and the 2B56 gain will be selected automatically when the thermocouple type is selected at the digital TYPE SELECT inputs. Gain-programming resistors are connected as shown in Figure 1. The value of each resistor is  $R = 10k\Omega/(G-1)$  where G is the gain of the user's thermocouple amplifier from the thermocouple terminals to the input of the 2B56. As an example, if the thermocouple amplifiers in use have a gain of 110 for type J, 90 for type K, and 220 for type T, then  $R_J =$ 91.7 $\Omega$ ,  $R_K = 112\Omega$ , and  $R_T = 45.7\Omega$ . Gain resistor pins for unused thermocouple types must be grounded. The resistors used to set gain should have a tolerance of 1% or better. A 1% error in setting gain will result in a 0.01°C/°C slope error.

The gain of the thermocouple amplifier will normally be determined by the thermocouple type, temperature measurement range, and A to D converter input range, but there are some practical limits imposed by the 2B56. The minimum allowable gain for proper operation is 40. The maximum gain which can be used is limited by the dynamic range of the compensation circuits in the 2B56, and is a function of thermocouple type and the temperature range (at the sensor) over which compensation is to be effective. Table I lists the maximum gain for each thermocouple type both for the specified  $+5^{\circ}C$  to  $+45^{\circ}C$  sensor temperature range and for a wider (reduced accuracy) 0 to  $+70^{\circ}C$  range.



Figure 3. Error Due to Thermocouple Nonlinearity

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Compensation of Other Thermocouple Types: Compensation for type J, K, and T thermocouples is built into the 2B56. A fourth compensation can be added by installing two resistors ( $R_{X1}$  and  $R_{X2}$ ) as shown in Figure 1. Table II gives the values needed for proper compensation of type E, R, and S thermocouples. Type B thermocouples are a special case, in that they have almost no output in the +5°C to +45°C range, and therefore, do not need cold junction compensation at all. To accommodate a type B thermocouple, select No Compensation (described in the next section). Errors due to cold junction temperature will be less than ±1°C for any measurement temperature above 260°C. In the measurement range beyond 1000°C (where type B thermocouples are normally used) the error will be less than ±0.3°C.

No Compensation Operation: In some instances it may be desirable to disable the compensation function of the 2B56, so that it functions as a straight-through amplifier with a gain of one (or two, if the output scaling feature is used). This might be done, for example, in a multichannel system with a mixture of thermocouples and strain gage signals or other sources requiring no compensation. It is also necessary when using the type B thermocouple, as described above. The X compensation can be programmed to provide no compensation by grounding pin 11 (X COMP), Figure 1. A 200 $\Omega$  resistor should be used for R<sub>X</sub> (at any gain). Selecting X compensation with this connection will give an uncompensated output.

Digital Inputs: The TYPE SELECT inputs are compatible with TTL or CMOS logic, or may be used with jumpers or switches. Table III shows the truth table for these inputs. Each input has an internal  $22k\Omega$  pullup resistor to  $V_{DD}$  and drives a single CMOS gate. For use with TTL signals,  $V_{DD}$ should be connected to the +5V logic supply. When CMOS logic is used, connect  $V_{DD}$  to the CMOS logic power supply (which must be in the +5V to +15V range). If jumpers or switches are used, connect  $V_{DD}$  to the +15V analog power supply. Grounding a SELECT input will give a logic "0"; an open input will be at logic "1" due to the action of the internal pullups. A separate pin is provided for logic ground to minimize ground loop problems. However, for proper operation logic ground at the module must be within  $\pm 0.3V$  of analog common. Failure to observe this restriction may result in damage to the module.

**Calibration:** Only one adjustment is necessary to get proper operation of the 2B56. This is shown in Figure 2 for both sensor types.  $R_{CAL}$  is adjusted to obtain the correct voltage at  $V_{CAL}$  for the appropriate sensor type and temperature, as listed in Table IV. Use a high-impedance voltmeter to measure  $V_{CAL}$  to prevent loading errors.

The tolerance to which the calibration adjustment must be made depends on the requirements of the application. For either sensor type, and for all thermocouple types, each millivolt of calibration error will result in a temperature offset error at the 2B56 output of  $0.44^{\circ}$ C, accompanied by a slope error of  $0.0015^{\circ}$ C/°C.

Curvature Error: The voltage output of thermocouples is a nonlinear function of temperature, so the reference junction output which is compensated by the 2B56 is also nonlinear. The correction signal generated by the 2B56, however, is approximately linear. The 2B56 is adjusted internally to give the best fit of its linear correction to the nonlinear reference junction output over the  $+5^{\circ}$ C to  $+45^{\circ}$ C range. The remaining error, which is included in the specifications given on page 2, is shown for each thermocouple type in Figure 3. Note that as a result of thermocouple nonlinearity the error at  $+25^{\circ}$ C will not be zero after calibration is done. The error for a particular thermocouple type could be adjusted to zero' at  $+25^{\circ}$ C by appropriate adjustment of the thermocouple amplifier offset, but the improvement will be at the expense of increased errors over the  $+5^{\circ}$ C to  $+45^{\circ}$ C range.

#### APPLICATIONS

The application of the 2B56 to a single-channel system is shown in Figure 1. Because the 2B56 compensates at the output of the thermocouple amplifier, it is also very attractive for use in multiplexed multichannel systems. Three typical applications are shown in Figure 4. The amplifier-per-channel structure shown in Figure 4a is one example of a system which could have a different gain for each thermocouple type in use, with channels preassigned or switchable for thermocouple type. The model 2B30 may be used as an amplifier for applications not requiring isolation.

In systems of this type, it is important that the ON resistance of the multiplex switches be less than 100 ohms, since larger values can create slope errors in the 2B56. If switches with higher resistance are used, a unity-gain buffer should be placed between the multiplexer and the 2B56. An AD741 or AD301type amplifier will suffice unless the system is very fast.

Figure 4b shows an input-multiplexed system. Different gains for different channels in this type of system are sometimes provided by software control of the amplifier gain. The 2B56 can also accommodate this situation, since it can accept a different gain for each thermocouple type.

Figure 4c shows a somewhat different application of the 2B56. Here the signal input is grounded, so that the output is simply the correction signal rather than a corrected version of the input. In this case the actual summation is done elsewhere, usually in the processor following the A to D converter. The advantage of such a structure is that it allows somewhat simpler calibration of the individual channels because the compensator can be bypassed.

There is no electrical limit to the number of channels that can be served by a single 2B56 in these applications or the



Figure 4. Model 2B56 in Various Multichannel Applications

many others that are possible. There is, however, a thermal limit in that a single temperature sensor must accurately monitor the temperature of a number of sets of input terminals. The actual channel limit will thus be determined by the allowable error and the degree to which all the inputs can be held at the same temperature.

Figure 5 shows the application of the 2B56 to the output of the 2B54 Four-Channel Isolator. More than one 2B54 can be served by the same 2B56 by using the built-in output switches of the 2B54 to connect several isolators to one output line. Note that the values of the gain-setting resistors for the 2B54 and 2B56 are the same, since both have the same gain formula. This permits very simple reconfiguration when the system must be tailored for new applications.



Figure 5. Four-Channel Thermocouple Temperature Measurement with Cold Junction Compensation

VOL. II, 9–56 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS

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# Low Cost, Two-Wire Temperature Transmitter

# MODEL 2B57

POWER

#### FEATURES

Low Cost Compatible with Standard 4-20mA Loops Low Span Drift:  $\pm 0.005\%$ <sup>o</sup>C max Low Nonlinearity:  $\pm 0.05\%$  max RFI Immunity Small Size:  $1.5'' \times 1.5'' \times 0.4''$ 

#### APPLICATIONS

Temperature Monitoring and Control Remote Temperature Sensing Process Control Systems Energy Management Systems

#### **GENERAL DESCRIPTION**

The model 2B57 is a low cost, two-wire temperature transmitter designed to interface with Analog Devices' AD590 temperature transducer and produce a standard 4 to 20mA output current proportional to the measured temperature. The 2B57 can also be interfaced with Analog Devices' AD592 temperature transducer when user calibrated. The 2B57 features a low span drift of  $\pm 0.005\%$ °C max, a high linearity ( $\pm 0.05\%$  max) and high noise immunity to assure measurement accuracy in harsh industrial environments.

The transmitter accommodates the AD590 temperature measurement range of  $-55^{\circ}$ C to  $+150^{\circ}$ C. Both zero and span adjustments are provided to trim the range for input measurement spans between 20°C and 205°C. The transmitter output of 4 to 20mA and a wide range of power supply voltages make the 2B57 compatible with standard two-wire control loops.

The basic package is a small  $(1.5'' \times 1.5'' \times 0.4'')$ , rugged, epoxy encapsulated module. For applications requiring protective housing, the 2B57 is available in a versatile metal case.

#### APPLICATIONS

The 2B57 has been specifically designed to provide low cost, accurate and reliable temperature measurement in any applications below  $+150^{\circ}$ C in which conventional electrical temperature sensors and transmitters are currently employed.

Industrial applications in process control and monitoring systems include chemical, petroleum, food processing, power generation and a wide variety of other industries. In multipoint energy management applications, low cost and small size combine to make the AD590 and 2B57 ideal for mounting in standard utility or thermostat boxes for remote temperature sensing.

#### **DESIGN FEATURES AND USER BENEFITS**

**RFI Noise Immunity:** The transmitter incorporates RFI filtering circuitry to assure protection against radio frequency interference.

Low Cost: The low cost of the 2B57 transmitter and two-wire operation reduce total system installation cost.

Linear Output: The transmitter output is linear with temperature, thus eliminating the need for linearizing circuitry.

Standard Loop Compatibility: The two-wire output structure conforms to the Instrument Society of America Standard ISA-S50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments."

TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS VOL. II, 9-57

# SPECIFICATIONS (typical @ +25°C and V<sub>S</sub> = +24V dc, unless otherwise noted)

MODEL	2B57A
INPUT SPECIFICATIONS	
Sensor Type <sup>1</sup>	AD590
Maximum Temperature Measurement Range	-55°C to +150°C
Minimum Input Span (for a 4-20mA Output)	20°C
Zero Adjustment Range	-55°C to +60°C
Input Protection <sup>2</sup>	+50V dc
Open Input Detection	Upscale
OUTPUT SPECIFICATIONS	
Output Span	4 to 20mA
Minimum Output Current	2.5mA
Maximum Output Current	26mA
Load Resistance Range	
Equation	$R_{LMAX} = (V_{SUPPLY} - 12V)/20mA$
@ +24V Supply	0 to 600Ω max
Output Protection <sup>2</sup>	+50V dc
NONLINEARITY (% of Span)	±0.02% typ (±0.05% max)
ACCURACY	
Warm-Up Time to Rated Performance	1 min
Total Output Error, without External Trims <sup>3</sup>	
Zero	±0.2% typ.(±0.5% max)
vs. Ambient Temperature (-30°C to +85°C)	±0.005%/°C typ (±0.01%/°C max)
Span	±0.2% typ (±0.5% max)
vs. Ambient Temperature (-30°C to +85°C)	±0.001%/°C typ (±0.005%/°C max)
RESPONSE TIME, to 90% of Span	0.15 sec
POWER SUPPLY	
Voltage, Rated Performance	+24V dc
Voltage, Operating	+12V to +50V dc
Supply Change Effect, % of Span	
on Zero	±0.005%/V
on Span	±0.001%/V
ENVIRONMENTAL	
Temperature Range, Rated Performance	-30°C to +85°C
Storage Temperature Range	-55°C to +100°C
Relative Humidity, to +40°C	0 to 90%
RFI Effect (5W @ 420MHz @ 3 ft)	
Error, % of Span	±0.5% max
CASE SIZE	$1.5'' \times 1.5'' \times 0.4''$
NOTES	

### **OUTLINE DIMENSIONS** Dimensions shown in inches and (mm).



#### MOUNTING CARD

#### **AC1583 OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



The AC1583 mounting card is available to assist in applying the 2B57. The AC1583 is suitable for mounting in a standard  $2'' \times 4''$  thermostat or electrical boxes. It includes screw terminals for field wiring, provisions for plugging in the 2B57 and AD590, and  $5k\Omega$  span and zero adjustment pots.

<sup>1</sup> AD590 produces an output current proportional to absolute temperature  $(1\mu A/^{\circ}K)$ . <sup>2</sup> Protected for any combination of input and output pins.

<sup>3</sup>Accuracy is specified as a percent of output span (16mA) for an input range of -55°C to +150°C. Accuracy spec includes combined effects of transmitter repeatability, hysteresis, and linearity. Does not include sensor error.

Specifications subject to change without notice.

#### VOL. II, 9-58 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS

# Applying the 2B57

#### **FUNCTIONAL DESCRIPTION**

The 2B57 transmitter converts the output of an AD590 temperature transducer to a current output within a span of 4 to 20mA. The transmitter includes input protection and filtering circuitry, an amplifier, voltage regulator, precision voltage reference and an output current generator.

A precision voltage reference, resistor network, and span and zero adjusts are used in conjunction with a low current drain amplifier to scale output signal of the AD590. The amplifier drives a current generator which controls output current (Figure 1).



Figure 1. Model 2B57 Functional Block Diagram

Input power and output signal are transmitted over the same two leads. The load resistance is connected in series with a dc power supply, and the current drawn from the supply is the 4 to 20mA output signal. The maximum series load resistance depends on the supply voltage and is given by  $R_{LMAX} = (+V_S - 12V)/20mA$ . A wide range of power supply voltages may be used (see Figure 2).



Figure 2. Maximum Load Resistance vs. Power Supply

#### THE SENSOR

The AD590 is a calibrated two terminal temperature sensor producing a current in microamperes  $(1\mu A/^{\circ}K)$  that is linearly proportional to absolute temperature for temperatures from -55°C to +150°C. The AD590 sensor is available in a hermetically sealed TO-52 transistor package, a miniature flat-pack, chip form and stainless steel probes (AC2626). The sensor construction assures reliable isolation from ground.

The AD590 is available in several accuracy grades, as shown in Table I. The grade selection will depend on whether the device is used uncalibrated or with calibration at a single value. For greater accuracy (in any grade), the device may be calibrated at two points.

#### TABLE I. AD590 ACCURACY SPECIFICATIONS (MAX ERROR)

Conditions	Max Error (±°C)				
Grade	I	J	к	L	м
Error at 25°C, as delivered	10.0	5.0	2.5	1.0	0.5
Errors over the -55°C to +150°C range:					
Without external calibration	20.0	10.0	5.5	3.0	1.7
With error nulled at 25°C only	5.8	3.0	2.0	1.6	1.0
Nonlinearity	3.0	1.5	0.8	0.4	0.3

#### **OPERATING INSTRUCTIONS**

Model 2B57 is factory calibrated to  $\pm 0.5\%$  accuracy for a maximum sensor measurement range of  $-55^{\circ}$ C to  $+150^{\circ}$ C (205°C span) with R<sub>SPAN</sub> and R<sub>ZERO</sub> resistor values as shown in Figure 3. For this input range 4mA output corresponds to an AD590 temperature of  $-55^{\circ}$ C and 20mA to  $+150^{\circ}$ C. The span and zero adjustments can be used to accommodate other input ranges.



#### Figure 3. Model 2B57 Basic Application

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Span Adjustment: The value of the span setting resistor R<sub>SPAN</sub> is determined by:

$$R_{SPAN} (\Omega) = \left(\frac{1.2V}{10^{-6} \text{ A} \times \text{SPAN}}\right) -5810\Omega$$

where SPAN is a desired measurement span in  $^{\circ}$ C. For example, for a measurement span of 100 $^{\circ}$ C R<sub>SPAN</sub> =

$$\left(\frac{1.2V}{10^{-6} \text{ A} \times 100}\right)$$
 -5810 $\Omega$  = 6.19k $\Omega$ . If a span accuracy

of  $\pm 0.5\%$  if desired, the value of the R<sub>SPAN</sub> resistor should be accurate to  $\pm 0.1\%$ .

Zero Adjustment: Zero adjustment must be performed after installation of the R<sub>SPAN</sub> resistor. To select R<sub>ZERO</sub> an AD590 or a calibrated current source may be used as an input to the 2B57. If an AD590 is used, it must be maintained at the desired reference temperature. A resistance decade box is inserted between pins 1 and 2 of the 2B57. The decade box is adjusted to produce an output corresponding to the selected reference temperature. For example, for a sensor measurement range of 0 to 100°C and an AD590 at 0°C, the R<sub>ZERO</sub> is adjusted for an output current of 4mA. If a current source is used, its output must equal the AD590 output at the selected reference temperature. For example, at 0°C the current source output must equal 273.2 $\mu$ A.

Sensor Calibration Trim: The sensor calibration error is the major contributor to maximum total error in all AD590 grades. To trim this error the temperature of the AD590 is measured by a reference temperature sensor and  $R_{ZERO}$  is trimmed to the calculated value of the 2B57 output current at that temperature. A reference temperature at the midpoint in the span should be selected.

For best measurement accuracy over temperature, RZERO and R<sub>SPAN</sub> should be trimmed with the AD590 at two known temperatures. For example, with the R<sub>SPAN</sub> selected for a 100°C span and with the AD590 at 0°C RZEBO is adjusted for a 4mA output. R<sub>SPAN</sub> is then trimmed for a 20mA output with the sensor at 100°C. Figure 4 illustrates a typical two-trim system accuracy.



Figure 4. Typical Two-Trim Accuracy (AD590 and 2B57)

#### **OPTIONAL PACKAGING CONFIGURATION (2B57A-1)**

The 2B57 is available mounted in an aluminum case including screw terminals for connecting an external sensor and power. This versatile housing may be surface mounted in racks, cabinets, NEMA enclosures, etc., or snapped onto standard relay tracks. The 2B57 in a metal housing is calibrated for a -55°C to +150°C measurement range and may be ordered by specifying model 2B57A-1. Price: 2B57A-1-\$95(1-9), \$68(100s).

#### TRANSMITTER HOUSING OUTLINE DIMENSIONS Dimensions shown in inches and (mm).





INTERNAL VIEW

Refer to operating instructions section for suggested method of calibration.

#### AC2626 PROBE (AD590 PACKAGING OPTION)

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the AD590F, the probe is available in linearity grades of 0.3°C, 0.4°C, 0.8°C or 1.5°C and is compatible with the 2B57 transmitter. The mechanical outline of the AC2626 is shown below.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring applications.

#### **AC2626 MECHANICAL OUTLINE**

Dimensions shown in inches and (mm).

### 3/16 STAINLESS STEEL TUBING FILLED WITH THERMALLY CONDUCTIVE EPOXY



NOTE 1 Probes are available in 4-inch or 6-inch lengths. Other lengths are available; consult factory for price and delivery.

NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue; M, green. NOTE 3 When assembling compression fitting (AC2629) to probe,

tighten the 1/2" nut 3/4's of a turn from finger tight.

# 

# Two-Wire, Linearized RTD Temperature Transmitter

# MODEL 2B58

RIDAL

CONTROL ROOM

#### FEATURES

Platinum RTD Input Linearized 4-20mA Output High Accuracy: ±0.1% Low Drift: ±0.01°C/°C Max RFI Immunity Low Cost FM Approved

#### APPLICATIONS

RTD Temperature Transmission in: Process Control Factory Automation Energy Management

#### **GENERAL DESCRIPTION**

The model 2B58 is a high accuracy, two-wire temperature transmitter designed to accept a platinum RTD (Resistance Temperature Detector) input and produce a proportional standard 4-20mA output. The RTD signal is internally linearized to provide an output which is linear with temperature. Four precalibrated ranges are available for RTD measurements from  $-100^{\circ}$ C to  $+400^{\circ}$ C.

The 2B58 features high accuracy of 0.1%, low drift of  $\pm 0.01^{\circ}$ C/°C, high noise rejection and RFI immunity. Both two-wire and three-wire  $100\Omega$  sensors may be used. Lead wire compensation is provided for three-wire RTDs. The 2B58 is approved by Factory Mutual for intrinsically safe use in 1 hazardous locations.

A rugged metal enclosure, suitable for field mounting, offers environmental protection and screw terminal input and output connections. This enclosure may be either surface or standard relay track mounted.

#### APPLICATIONS

The 2B58 has been specifically designed to provide highperformance two-wire transmission of measured temperatures using RTD sensors.

Two-wire current transmission permits remote mounting of the transmitter near the sensor to minimize the effects of noise and signal degradation to which low level sensor outputs are susceptible. Transmission of the proportional current output may be accomplished by means of inexpensive copper wires. These factors make the 2B58 ideally suited for applications where accuracy, stability, and low cost installation are desired.

#### DESIGN FEATURES AND USER BENEFITS

2868

RTD TRANSMITTER

High Accuracy: The 2B58 offers high calibration accuracy, linearized output and conformity with the standard DIN  $43760 (\alpha = 0.00385)$  RTD sensors.

.20

Low Cost: The 2B58 combines low price with a two-wire transmission, lowering total installation cost.

High Noise Rejection: The transmitter features internal filtering circuitry to assure protection against RFI and line frequency pickup.

Standard Loop Compatibility: The two-wire output structure conforms to the ISA Standard S50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments".

Wide Operating Temperature Range: The 2B58 has been designed to operate over -30°C to +85°C ambient temperature range.

# **SPECIFICATIONS**

(typical @ +25°C and VS = +24V dc unless otherwise noted)

Model	2858A
INPUT SPECIFICATIONS	
Sensor Type	Platinum, 100Ω @ 0°C, $\alpha = 0.00385$
	2 or 3 Wire
Normal Mode Rejection	56dB @ 60Hz
Sensor Excitation Current	0.5mA
Zero and Span Adjustment Range	±5% of Span
OUTPUT SPECIFICATIONS	· · · · · · · · · · · · · · · · · · ·
Output Span	4-20mA
Minimum Output Current	3.5mA, typ
Maximum Output Current	40mA, typ
Load Resistance Range Equation	$R_L max = (+V_S - 16V)/20mA$
@ +24V Supply	0 to 400Ω
Output Protection <sup>1</sup>	±60V
ACCURACY	· · · · · · · · · · · · · · · · · · ·
Total Output Error <sup>2</sup>	±0.1%
Stability vs. Ambient Temperature	
Zero, Measurement Range 01 through 03 <sup>3</sup>	$\pm 0.01^{\circ} C/^{\circ} C \max (\pm 0.005^{\circ} C/^{\circ} C typ)$
Measurement Range 04 <sup>3</sup>	±0.01°C/°C
Span	±0.005%/°C
Stability vs. Time <sup>2</sup>	±50ppm/Month
Lead Resistance Effect, to 40Ω per Lead	•••
Span Error	±0.5%
Warm-Up Time to Rated Performance	3 Minutes
INTRINSICALLY SAFE OPERATION	
Use in Class I. Division 1.	FM Approved
Groups A,B,C, and D Hazardous Locations	
RESPONSE TIME	·····
To 90% of Span	0.4 sec
Voltage Operating Range	+16V to +60V dc
Supply Change Effect % of Span	101 10 1001 40
on Zero	+0.005%/V
on Span	+0.01%/V
ENVIRONMENTAL Turnensen Banga Band Barformanas	10°C to +85°C
Temperature Kange, Kated Fertormance	-50 C 10 +85 C
Storage Temperature Range	-55 C to +125 C
Firm	t0.6% of Span
DELEffect (SW @ 470MHz @ 3 ft )	10.0% of Span
Fror	t0 5% of Span
DIDICION I	
PHYSICAL Con Size	4" × 2 25" × 1 25"
Uase bize	$\tau \land 3.23 \land 1.23$
weight	0 02 (227 g)
NOTES	

<sup>10</sup> Protected for reverse polarity and for any input/output connection combination. <sup>3</sup> Accuracy is specified as a percent of output span (16mA). Accuracy spec includes combined effects of transmitter repeatability, hysteresis and sensor linearization conformity. Does not include sensor error.

<sup>3</sup> See ordering information for measurement temperature ranges 01 through 04. <sup>4</sup> Per MIL-STD-202E Method 103B,

Per MIL-STD-202E Method 105B.

#### Specifications subject to change without notice.

#### **OUTLINE DIMENSIONS (MAX)**

Dimensions shown in inches and (mm).



#### ORDERING INFORMATION



#### STANDARD RELAY TRACK MOUNTING



Model 2B58 may be conveniently mounted in a standard relay mounting channel (3.25" wide) such as Reed Devices Inc. (RDI) model 3TK2-6 or equivalent.

VOL. II, 9-62 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS

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# Low Cost, Two-Wire RTD Temperature Transmitter MODEL 2B59

#### FEATURES

Low Cost Standard RTD Input Linearized 4-20mA Output High Accuracy: ±0.1% Small Size Ease of Installation

#### APPLICATIONS

Temperature Monitoring and Transmission Energy Management Systems



#### CALIBRATION

The 2B59 is factory calibrated to provide zero and span accuracy of  $\pm 0.1\%$  of span. Should field calibration of the 2B59 to the specified range be desired, the following procedure is recommended:

- 1. Connect the transmitter as shown in Figure 2. Substitute a resistance standard for the RTD and use a load resistor for the appropriate power supply voltage, as specified by the graph of  $R_{LOAD}$  max vs.  $V_{SUPPLY}$  (Figure 1).
- 2. Determine minimum and maximum resistance values of sensor being used from standard resistance/temperature tables. (For example, for a 100 Pt sensor, a measurement range of 0 to +100°C corresponds to the resistance range of 100.0 $\Omega$  to 138.50 $\Omega$ .)
- 3. Connect required minimum input resistance standard. Adjust ZERO potentiometer, if necessary, to obtain an output of  $4 \pm 0.016$ mA.
- Connect required maximum input resistance standard. Adjust SPAN potentiometer, if necessary, to obtain an output of 20 ±0.016mA.
- 5. Repeat steps 3 and 4 until readings converge.

An alternate method of calibration utilizing an RTD sensor would be to adjust the ZERO and SPAN potentiometers while alternatively maintaining the probe at the specified minimum and maximum measured temperatures. A precision thermometer, located at the temperature probe, should be used to provide an accurate point of reference.

#### GENERAL DESCRIPTION

The model 2B59 is a low cost temperature transmitter designed to accept an RTD sensor input and produce a 4-20mA output proportional to the measured temperature. The RTD signal is internally linearized to provide an output which is linear with temperature. The 2B59 is a true two-wire transmitter, with the same wiring used for power and output. The load resistance is connected in series with a dc power supply  $(+V_S)$  and the current drawn from the supply is the 4-20mA output signal.

The transmitter features high calibration accuracy of  $\pm 0.1\%$ . Several factory-calibrated temperature measurement ranges are available for standard platinum and nickel-iron RTD sensors. Both zero and span user-accessible screwdriver adjustments are provided for fine calibration after installation, if needed.

The 2B59 is packaged in a small  $(1.2'' \times 1.5'' \times 0.5'')$ , rugged, epoxy encapsulated module and may be easily mounted by using a single screw. Connections to the transmitter are made via four color-coded leads using standard wire nuts.

#### APPLICATIONS

The 2B59 has been specifically designed to provide low cost, small size, ease of installation, and reliability in multipoint temperature monitoring applications.

In energy management and control systems, the 2B59 may be mounted in standard  $2'' \times 4''$  utility or thermostat boxes in conjunction with a sensor and used for duct or room temperature sensing and transmission.

# SPECIFICATIONS (typical @ +25°C and VS = +24V unless otherwise noted)

MODEL	2B59A
INPUT SPECIFICATIONS	
Sensor Type	
Platinum	$100\Omega @0C, \alpha = 0.00385$
Nickel-Iron	1000Ω, 2000Ω @ +21.1°C (+70°F)
	$\alpha = 0.00527$
Zero and Span Adjustment Range	±3% of Span min
Open Input Detection	Upscale
OUTPUT SPECIFICATIONS	· · ·
Output Span	4-20mA
Minimum Output Current	3.4mA
Maximum Output Current	35mA
Load Resistance Equation	$R_L max = (+V_S - 10V)/20mA$
@ +24V Supply	0 to 700Ω
ACCURACY	
Total Output Error <sup>1</sup>	±0.1%
Stability vs. Ambient Temperature	
Zero	±0.015%/°C
Span	±0.005%/°C
Warm-Up Time to Rated Performance	1 min
RESPONSE TIME	
To 90% of Span	0.125ms
POWER SUPPLY	
Voltage, Operating Range <sup>2</sup>	+10V to +35V dc
Supply Change Effect, % of Span	±0.001%/V
ENVIRONMENTAL	
Temperature Range, Rated Performance	-25°C to +85°C
Storage Temperature Range	-55°C to +125°C
Humidity Effect	
Error, 90% RH @ +40°C	±0.2% of Span
PHYSICAL	
Case Size	1.2''  imes 1.5''  imes 0.5''

#### NOTES

<sup>1</sup>Accuracy is specified as a percent of output span (16mA). Accuracy spec includes combined effects of transmitter linearity, repeatability and hysteresis. Does not include sensor error.

<sup>2</sup> Protected for reverse polarity.

Specifications subject to change without notice.

#### ORDERING INFORMATION



+200 to +400 (+93 to +204) - Sensor 3 06

(Consult factory for additional ranges.)

**OUTLINE DIMENSIONS** 

Dimensions shown in inches and (mm).





c;

Figure 1. RLOAD vs. VSUPPLY



Figure 2. Basic Application

# 

# The Complete Signal Conditioning I/O Subsystem

#### FEATURES

Low Cost, Completely Integrated 16-Channel Modular Signal Conditioning Subsystem Wide Selection of Functionally Complete Input and **Output Plug-In Modules,** Rugged Industrial Chassis, Rack or Surface Mounted **On-Board Power Supplies Available** Analog Input Modules Available for Direct Interface to a Wide Variety of Signal Sources Thermocouples, RTDs, Strain Gages, Millivolt and Voltage Sources, 4-20mA/0-20mA Process Current Inputs **Current Output Modules** 4-20mA/0-20mA Outputs **Complete Signal Conditioning Function** Input Protection, Filtering, Amplification, Galvanic Isolation to ±1500V, Wide-Range Zero Suppression, High Noise Rejection and RFI/EMI Immunity, Simultaneous Voltage and Current Outputs

#### **GENERAL DESCRIPTION**

The 3B Series Signal Conditioning I/O Subsystem provides a low cost, versatile method of interconnecting real world analog signals to a data acquisition, monitoring or control system. It is designed to interface directly to analog signals such as thermocouple, RTD, Strain Gage, or AD590/AC2626 solid state temperature sensor outputs or millivolt or process current signals and convert the inputs to standardized analog outputs compatible with high level analog I/O subsystems.

The 3B Series Subsystem consists of a 19" relay rack compatible universal mounting backplane and a family of plug in (up to 16 per rack) input and output signal conditioning modules. Eight and four channel backplanes are also available. Each backplane incorporates screw terminals for sensor inputs and current outputs and a connector for high level single ended outputs to the user's equipment.

The input and output modules are offered in both isolated  $(\pm 1500V \text{ peak})$  and nonisolated versions. The input modules feature complete signal conditioning circuitry optimized for specific sensors or analog signals and provide high level analog outputs. Each input module provides two simultaneous outputs: 0 to 10V (or  $\pm 10V$ ) and 4-20mA (or 0-20mA). Output modules accept high level single ended signals and provide an isolated or nonisolated 4-20mA (or 0-20mA) process signal. All modules feature a universal pin-out and may be readily "mixed and matched" and interchanged without disrupting field wiring.

Each backplane contains the provision for a subsystem power supply. The 3B Series Subsystem can operate from a dc/dc converter or ac power supply mounted on each backplane or from externally provided dc power. Two LEDs are used to indicate that power is being applied.

# **3B** Series



conditioning problems in measurement and control applications. Some typical uses are in mini- and microcomputer based systems, standard data acquisition systems, programmable controllers, analog recorders, dedicated control systems, and any other applications where monitoring and control of temperature, pressure, flow, and analog signals are required. Since each input module features two simultaneous outputs, the voltage output can be used to provide an input to a microprocessor based data acquisition or control system while the current output can be used for analog transmission, operator interface, or an analog backup system.

#### DESIGN FEATURES AND USER BENEFITS

Ease of Use: Direct sensor interface via screw terminals, standardized high level outputs, factory precalibration of each unit and the modular design make the 3B Series Subsystem extremely easy to use. The subsystem features rugged packaging for the industrial environment and can be easily installed and maintained.

High Protection and Reliability: All field wired terminations offer 130V or 220V rms normal mode protection. To assure connection reliability, gold plated pin and socket connections are used throughout the system. The isolated modules offer protection against high common mode voltages and are designed to meet the IEEE Standard for Transient Voltage Protection (472–1974: SWC).

High Performance: The high quality signal conditioning features  $\pm 0.1\%$  calibration accuracy and chopper-based amplification which assures low drift ( $\pm 1\mu V/^{\circ}C$ ) and excellent long term stability. For thermocouple applications, high accuracy cold junction sensing is provided in the backplane on each channel. Low drift sensor excitation is provided for RTD and strain gage models. For RTD models, the input signal is linearized to provide an output which is linear with temperature.

#### APPLICATIONS

The Analog Devices 3B Series Signal Conditioning Subsystem is designed to provide an easy and convenient solution to signal

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

#### FEATURES

Wide Variety of Sensor Inputs Thermocouples, RTDs, Strain Gages, AD590/AC2626 Dual High Level Outputs Voltage: 0 to +10V or ±10V Current: 4-20mA/0-20mA Mix and Match Input Capability Sensor Signals, mV, V, 4-20mA, 0-20mA High Accuracy: ±0.1% Low Drift: ±1 $\mu$ V/°C Reliable Transformer Isolation: ±1500V CMV, CMR = 160dB Meets IEEE-STD 472: Transient Protection (SWC) Input Protection: 130V or 220V rms Continuous Low Cost Per Channel

#### **GENERAL DESCRIPTION**

Each input module is a single channel signal conditioner that plugs into sockets on the backplane and accepts its signal from the input screw terminals. All input modules provide input protection, amplification and filtering of the input signal, accuracy of  $\pm 0.1\%$ , low drift of  $1\mu V/^{\circ}C$  (low level input modules), and feature two high level analog outputs that are compatible with most process instrumentation. The isolated input modules also provide  $\pm 1500V$  isolation.

#### **THERMOCOUPLE INPUT MODEL 3B37**

The isolated thermocouple models incorporate cold junction compensation circuitry which provides an accuracy of  $\pm 0.5^{\circ}$ C over the  $+5^{\circ}$ C to  $+45^{\circ}$ C ambient temperature range. Open thermocouple detection (upscale) is also provided with the thermocouple models. Standard models are available with factory calibration for thermocouple types J, K, T, E, R, S and B. However, if another thermocouple type or a special range is desired, the 3B37-X-00 and ranging card, AC1310, can be used to satisfy the requirement. All screw terminal connections have at least 130V rms protection.

#### RTD INPUT MODELS 3B14, 3B15, 3B34

Each RTD model provides a sensor excitation current of 0.25mA and produces an output signal that is linear with temperature with a conformity error of  $\pm 0.05\%$  of span and accuracy of  $\pm 0.1\%$  span. The lead resistance effect for the three models is  $\pm 0.02^{\circ}C/\Omega$  for the 3B14 and the 3B34, and  $\pm .00001^{\circ}C/\Omega$  for the 3B15. All excitation input and output screw terminal connections have at least 130V rms protection.

#### STRAIN GAGE INPUT MODEL 3B16

Model 3B16 is designed to accept inputs from full four arm bridge strain gage-type transducers. The 3B16 provides a constant + 10V bridge excitation and can be used with a bridge resistance of  $300\Omega$  or greater. All excitation input and output screw terminal connections have 130V rms protection.

#### WIDEBAND STRAIN GAGE MODEL 3B18

Model 3B18 is designed to accept inputs from full four arm bridge strain gage-type transducers. The 3B18 provides a switch selectable excitation of +3.3V or +10.0V and can be used with  $100\Omega$  to  $1000\Omega$  strain gage bridges. The module has a 20kHz bandwidth to interface to dynamic signals.

## MILLIVOLT AND VOLTAGE INPUT MODELS 3B10, 3B11, 3B30, 3B31

Models 3B10 and 3B11 are nonisolated modules that accept



The choice of a specific 3B module depends on the type of input signal and also whether an isolated or nonisolated interface is required. Input modules are available to accept millivolt, volt, process current, thermocouple, RTD, strain gage, and AD590 inputs. The voltage output of each module is available from the voltage I/O connector while the current output is available on the output screw terminals.

millivolt and voltage signals respectively. Models 3B30 and 3B31 are isolated modules that accept millivolt and voltage signals respectively. All screw terminal connections have at least 130V rms protection.

#### WIDEBAND MILLIVOLT AND VOLT INPUT MODELS 3B40, 3B41

Models 3B40 and 3B41 are isolated modules that accept millivolt and voltage signals respectively. The modules have a 10kHz bandwidth to interface to dynamic signals. All screw terminal connections have at least 130V rms protection.

#### CURRENT INPUT MODELS 3B12, 3B32

Models 3B12 and 3B32 are nonisolated and isolated modules respectively that accept process current signals. Both models use a  $100\Omega$  sensing resistor that is mounted on backplane terminals 2 and 3. All screw terminal connections have at least 130V rms protection.

#### AD590 INPUT MODEL 3B13

Model 3B13 accepts an AD590 as its input signal. Sensor excitation is provided and a  $2k\Omega$  sensing resistor is mounted on backplane terminals 2 and 3. All excitation input and output screw terminal connections have 130V rms protection.

#### AC INPUT MODELS 3B42, 3B43, 3B44

Models 3B42, 3B43 and 3B44 are designed to accept ac signals from 20mV to 450V rms. The modules are rms calibrated for sinusoidal inputs, such as ac power lines. All screw terminal connections have at least 130V rms protection.

#### **FREQUENCY INPUT MODELS 3B45, 3B46**

Preliminary models 3B45 and 3B46 are designed to accept frequency input signals from 25Hz to 25kHz. User selectable thresholds of 1.6V and 0V (for zero crossing) are available. All screw terminal connections have at least 130V rms protection.

## **Output Modules**

High Level Voltage Input (0 to +10V, ±10V) Process Current Output (4-20mA/0-20mA) High Accuracy: ±0.1% Reliable Transformer Isolation: ±1500V CMV, CMR = 90dB Meets IEEE-STD 472: Transient Protection (SWC)

Output Protection: 130V or 220V rms Continuous Reliable Pin and Socket Connections Low Cost Per Channel

#### **GENERAL DESCRIPTION**

Each output module accepts a high level analog signal from the system connector and provides a current output on the output screw terminals. When a +24V loop supply is used, loads up to 850 $\Omega$  can be driven. If desired, +15V can be used to power the output modules with a smaller load (up to 400 $\Omega$ ). Each output module features high accuracy of ±0.1%. If isolation is required, the 3B39 provides ±1500V peak common mode voltage isolation protection.

#### NONISOLATED OUTPUT MODEL 3B19

The 3B19 output module accepts a 0 to +10V or  $\pm 10V$  input signal and converts it to a proportional current output. Output



ranges are jumper selectable for either 0 to 20mA or 4 to 20mA. The current output is protected to 130V rms continuous.

#### **ISOLATED OUTPUT MODEL 3B39**

Model 3B39 is an isolated module that accepts a 0 to +10V or  $\pm 10V$  input signal and converts it to a proportional current output. Output ranges are jumper selectable for either 0 to 20mA or 4 to 20mA. Input to output isolation is rated to 1500V pk continuous.

## Backplanes

FEATURE 4, 8, or 16-Channel Versions Available ac or dc Power Supply Options

#### **GENERAL DESCRIPTION**

The three backplane models, 3B01, 3B02 and 3B03 are designed for 16, 8 and 4 channels, respectively, to give users the flexibility to match the size of a system to specific applications. The sixteen channel backplane can be mounted in a  $19'' \times 5.25''$  panel space. The backplanes can be surface mounted, mounted on a rack or mounted in a NEMA enclosure.

#### POWER SUPPLY

The 3B Series Subsystem can operate from a common ac power supply or dc/dc (+24V input) power supply mounted on the backplane or an externally provided  $\pm 15V$  and +24V supply. The power supply is bussed to all signal conditioners in the system. The current consumption is a function of the modules that are actually used.



#### **3B Series Subsystem Specifications**

#### INPUT MODULES

#### Input Types

Thermocouples: J, K, T, E, R, S, B RTDs:  $100\Omega$  Platinum (linearized) Strain Gage Transducers:  $\pm 30mV$  and  $\pm 100mV$  spans Solid State Temperature Transducers: AD590 or AC2626 DC Voltage:  $\pm 10mV$ ,  $\pm 50mV$ ,  $\pm 100mV$  $\pm 1V$ ,  $\pm 5V$ ,  $\pm 10V$ DC Current: 4 to 20mA, 0 to 20mA

#### **Outputs (Simultaneous)**

0 to  $\pm 10V$  or  $\pm 10V$  and 4 to 20mA or 0 to 20mA

#### Performance

Accuracy:  $\pm 0.1\%$  of span Nonlinearity:  $\pm 0.01\%$  of span Bandwidth: 3Hz (-3dB)

Isolated Modules Common Mode Voltage, Input to Output: ±1500V pk continuous Transient Protection: Meets IEEE-Std 472 (SWC) Normal Mode Input Protection: 220V rms continuous Current Output Protection: 130V rms continuous

Common Mode Rejection @ 50Hz or 60Hz: 160dB

Normal Mode Rejection @ 50Hz or 60Hz: 60dB

#### Nonisolated Modules

Common Mode Voltage: ±6.5V Normal Mode Input Protection: 130V rms continuous

Current Output Protection: 130V rms continuous

Common Mode Rejection @ 50Hz or 60Hz: 90dB

Normal Mode Rejection @ 50Hz or 60Hz: 60dB

#### **OUTPUT MODULES**

#### Input

0 to  $\pm 10V$  or  $\pm 10V$ 

#### Output

4 to 20mA or 0 to 20mA

Specifications subject to change without notice.

#### Performance Accuracy: $\pm 0.1\%$ of span

Nonlinearity:  $\pm 0.01\%$  of span

Isolated Module Common Mode Voltage, Input to Output: ± 1500V pk continuous Current Output Protection Transient: Meets IEEE-Std 472 (SWC) Continuous: 220V rms

Nonisolated Module Current Output Protection: 130V rms continuous

#### BACKPLANES

Channel Capacity 3B01: 16 channels 3B02: 8 channels 3B03: 4 channels

#### **POWER SUPPLIES**

Backplane Mounted: 100, 115, 220, 240V ac, 50/60Hz or +24V dc External Power Option  $\pm$  15V dc and +24V dc

#### MECHANICAL

Input or Output Modules: 3.150" × 0.775" × 3.395" (80.0mm × 19.7mm × 86.2mm) Backplanes: 3B01: 17.40" × 5.20" × 4.37" (442.0mm × 132.1mm × 111.1mm) 3B02: 11.00" × 5.20" × 4.37" (279.4mm × 132.1mm × 111.1mm) 3B03: 7.80" × 5.20" × 4.37" (198.1mm × 132.1mm × 111.1mm)

#### ENVIRONMENTAL

Temperature Range, Rated Performance: -25°C to +85°C Storage Temperature Range: -55°C to +85°C Relative Humidity: Conforms to MIL-STD 202, Method 103 RFI Susceptibility: ±0.5% span error, SW @ 400MHz @ 3 ft.

#### VOL. II, 9-68 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS



# Alarm Limit Subsystem 4B Series



#### FEATURES/BENEFITS

• Low Cost, Completely Integrated 12-Channel Modular Alarm Limit Subsystem

Selection of Alarm Limit Modules Rugged Industrial Chassis, Rack or Surface Mounted On-Board Power Supplies Available

- Alarm Modules Accept High Level Voltage and Process Current Inputs
- Complete Alarm Function per Module High Accuracy of ±0.1% Two`Set Points, Adjustable Over 100% Span

Dead Band Adjustment per Set Point, Adjustable Over 0.5%-10.0% Span

Alarm Types are Configurable for HI or LO Operation Two Relay Outputs

Three Digit Display Indicates Set Points and Process Variable as a Percent of the Input Span LED per Set Point Provides Local Alarm Indication

Input Protection High RFI/EMI Immunity

- Specifications Valid Over the 0 to +70°C Temperature Range
- Easy to Install, Calibrate and Service
  Direct Connections to Industrial Screw Terminals
  Modules Removable without Disturbing Field Wiring or Power

Front Panel Set Point and Dead Band Adjustments

• Convenient Connection to User's Equipment Interfaces Directly to Analog Output Subsystems Used for Single Board Computer Interfaces Universal Adapter Board Allows Easy Interface to Any Equipment

#### **GENERAL DESCRIPTION**

The 4B Series Alarm Limit Subsystem is a low cost method of providing adjustable alarm limits to a variety of process sensors and transducers. It has been designed as a companion product to the 3B Series Signal Conditioning Subsystem, which interfaces directly to a variety of process sensors and transducers and converts the inputs to standardized high level analog outputs. The Alarm Limit Subsystem accepts the high level output from the 3B Series Subsystem or any other transmitter and provides fully independent HI and LO relay outputs.

The subsystem consists of a 19" relay rack compatible universal mounting backplane and a family of plug-in (up to 12 per rack) alarm limit modules. A four channel backplane is also available. The modules, designed for voltage or current inputs, can be readily mixed and matched and interchanged without disturbing field wiring. Each backplane incorporates screw terminals for field wiring and a connector for high level single ended inputs from the user's equipment.

Each alarm module has two set points which are fully adjustable over the 100% span. It will accept a standardized high level analog input and will provide one or two ON/OFF outputs. The allowable input ranges are  $\pm$  10V, 0 to + 10V, 4-20mA and 0-20mA. All input types can be connected to either the voltage input connector or the input screw terminals.

The two set points within each module can be user configured with push-on jumpers for HI-LO, HI-HI or LO-LO use. If only one limit per channel is desired, the module can be used in a HI or LO state. The value of each set point and the process variable can be viewed with a 3 digit display which is controlled with a rotary switch. Each set point has an adjustable dead band (hysteresis) which can be adjusted up to 10% of span and can be used to eliminate nuisance alarms.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

#### **DESIGN FEATURES AND USER BENEFITS**

Direct interface via screw-terminals or ribbon cable, two screwdriver adjustable set points per module, adjustable dead band per set point, a three digit display that indicates the value of the process variable and set points, and the modular design make the 4B Series Subsystem extremely easy to use. The subsystem features rugged packaging for the industrial environment and can be easily installed and maintained.

All input screw terminals offer 130V rms normal mode protection. Connection reliability is assured by gold plated pin and socket connectors. The high quality alarm modules feature  $\pm 0.1\%$ accuracy and a low drift with temperature ( $\pm 0.005\%$ /°C).

#### APPLICATIONS

The Analog Devices' 4B Series Alarm Limit Subsystem is designed to provide an easy and convenient solution to alarm/annunciation problems in measurement and control applications. In a typical application, the 4B Series Alarm Subsystem provides alarm indication for any sensor input when used with the 3B Series Signal Conditioning Subsystem. The 3B Series interfaces directly to sensors and converts the inputs to the standardized high level analog signal that the 4B Series alarms. This modular approach provides a very flexible means to alarm indication since the same 4B module can be used to alarm a variety of sensors when used with the appropriate 3B module. The 4B Series can also provide alarm indication or ON/OFF control when used with field transmitters or any other device that provides a process current or high level voltage output.

#### FUNCTIONAL DESCRIPTION

Each alarm module is a single channel unit that plugs into sockets on the backplane and accepts its signal from either the input screw terminals or the voltage input connector. All alarm modules provide input protection, filtering of the input signal, accuracy of  $\pm 0.1\%$  and feature two relay outputs that are capable of driving loads up to 3A.

The choice of a specific 4B module depends on whether the input signal is a high level voltage or a process current. The voltage inputs can be connected to a 4B module by either the input screw terminals or the voltage input connectors. Process currents can also be connected through either the screw terminals or the voltage input connector, but must use a sensing resistor. The current input models are shipped with the required sense resistor, which is to be installed on the input screw terminals.

- The transfer function provided by each alarm module is:
  - Inputs: High level voltage or process current Outputs: Two independent ON/OFF Relay Outputs

Figure 1 shows a functional diagram for the model 4B10 alarm limit module which has been configured for HI-LO operation. The high level voltage input signal is filtered and compared against both set points. If the process variable is above the HI limit or below the LO limit, the appropriate relay is turned on.

Each set point has an adjustable dead band (0.5%-10.0% span), which is used to eliminate nuisance alarms. Dead band is the amount of signal change necessary, after an alarm has occurred, to return an alarm to its original condition. As an example, if the HI limit is set at 75% of span and the dead band is 2%, the alarm will turn on when the process variable is at 75% and will not turn off until the process variable falls to 73%. For a LO limit configuration, the dead-band relationship is reversed and the alarm would not turn off until the process variable has risen above the sum of the LO set point value and the dead-band value.

Each set point has an LED which turns on when an alarm condition occurs and provides local alarm indication.



#### Figure 1. 4B10 Functional Block Diagram

The alarm status of both limits can be read externally from the digital I/O connector. When an alarm state exists which is TTL active high on the readback pins, the relay can be turned off with an external override signal (TTL active low) that connects to the digital I/O connector. The readback/override feature allows for external monitoring of the alarm states as well as for external control or alarm acknowledgement. When an override signal is used, the readback feature reads the alarm state and not the relay input signal so that the state of the process variable can still be monitored.

For the modules with a display, positive overload is indicated by  $\Box$  and negative overload is indicated by a  $\Box$  in the left most position.

The 4B modules have five user programmable jumper options. Each unit can be configured for unipolar or bipolar inputs, both set points can be configured for HI or LO limit operation, and both relays can be configured for Normally Open (NO) or Normally Closed (NC) operation. These options allow the user to readily tailor the 4B units to his specific needs. For instance, if HI-HI operation were required, it is available by changing the appropriate jumpers. All modules are shipped from the factory configured for unipolar input, NO relay action, and HI-LO operation.

# 4B MODULE SPECIFICATIONS

(typical @  $+25^{\circ}$ C and  $\pm 15V$ , +5V dc power) Model 4B10 4B20 4B11, 4B21 4B12, 4B22 Inputs<sup>1</sup>  $0 to + 10V, \pm 10V$ 4-20mA 0-20mA Outputs (2 SPST Relays) Resistive Rating: 3A (a 120V ac or 24V dc Performance ±0.1% span Accuracy Temperature Stability ± 0.005% span/°C Bandwidth<sup>3</sup> 5Hz (- 3dB) Normal Mode Input Protection 130V rms Normal Mode Rejection @ 50Hz or 60Hz 20dB 100MΩ Input Resistance Warm-Up Time to Rated Performance 3 Minutes Features Two Set Points per Module Adjustable over 100% span by 25 turn potentiometers Dead band per Set Point 0.5%-10.0% span, adjustable by I turn potentiometer **Relay Action** Field reversible by jumper change Three Digit Display<sup>5</sup> Alarm Status Readback 0-99.9% of input span TTL Level External Override Signal TTL Level Power Supply Voltage, Rated Performance  $\pm 15V. + 5V$ Voltage, Operating ± 12V to ± 18V, +4.5V to 5.5V Current ±12mA, +150mA Size<sup>7</sup> 4.020" × 1.050" × 4.020" Environmental Temperature Range, Rated Performance 0 to + 70°C Storage Temperature Range - 25°C to + 85°C Relative Humidity, Conforms to MIL. Std 202, Method 103B 0 to 95% @ 60°C, noncondensing **RFI** Susceptibility ± 0.5% span e 5W @ 400MHz @ 3 ft

NOTES

Voltage input range is jumper selectable. Accuracy includes setability, repeatability, linearity, and hysteresis. Models 4B10, 4B11, and 4B12 have a quantization error of  $\pm 1$  (gip). Unipolar inputs only. Bipolar inputs have a bandwidth of 10Hz (-3dB).

Uniposit imputs only. Biposit inputs have a input resistance of 1000K1. Uniposit inputs only. Biposit inputs have an input resistance of 4000K1. Only models 4810, 4811 and 4812 have a three digit display. "Only models 4810, 4811 and 4812. Models 4820, and 4821 require ± 12mA for ± 15V and + 125mA

from + 5V. Only applies to models 4B10, 4B11 and 4B12. Models 4B20, 4B21 and 4B22 measure 4.020" × 1.050" × 3.530". \*Specifications same as 4B10, 4B20

Specifications subject to change without notice.

VOL. II, 9-70 TEMPERATURE TRANSDUCERS & SIGNAL CONDITIONERS

# **Digital-to-Analog Converters**

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# Selection Guide Digital-to-Analog Converters

# **General Purpose 8-Bit D/A Converters**





### AD1408/AD1508

Improved Replacement for Industry Standard	Vol. I
1408/1508	9-265
Improved Settling Time: 250ns typ	
Improved Linearity: ±0.1% Accuracy Guaranteed	
Over Temperature Range (-9 Grade)	
High Output Voltage Compliance: +0.5V to -5.0V	
Low Power Consumption: 157mW typ	
High Speed 2-Quadrant Multiplying Input: 4.0mA/µs Slew Rate	
Single Chip Monolithic Construction	
Hermetic 16-Pin Ceramic DIP	

### AD DAC-08

Exact Replacement for Industry Standard DAC-08 Fast (85ns typical) Settling Time Linearity Error  $\pm 1/4$ LSB ( $\pm 0.1\%$ ) Guaranteed Over Full Temperature Range

Wide Output Voltage Compliance: - 10V to + 18V Single Chip Monolithic Construction 16-Pin Ceramic DIP Packaging Vol. I 9-89 10

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# **Selection Guide Digital-to-Analog Converters**

# **General Purpose 10-Bit D/A Converters**





### **AD DAC-100**

**Complete Current Output Converter High Stability Buried Zener Reference Single Chip Monolithic Construction** Wide Supply Range ±6V to ±18V **Trimmed Output Application Resistors** Fast Settling - 225ns (8 Bits), 375ns (10 Bits) **Guaranteed Monotonicity Over Full Operating Temperature Range** TTL and DTL Compatible Logic Inputs Hermeticaly-Sealed 16-Pin Ceramic DIP (All Grades)

### AD561

**Complete Current Output Converter High Stability Buried Zener Reference** Laser Trimmed to High Accuracy (1/4 LSB Max Error, AD561K, T) Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges Fast Settling - 250ns to 1/2LSB **Guaranteed Monotonicity Over Full Operating Temperature Range** TTL/DDT and CMOS Compatible (Positive True Logic) **Single Chip Monolithic Construction** 

Hermetically-Sealed Ceramic DIP (All Grades)

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## **General Purpose 12-Bit D/A Converters**









### AD565A

#### Single Chip Construction

Very High Speed: Settles to 1/2LSB in 250ns max Full Scale Switching Time: 30ns

High Stability Buried Zener Reference On Chip Monotonicity Guaranteed Over Temperature Linearity Guaranteed Over Temperature: 1/2LSB max (AD565AK, T)

Guaranteed for Operation with  $\pm$  12V Supplies Low Power: 225mW Including Reference Pin-Out Compatible with AD563, AD565

### AD566A

Single Chip Construction

Very High Speed: Settles to 1/2LSB in 350ns max Full Scale Switching Time: 30ns Guaranteed for Operation with – 12V Supply Monotonicity Guaranteed Over Temperature Linearity Guaranteed Over Temperature:

1/2LSB max (AD566AK, T) Low Power: 180mW Pin-Out Compatible with AD562, AD566

### **AD DAC80 SERIES**

Single Chip Construction On-Board Output Amplifier Low Power Dissipation: 300mW Monotonicity Guaranteed Over Temperature Guaranteed for Operation with ± 12V Supplies Improved Replacement for Standard DAC80 High Stability, High Current Output Buried Zener Reference

Laser Trimmed to High Accuracy: ±1/2LSB max Nonlinearity

Low Cost Plastic Packaging

Current Out Models and Voltage Output Models Available

### AD6012

1/2LSB max Differential Linearity Error Over Temperature 250ns Typical Settling Time Full Scale Current 4mA High Speed Multiplying Capability TTL/CMOS/ECL/HTL Compatible High Output Compliance: -5V to +10V Complementary Current Outputs Low Power Consumption: 230mW Page Vol. I 9-57

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# Selection Guide Digital-to-Analog Converters

# High Resolution D/A Converters





### AD DAC71/AD DAC72

16-Bit Resolution	Vol. I
±0.003% Maximum Nonlinearity	9-271
Low Gain Drift ±7ppm/°C	
0 to +70°C Operation (AD DAC71, AD DAC71H,	
AD DAC72C)	
-25°C to +85°C Operation (AD DAC72)	
Current and Voltage Models Available	
Improved Second-Source	

### DAC1136

16-Bit Resolution and Accura	icy
Low Cost	
Nonlinearity 1/2LSB	-
Settling to 1/2LSB (0.0008%)	in 6µs

### DAC1138

18-Bit Resolution and Accuracy (38μV, 1 Part in 62,144)

Integral Nonlinearity 1/2LSB Differential Nonlinearity 1/2LSB Settling to 1/2LSB (0.002%) in 10µs Hermetically-Sealed Semiconductors Vol. II 10–27

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### **DAC1146**

Low Cost, High Accuracy 18-Bit D/A Converter Integral Nonlinearity:  $\pm 0.00076\%$  FSR max Differential Nonlinearity:  $\pm 0.00076\%$  FSR max Low Differential Nonlinearity T.C.:  $\pm 1ppm/^{\circ}C$  max Wide Power Supply Operation:  $\pm 11.5V$  to  $\pm 16V$ Fast Settling: 6 µs to  $\pm 0.00076\%$  FSR Small Size 2"  $\times 2" \times 0.4"$ 

### HDD-1409

14-Bit Resolution 200kHz Word Rates RZ Gated Output 32-Pin DIP

APPLICATIONS FDM/TDM Transmultiplexers Digital Signal Processing PCM Systems Digital Audio

### AD569

Guaranteed 16-Bit Monotonicity Voltage Output, 6µs Settling Time Monolithic BIMOS Construction ±0.02% Nonlinearity 8- and 16-Bit Bus Compatible 6µs Settling Time Low Drift Low Power: 150mW Low Cost

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# Selection Guide Digital-to-Analog Converters CMOS Multiplying D/A Converters







### AD7523

8 Bits of Resolution Fast Settling: 100ns Low Power Dissipation Low Feedthrough: 1/2LSB @ 200kHz Full Four-Quadrant Multiplying Page Vol. I 9-167

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AD7533

Lowest Cost 10-Bit DAC Low Cost AD7520 Replacement Linearity: 1/2, 1 or 2LSB Low Power Dissipation Full Four-Quadrant Multiplying DAC CMOS/TTL Direct Interface Latch-Free (Protection Schottky Not Required) End-Point Linearity

### AD7525

Resolution: 3 1/2 Digit BCD (1999 Counts) Nonlinearity:  $\pm$  1/2LSB T<sub>MIN</sub> to T<sub>MAX</sub> Gain Error:  $\pm$  0.05% FS Excellent Repeatability Accuracy Low Power Dissipation



#### 



### AD7240

12 Bits of Resolution Fast Voltage Settling Time: 550ns to 0.01% Total Unadjusted Error: 1LSB max Single Supply Operation Latch-Up Proof (No Protection Schottky Required) Superb Differential Nonlinearity: 1/2LSB max Over Temperature Low Power Dissipation: 30mW

### AD7541A

12 Bits of Resolution Improved Version of AD7541 Full Four Quadrant Multiplication 12-Bit Linearity (End-Point) ±1LSB Gain Error All Parts Guaranteed Monotonic TTL/CMOS Compatible Protection Schottky not Required Low Logic Input Leakage

### AD7534

14 Bits of Resolution Y Full 4-Quadrnat Multiplication S Microprocessor Compatible with Double Buffered Inputs Exceptionally Low Gain Temperature Coefficient, Oppm/°C typ Small 20-Pin Package Low Output Leakage (<20nA) over the Full Temperature Range

All Grades 14-Bit Monotonic over the Full Temperature Range

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# Selection Guide Digital-to-Analog Converters

# **CMOS Multiplying D/A Converters**



### AD7546

16 Bits of Resolution	
Monotonic to 16 Bits Over Temperature	
On-Chip Deglitch Switch	
Unipolar and Bipolar Operation	
A	

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Microprocessor Compatible TTL/CMOS Compatible Latched Inputs

Voltage Output (Constant Output Impedance) Low Cost

Low Power Consumption: 50mW typ



Log D/A Converters





### AD7111

Dynamic Range: 88.5dB Resolution: 0.375dB On-Chip Data Latches Full ±25V Input Range Multiplying DAC Low Distortion Single +5V Supply Latch-Up Free (No Protection Schottky Required)

APPLICATIONS Digitally Controlled AGC Systems Audio Attenuators Wide Dynamic Range A/D Converters Sonar Systems Function Generators

### AD7115

Dynamic Range: 0 to 19.9dB Plus Full Muting Resolution: 0.1dB 2 1/2 Digit BCD Input Coding On-Chip Data Latches Full ±25V Input Range Low Distortion and Noise Latch-Up Free (No Protection Schottky Required) TTL Compatible **Page** Vol. I 9–109

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### AD7118

Dynamic Range 85.5dB	Vol. I
Resolution 1.5dB	9-123
Full ±25V Input Range Multiplying DAC	
Extended Temperature Range - 55°C to + 125°C	
Low Distortion	
Low Power Consumption	
Latch-Proof Operation (Schottky Diodes Not	
Required)	

# **Selection Guide** Digital-to-Analog Converters

# 8-Bit $\mu$ P-Compatible D/A Converters





### AD558

Complete 8-Bit DAC Voltage Output – 2 Calibrated Ranges Internal Precision Band-Gap Reference Single-Supply Operation: +5V to +15V Full Microprocessor Interface Fast: 1µs Voltage Settling to ±1/2LSB Low Power: 75mW No User Trims Guaranteed Monotonic Over Temperature All Errors Specified T<sub>min</sub> to T<sub>max</sub> Small 16-Pin DIP Package Single Laser-Wafer-Trimmed Chip for Hybrids

### AD7224

8-Bit DAC with Output Amplifier Full Double Buffering Microprocessor Compatible Single Supply Operation Multiplying Capability No User Trims Low Power 0.3" Wide 18-Pin DIP Vol. I 9–129

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### AD7226

Four 8-Bit DACs with Output Amplifiers 0.3" Wide, 20-Pin DIP Microprocessor Compatible TTL/CMOS Compatible No User Trims Single Supply Operation Possible Vol. I 9-133

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### AD7524

Microprocessor Compatible (6800, 8085, Z80, Etc.) TTL/CMOS Compatible Inputs On-Chip Data Latches End Point Linearity Low Power Consumption Monotonicity Guaranteed (Full Temperature Range) Latch-Free (No Protection Schottky Required)



### AD7528

Dual D/A Converter On-Chip Latches for Both DACs +5V to +15V Operation DACs Matched to 1% Four Quadrant Multiplication TTL/CMOS Compatible Latch-Free (Protection Schottkys Not Required) Vol. I 9–183 10

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# Selection Guide Digital-to-Analog Converters

## 12-Bit $\mu$ P-Compatible D/A Converters









### AD567

Single Chip Construction Double-Buffered Latch for 8-Bit µP Compatibility Fast Settling Time: 500ns max to ± 1/2LSB High Stability Buried Zener Reference on Chip Monotonicity Guaranteed Over Temperature Linearity Guaranteed Over Temperature: 1/2LSB max (AD567K, T)

Guaranteed for Operation with  $\pm 12V$  or  $\pm 15V$ Supplies

Low Power: 300mW Including Reference TTL/5V CMOS Compatible Logic Inputs

### AD667

Voltage Output Single Chip Construction Double-Buffered Latch for 8-Bit µP-Compatibility Fast Settling Time: 5ns max to ±1/2LSB High Stability Buried Zener Reference On Chip Monotonicity Guaranteed Over Temperature Linearity Guaranteed Over Temperature: 1/2LSB max (AD667K, T)

Guaranteed for Operation with  $\pm 12V$  or  $\pm 15V$ Supplies

Low Power: 300mW Including Reference TTL/5V CMOS Compatible Logic Inputs

### AD3860

Nonlinearity:  $\pm 1/2LSB T_{min}$  to  $T_{max}$ 12-Bit Input Register Small Size: 24-Pin DIP Fast Settling: 5µs to  $\pm 0.01\%$ Internal Reference Internal Output Amplifier Vol. I 9-93

### AD390

Four Complete 12-Bit DACs in One IC Package Linearity Error  $\pm 1/2$ LSB T<sub>min</sub> – T<sub>max</sub> (AD390K, T) Factory-Trimmed Gain and Offset Buffered Voltage Output Monotonicity Guaranteed Over Full Temperature Range Double-Buffered Data Latches

Includes Reference and Buffer

Fast Settling: 8µs max to ± 1/2LSB

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### AD7542

Nonlinearity: ± 1/2LSB T<sub>min</sub> to T<sub>max</sub> Low Gain Drift: 2ppm/°C typ, 5ppm/°C max Microprocessor Compatible Full 4-Quadrant Multiplication Low Multiplying Feedthrough Low Power Dissipation: 40mW max Small Size: 16-Pin DIP

### AD7543

Nonlinearity: ±1/2LSB T<sub>min</sub> to T<sub>max</sub> Low Gain T.C.: 2ppm/°C typ, 5ppm/°C max Serial Load on Positive or Negative Strobe Asynchronous CLEAR Input for Initialization Full 4-Quadrant Multiplication Low Multiplying Feedthrough: 1LSB max @ 10kHz Requires no Schottky Diode Output Protection Low Power Dissipation: 40mW max +5V Supply Small Size: 16-Pin DIP 10

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# Selection Guide Digital-to-Analog Converters

# 12-Bit $\mu$ P-Compatible D/A Converters





### AD7545

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Low Gain T.C.: 2ppm/°C typ Fast TTL Compatible Data Latches Single +5V to +15V Supply Small 20-Pin 0.3" DIP Latch Free (Schottky Protection Diode Not Required) Ideal for Battery Operated Equipment

### AD7548

8-Bit Bus Compatible 12-Bit DAC		Vol. I
All Grades 12-Bit Monotonic Over Full Temperature		9-247
Ranges		
Operation Specified at +5V, +12V or +15V	•	
Power Supply		
Low Gain Drift of 5ppm/°C Maximum		
Full 4-Quadrant Multiplication		
Small 20-Pin Package		
-		



**Video Display D/A Converters** 



### **HDG SERIES**

Ultra Fast 7ns Settling Time to 0.4% (8ns max) Low 50 pV-s max Glitch Energy Operates from Single -5.2V Power Supply **Complete Composite Inputs** Designed for General Output Compatibility with EIA Standard RS-170 and RS-343, Including **10% Brightness** HDG-0805 **Resolution: 8 Bits** % of Gray: 0.4% Settling Time: 8ns HDG-0605 **Resolution: 6 Bits** % of Gray: 1.6% Settling Time: 6ns HDG-0405 **Resolution: 4 Bits** % of Gray: 6.4% Settling Time: 4ns

### AD9700

Update Rates to 125MHz 2ns Rise Time On-Chip Reference Voltage Single – 5.2V Power Supply Complete Composite Inputs

APPLICATIONS Raster Scan Displays Color Graphics Automated Test Equipment TV Video Reconstruction Page Vol. 1 9-309

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# Selection Guide Digital-to-Analog Converters

# Video Display D/A Converters





### AD9768

8 Bits of Resolution 5ns Settling Time 100MHz Update Rate 20mA Output Current ECL-Compatible 40MHz Multiplying Mode Page Vol. I 9-261

### HDD SERIES

 HDD-0810 - 8 Bits of Resolution
 Vol. I

 HDD-1015 - 10 Bits of Resolution
 9-295

 Ultra Fast 10ns Settling Time to 0.2% (HDD-0810)
 15ns Settling Time to 0.1% (HDD-1015)

 Internal Monolithic Reference
 Low 200pV-s Glitch Energy

 Single - 5.2V Power Supply
 Designed for General Output Compatibility with EIA

 Standards RS-170 and RS-343, Including
 10% Brightness

 Complete Composite Inputs (HDD-0810C, HDD-1015C)
 HDD-1015C)

## Video Speed Current Output D/A Converters







### HDS-0810E/HDS-1015E

HDS-0810E: 8 Bits HDS-1015E: 10 Bits ECL Inputs Settling Time to 10ns Low Glitch Energy – 200pV-s 100MHz Update Rates Low Power <1 Watt

### HDS-0820/HDS-1025

HDS-0820: 8 Bits HDS-1025: 10 Bits 25ns Current Settling to 0.1% 10mA Current Out Guaranteed Monotonicity Over Temperature No External Parts Required Reliable Hybrid Construction

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### HDS-1240E

12 Bits of Resolution	Vol. I
12-Bit Settling Time to 40ns	9-323
Low Glitch Energy	
ECL Compatible	
Replacement for ADH-030, DA-4000, DAC397	

# Selection Guide Digital-to-Analog Converters

# Video Speed Voltage Output D/A Converters





### HDH SERIES

200ns Voltage Settling to 0.1%	
10mA Current Out	
Guaranteed Monotonicity Over Temperature	
No External Parts Required	
Reliable Hybrid Construction	
HDH-0802	
Resolution: 8 Bits	
Settling Time: 200ns to 0.4%	
HDH-1003	
Resolution: 10 Bits	
Settling Time: 300ns to 0.1%	
HDH-1205	
Resolution: 12 Bits	
Settling Time: 500ns to 0.125%	

### HDD-1206

12 Bits of Resolution Registers, D/A, Amplifier in Single Hybrid Deglitched Voltage Output 6MHz Update Rate



12-Bit Multiplying Accuracy Good Drive: 10.24mA Highest Speed Available Vol. I 9-315

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### VOL. II, 10-20 DIGITAL-TO-ANALOG CONVERTERS

# **Orientation** Digital-to-Analog Converters

### FACTORS IN CHOOSING A D/A CONVERTER

In the current issue of this two-volume catalog, there are listed some 62 different families of digital-to-analog converters (DACs). If one were to consider all the variations, there would be more than 260 types to choose among. The reason for so many different types is the number of degrees of freedom in selection-technological, functional, and performance. Complete information on converters may be found in the 250page book, ANALOG-DIGITAL CONVERSION NOTES, published by Analog Devices and available for \$5.95 from P.O. Box 796, Norwood MA 02062.

### **TECHNOLOGICAL FACTORS**

The technologies represented in these two volumes include modules (cards and potted circuits) and integrated circuits monolithic and hybrid. Modules historically have provided the extremes of performance and arbitrary levels of functional completeness (e.g., the 18-bit DAC1138, the 10-bit 20MHz-word-rate deglitched MDD-1020, and the isolated 10-bit DAC1423 loop DAC), although ICs are catching up rapidly.

The technical data in this volume embrace exceptionally high performance (high-resolution and high-speed) d/a converters, in the form of encapsulated modules. As the Selection Guide indicates, there is also a universe of technical data, to be found in Volume I, on a wide range of monolithic and hybrid d/a converters, including microprocessor-compatible types with resolution through 16 bits, and chips for hybrid assembly.

### FUNCTIONAL CHARACTERISTICS

The basic structure of all conventional D/A converters involves a network of precision resistors, a set of switches, and some form of level-shifting to adapt the switch drives to the specified logic levels. In addition, the device may contain outputconditioning circuitry, an output amplifier, a reference amplifier, an on-board reference, on-board buffer-registers (singleor dual-rank), configuration conditioning, and even highvoltage isolation.

### **Basic DAC**

This form, which supplies a current, and consequently a small voltage across its internal impedance or an external low-impedance load, is used principally for high speed. Basic currentoutput DACs are inherently fast, but additional elements (such as an output op amp), furnished by the user to meet overall system specs, slow down the conversion.

While the basic DAC function is almost always linear, there are exceptions. For example, the AD7111 LOGDAC, which has linear two-quadrant analog response, has a digitally controlled exponential gain function, i.e., 0.375dB per bit, a useful function in digital audio systems.

#### **Output Conditioning**

The analog quantity that is the "output" of a DAC, representing the input digital data, may be a "gain" (multiplying DAC), a current, and/or a voltage. In order to obtain a substantial voltage output at low impedance, an op amp is required. It is generally provided on-board in modular and hybrid DACs.

Almost all types of DACs provide one or more feedback resistors; they are matched to, and thermally track, resistances in the network, so that an external op amp, if used, will not require an external feedback resistor that might introduce tracking errors. If more than one feedback resistor is provided, a choice of analog output voltage ranges becomes available, e.g., 0-5V full-scale or 0-10V full-scale. If bipolar output-voltage ranges are specified, a bipolar-offset output is provided to subtract a half-scale value from the current flowing through the op amp summing point; it is usually derived from the DAC's reference (or analog) input to avoid additional tracking error. Multiplying DACs use an internal or external op amp for bipolar offset.

In addition to the usual zero-based current and voltage outputs, DACs are available with 4-to-20mA ISA-standard loopcurrent outputs, both direct-coupled (DAC1420/22) and highvoltage-isolated (DAC1423), with some additional features that are specifically useful in digital control of analog processes. In order to avoid difficulties, the user must pay especial attention to the specified output polarity, its relationship to the reference (if external) and to the input digital code. This can be especially tricky if the output is bipolar and the input requires a complementary (negative-true) digital coding. Another such case is where a current-output DAC, specified for a particular output-voltage polarity when used with an inverting op amp, is used in a mode that develops an output voltage passively (without the op amp) across an external resistive load. In addition to polarity, in this case, the user should be aware of the output-compliance constraint and the specified resistive component of output impedance.

#### **Reference Input**

The reference may be specified as external or internal, fixed or variable, single-polarity or bipolar. If internal, it may be permanently connected (as in the DAC1106/1108) or optionally connectible (as in the DAC1136/1138). If the DAC is a 4quadrant multiplying type, the reference (or "analog input") is external, variable, and bipolar. The user should check a converter's specifications to determine whether the fullscale accuracy specifications are overall or subdivided into a converter-gain spec and a reference spec.

#### **Digital Data**

There are a number of ways in which converters differ in regard to the input data: First, the *coding* must be appropriate (binary, offset-binary, two's-complement, BCD, arbitrary, etc.), and its sense should be understood (positive-true, negative-true). The *resolution* (number of bits) must be sufficient; in addition, the specifications must be checked to ascertain that the  $2^n$  distinct binary input codes will not only be accepted, but that also they will (if necessary) correspond to  $2^n$  output values in a monotonic progression at any temperature in the operating range, with sufficient accuracy. The data levels accepted by the converter must be checked (TTL, ECL, low-voltage CMOS, high voltage CMOS), as must the input loading imposed by the converter, and the supply conditions under which the converter will respond to the data. Check the data notation (is the MSB Bit 1 or Bit (n-1)?)-misinterpretation can lead to connecting the data bits in backward order. If *buffer registers* are desired, the converter should have an appropriate buffer configuration. The data can be clocked in, while the DAC output remains unchanged.

### Controls

If the DAC has external digital controls—for example, register strobes— their drive levels, digital sense (true or false), loading, and timing must be considered. The function and use of configuration controls (where present), such as serial/parallel, short-cycle, or chip-select decoding should be understood, and the appropriate ways of disabling them when not needed should be employed.

#### **Power Supplies**

Appropriate power supplies should be made available, considering the logic levels and analog output signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specs should be employed. Any recommended external protection circuitry (e.g., Schottky diodes, to ensure that  $V_{CC}$  is never more than 0.4V above  $V_{DD}$  in the AD7522) should be planned for. In many cases separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between the grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

For video converters, use massive, low impedance ground systems. The analog and digital grounds are connected together inside converters of these types, so bus bars are essential for system grounding and power distribution; use lots of ground plane on PC boards.

### SPECIFICATIONS AND TERMS

Definitions of the performance specifications, and related information, are provided on the next few pages, in alphabetical order.

### Accuracy, Absolute

Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Error is usually commensurate with resolution, i.e., less than  $2^{-(n + 1)}$ , or "½ LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01% of each ideal value.

Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

### Accuracy, Relative

Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated. Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative-accuracy error of a linear DAC can be interpreted as a measure of nonlinearity (see *Linearity*).

### Compliance-Voltage Range

For a current-output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

#### Common-Mode Rejection (CMR)

The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually a logarithmic expression representing a "common-mode rejection ratio" e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 10<sup>6</sup>:1 means that a 1V common-mode voltage passes through the device as though it were a differential input signal of 1 microvolt.

### **Common-Mode Voltage**

An undesirable signal picked up in a circuit by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

#### Deglitcher

As the input code to a DAC is increased or decreased by small changes, it passes through what is known as major and minor transitions. The most major transition is at half-scale, when the DAC switches around the MSB, and all switches change state, i.e., 01111111 to 10000000. If, at major transitions, the switches are faster (or slower) to switch off than on, this means that, for a short time, the D/A will give a zero (or fullscale) output, and then return to the required 1 LSB above the previous reading. Such large transient spikes which differ widely in amplitude and are extremely difficult to filter out, are commonly known as "glitches", hence, a deglitcher is a device which removes these glitches or reduces them to a set of small, uniform pulses. It normally consists of a fast samplehold circuit, which holds the output constant until the switches reach equilibrium. Glitch energy is smallest in fast-switching DACs driven by fast logic gates that have little time-skew between 0-1 and 1-0 transitions.



### Feedthrough

Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplying DAC. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

#### Four-Quadrant

In a multiplying DAC, "four quadrant" refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign.

#### Gain

The "gain" of a converter is that analog scale-factor setting that provides the nominal conversion relationship, e.g., 10V span for a full-scale code change, in a fixed-reference converter. For fixed-reference converters where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain- and zero-adjustment are discussed under Zero.

### Least-Significant Bit (LSB)

In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value, or weight. For example, in the natural-binary number 1101 (decimal 13, or  $2^3 + 2^2 + 0 + 2^0$ ), the rightmost digit is the LSB. Its analog weight, relative to full scale, is  $2^{-n}$ , where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n-bit converter.

### Linearity

Linearity error of a converter (also, *integral nonlinearity*, see Linearity, Differential), expressed in % or ppm of full-scale range, or (sub)multiples of 1 LSB, is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight



a. %LSB Nonlinearity Achieved By Arbitrary Location of "Best Straight Line". b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of a.

Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification. line", determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristics from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (sometimes referred to as "end-point" linearity). End-point linearity error is similar to relative-accuracy error.

For multiplying D/A converters, the *analog* linearity error, at a specified digital code, is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

#### Linearity, Differential

Any two adjacent digital codes should result in measured output values that are exactly 1 LSB apart  $(2^{-n} \text{ of full scale for an} n-bit converter). Any deviation of the measured "step" from$ the ideal difference is called*differential nonlinearity*, expressedin (sub)multiples of 1 LSB. It is an important specification,because a differential linearity error greater than 1 LSB canlead to non-monotonic response in a D/A converter andmissed codes in an A/D converter (see*Differential Linearity* in the A/D converter section for an illustration).

#### Monotonic

A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases, with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a differential nonlinearity specification, since differential nonlinearity less than 1 LSB is a sufficient condition for monotonic behavior.

### Most-Significant Bit (MSB)

In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the natural-binary number 1101 (decimal 13, or  $2^3 + 2^2 + 0 + 2^0$ ), the leftmost "1" is the MSB, with a weight of  $2^{n-1}$ , or 8 LSBs. Its analog weight, relative to a DAC's fullscale span, is <sup>1</sup>/<sub>2</sub>. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits.

#### Multiplying DAC

A multiplying DAC differs from a fixed-reference DAC in being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the "reference" (i.e., analog input) voltage and the fractional equivalent of the digital input number (see also four-quadrant).

### Noise, Peak and rms

Internally generated random noise is not a major factor in D/A converters, except at extreme resolutions (e.g., DAC1138) and dynamic ranges (AD7111). Random noise is characterized by ms specifications for a given bandwidth, or as a spectral density (current or voltage per root hertz); if the distribution is Gaussian, the probability of peak-to-peak values exceeding 7x the rms value is less than 0.1% (see the waveform table in Section 7).

Of much greater importance in DACs is interference in the form of high-amplitude low-energy (hence low-rms) spikes appearing at the DAC's output, caused by coupling of digital signals in a surprising variety of ways; they include coupling via stray capacitance, via power supplies, via inadequate ground systems, via feedthrough, and by glitch-generation. Their presence underscores the necessity for maximum application of the designer's art, including layout, shielding, guarding, grounding, bypassing, and deglitching.

#### Offset

For almost all bipolar converters (e.g.,  $\pm 10$ -volt output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1 MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference, because the ½ scale offset cancels the weight of the MSB at zero, independently of the amplitude of both.

### Power-Supply Sensitivity

The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (or fractions of 1 LSB) for a 1% dc change in the power supply, e.g.,  $0.05\%/\%\Delta V_S$ ). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed ±½ LSB for a 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

### Quantizing Uncertainty (or "Error")

The analog continuum is partitioned into  $2^n$  discrete ranges for n-bit processing. All analog values within a given range of output (of a DAC) are represented by the same digital code, usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of  $\pm 1/4$  LSB, due to limited resolution, in addition to the actual conversion errors. For applications in which discrete output levels are desired (e.g., digitally controlled power supplies or digitally controlled gains), this consideration is not relevant.

### Resolution

An n-bit binary converter should be able to provide 2<sup>n</sup> distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a *resolution* of n bits. The smallest output change that can be resolved by a linear DAC is 2<sup>-n</sup> of the fullscale span. However, a nonlinear device, such as the AD7111 LOGDAC has a logarithmic gain resolution of 0.375/88.5dB= 1.256dB, which corresponds to a gain increment of 4.25/step, or 26,600:1.

#### Settling Time

The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction

(usually ±½ LSB) of the final value. Typical prescribed changes are full-scale, 1 MSB, and 1 LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

### Slew Rate (or Slewing Rate)

Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of a few  $V/\mu s$  are common, and moderate in cost. Slew rates greater than about 75 volts/ $\mu s$  are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

### Stability

Stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficient").

### Staircase

A voltage or current, increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot), generated by applying a pulse train to a counter, and the output of the counter to the input of a DAC.

A very simple A/D converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1 LSB, the count is stopped, and the code corresponding to the count is the digital output.

#### Switching Time

In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10%-90%), but does not include settling time, e.g. to  $\leq$ ½ LSB.

#### **Temperature Coefficients**

In general, temperature instabilities are expressed as %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include gain, linearity, offset (bipolar), and zero.

Gain Tempco: Two factors principally affect converter gain stability with temperature.

a) In fixed-reference converters the reference source will vary with temperature. For example, the tempco of an AD581L is generally less than 5ppm/°C.

b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters (e.g. AD566K/T).

High-resolution converters require much better tempcos for accuracy commensurate with the resolution.

Linearity Tempco: Sensitivity of linearity ("integral" and/ or differential linearity) to temperature (in % FSR/°C or ppm FSR/°C) over the specified range. Monotonic behavior is achieved if the differential nonlinearity is less than 1 LSB at any temperature in the range of interest. The differential nonlinearity temperature coefficient may be expressed as a ratio, as a maximum change over a temperature range, and/or implied by a statement that the device is monotonic over the specified temperature range.

**Offset Tempco:** The temperature coefficient of the all-DAC-switches-off (minus full scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors:

a) The tempco of the reference source

b) The voltage zero-stability of the output amplifier

c) The tracking capability of the bipolar-offset resistors and the gain resistors

Unipolar Zero Tempco (in % FSR/°C or ppm FSR/°C): The temperature stability of a unipolar fixed-reference DAC is principally affected by current leakage (current-output DAC), and offset voltage and bias current of the output op-amp (voltage-output DAC).

#### Zero- and Gain-Adjustment Principles

The output of a unipolar DAC is set to zero volts in the allbits-off condition. The gain is set for F.S.  $(1 - 2^{-n})$  with all bits on. The "zero" of an offset-binary bipolar DAC is set to -F.S. with all bits off, and the gain is set for +F.S.  $(1 - 2^{(n-1)})$ with all bits on. The data sheet instructions should be followed.

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### VOL. II, 10-26 DIGITAL-TO-ANALOG CONVERTERS



# High Resolution 16- and 18-Bit Digital-to-Analog Converters DAC1136/1138

### FEATURES

#### DAC1138

18-Bit Resolution and Accuracy ( $38\mu$ V, 1 Part in 262,144) Nonlinearity 1/2LSB max (DAC1138K) Excellent Stability Settling to 1/2LSB (0.0002%) in 10 $\mu$ s Hermetically-Sealed Semiconductors

#### DAC1136

16-Bit Resolution and Accuracy (152µV, 1 Part in 65,536) Low Cost Nonlinearity 1/2LSB max (DAC1136K, L)

Settling to  $1/2LSB \max (0.0008\%)$  in  $6\mu s$ 

### DEGLITCHER IV

Eliminates DAC Glitches Available on DAC1136/1138 Card-Mounted Assembly

### **GENERAL DESCRIPTION**

The DAC1136/1138 are complete self-contained current or voltage output modular digital-to-analog converters with resolutions and accuracies of 16 and 18 bits.

The DAC1136/1138 combine precision current sources with state-of-the-art steering switches to produce a very linear output. Inputs to these converters are compatible with TTL levels. The converters have a current output of -2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V, ±5V, or ±10V.

The DAC1136/1138 are available on Card-Mounted Assemblies. In this configuration, selectable options include: input codes, output amplifiers, and a high speed transient-suppressing Deglitcher Module, Deglitcher IV.

### WHERE TO USE HIGH RESOLUTION DACS

The DAC1136/1138 deliver exceptional accuracy for a broad range of display, test and instrumentation applications. The DAC1136, with a resolution of 16 bits or 1 part in 65,536, and the DAC1138 with a resolution of 18 bits or 1 part in 262,144 are ideally suited for applications requiring wide dynamic range measurement and control. Applications include data acquisition systems, high resolution CRT displays, automatic semiconductor testing, photo-typesetting, frequency synthesis and nuclear reactor control.



### **CERTIFICATE OF CALIBRATION**

Each DAC1138 has been calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A Certificate of Performance is sent with each unit, which includes 1000 hour stability data for the reference zener and linearity test data.



Figure 1. Block Diagram and Pin Designations

**SPECIFICATIONS** (typical @ + 25°C, rated power supplies unless otherwise noted; specifications for mounting card with amplifier/deglitcher options same as module unless otherwise noted)

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			DAC1136 on Mounting Card with			
			Amplifier/Deglitcher Options.			
	DACI136 Module		Deglitcher IV Low Drift 234L High Speed 44K (Internal AD542K) w/wo Deglitcher w/wo Deglitcher			
RESOLUTION, BITS		16	1			· · · · · · · · · · · · · · · · · · ·
ACCURACY						
Integral Nonlinearity	± 1LSB max	± 1/2LSB max	± 1/2LSB max			
Differential Nonlinearity	± 1LSB max	± 1/2LSB max	± 1/2LSB max			
Gain and Offset Error (Externally Adjustable)		1	1	Gain, offset	and glitch-nulling a ded on the mounting	ajustments
ANALOGOUTPUT				pion		
Unipolar Mode		- 2mA to 0mA				
Bipolar Mode	ſ	- 1mA to + 1m/	A '			
Voltage Output Range (Pin Selectable)	0 to +	$-5V,0$ to $+10V, \pm 5$	5V, ±10V			
DIGITAL INPUTS	1	TTL/CMOS; See Fig	gure 2			
INPUT CODES						
Unipolar Mode Binalar Mode	Compl	lementary Binary (C	COMPBIN)	BIN, COMP BIN, 2'S COMP, COMP 2'S COMP OBIN, COMP OBIN SIGN PLUS MAG BIN, COMP SIGN PLUS MAG BIN		
Bipolar Mode	Compleme	ntary Offset Binary	(COMPOBIN)			
STROBEINPUT		None		One standar	d series 741 Sload 1	eading-edge
STROBEINIOT		None		triggered,	pulse width 100ns n	ninimum.
DYNAMICCHARACTERISTICS					•	
Settling Time to 1/2LSB						
Current						
Full Scale Step		δμς δυς			oltage Output, Only	y v
Voltage		0,00			onuge output, on	,
Unipolar (10V Step)		90µs		80µs	45µs	25µs
Bipolar (20V Step)		250µs		90µs	60µs	30µs
LSB Step Slew Rate	4	8μs 1V/μs		δμs 2V/μs	δμs 6V/μs	8μs 20V/μs
TEMPERATURE COEFFICIENTS	· · · ·					
(ppm of FSR/°C) <sup>1</sup>						
Integral Nonlinearity	±1	±1	$\pm 1.5  \text{max}$			
Differential Nonlinearity	±1	±1	± 1.5 max		· •	
Offset	±,	Ξ <b>Σ</b> Ι	± 8 max			
Unipolar Mode		±0.5		±0.5	±0.1	±2
Bipolar Mode		± 5				
STABILITY, LONG TERM				1. Sec. 1. Sec		
(ppm of FSR/1,000 hrs.) <sup>2</sup> (Sain (Excluding V-v-v)		+ 5				
Offset		±6		±1	±0.5	±25
NOISE (Include V <sub>REF</sub> ; Double for						
Bipolar Mode)						_ +
Output Current (BW = $100 \text{kHz}$ )		0.5nA rms			Voltage Output,	Only
$(u \ 0V(A111)^{\circ} Code; "ZERO")$		4uV pk-pk				
(it 5V (MSB = 0 Code; "Half Scale")		6µV pk-pk				
("10V (A110's Code; "Full Scale")		9μV pk-pk		I.		
Output Voltage (BW = 100kHz)		30µV rms		20µV rms	40µV rms	35µV rms
VOLTAGE COMPLIANCE (Amplifier						
Max Eos Allowed for Rated Accuracy		±2mV max			=.	· · ·
Initial E <sub>OS</sub> (Factory Adj.)		± 100µV		± 50μV	$\pm 20 \mu V$	±100µV
E <sub>os</sub> Drift		±10µV/°C		±5µV/°C	±0.1µV/°C	±15µV/°C
Voltage Protection	vi	a Internal Schottky I	Diodes			
Source Resistance		a milernar benotiky i	Diodes			
Unipolar Mode		≥33kΩ	-		*	
Bipolar Mode		>5kΩ				
		Topr				
$Voltage(Z_{outr} \approx 200\Omega)$	+6.000	V (Maximum Error	r. +0.024V)			•
Noise $(BW = 0.1-10Hz)$		3μV pk-pk	,,			
Тетрсо		5ppm/°C				
POWER SUPPLY REQUIREMENTS <sup>3</sup>						
$+5Vdc, \pm 5\%$		9mA + 20m A		+ 39 - 4	95mA	+ 40m A
$= 157 \text{ uc}, \pm 370$ DOWED SUDDLY DELECTION ( $\pm 157.3$		± Joint		± 30000	± 3/mA	± 40mA
Gain or Offset vs. FSR		80dB		100dB	100dB	75dB
Differential Nonlinearity		± 1/4LSB per Volt	ΔVs		100415	1 , 500
ENVIRONMENTAL				1.		· · · · · · · · · · · · · · · · · · ·
Operating Temperature	t	0 to + 70°C	_	I	1	
Storage Temperature		- 55°C to + 85°C	C	- 55°C to + 80°C	-55°C to +8	5°C - 55°C to + 85°C
Humany		7010 93%, NOLICOND	ensmig	J		

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NOTES <sup>1</sup>Maximum temperature coefficients guaranteed from 15°C to 35°C, typical from 0 to +70°C. <sup>7</sup>Recommended DNL calibration check: 6 months.

<sup>3</sup>Recommended Power Supply: Analog Devices Model 923. Specifications subject to change without notice.

**SPECIFICATIONS** (typical @ +25°C, rated power supplies unless otherwise noted; specifications for mounting card with amplifier/deglitcher options same as module unless otherwise noted)

.....

			DAC1138 on Mounting Card with		
	DACING M.		Amplifier/Deg	litcher Options.	
	I DACI138 MOO	luie	(Internal AD542K)	Low Drift 234L w/wo Deplitcher	
RESOLUTION BITS		18	(	www.obegmener	
ACCURACY		10			
Integral Nonlinearity	± 1LSB max	± 1/2LSB max			
Differential Nonlinearity	± 1LSB max	± 1/2LSB max			
Gain and Offset Error (Externally Adjustable)		±1LSB	Gain, offset and glitch	-nulling adjustments	
			provided on the	mounting card.	
ANALOG OUTPUT		2m A to 0m A			
Bipolar Mode	-	1mA to + 1mA			
Voltage Output Range (Pin Selectable)	0 to + 5V,0	$to + 10V, \pm 5V, \pm 10V$			
DIGITAL INPUTS	TTL/C	MOS; See Figure 2			
INPUT CODES					
Unipolar Mode	Complement	tary Binary (COMP BIN)	BIN, COMP BIN, 2's C	COMP, COMP 2's COMP	
Bipolar Mode	Complementary	Offset Binary (COMPOBIN)	OBIN, C	OMPOBIN	
			SIGN PLUS MAG BIN, CO	MF SIGN FEUS MAG BIN	
STROBEINPUT		None	Une standard series /	4LS load, leading-edge	
DVNA MIC CHARACTERISTICS			inggerea, puise wi		
Settling Time to 1/2LSB					
Current					
Full Scale Step		10µs	Voltage O	utput, Only	
LSB Step Voltage		ծμs	Voltage O	utput, Only	
Unipolar (10V Step)		175µs	80µs	45µs	
Bipolar (20V Step)		140µs	90µs	60µs	
LSB Step		18µs	18µs	18µs	
Siew Rate		2ν/μs	2ν/μs	bv/μs	
TEMPERATURE COEFFICIENTS					
Integral Nonlinearity		±0.3			
Differential Nonlinearity		±0.4			
Gain (Excluding V <sub>REF</sub> )		±0.8			
Utiset Unipolar Mode		+05	+0.5	+01	
Bipolar Mode		±1	0.5	- 0.1	
STABILITY, LONG TERM					
(ppm of FSR/1,000 hrs.) <sup>2</sup>					
Gain (Excluding V <sub>REF</sub> )		±2			
		±2 ,	±1	±0.5	
NOISE (Include V <sub>REF</sub> ; Double for Bipolar Mode)					
Output Current (BW = 100kHz)		0.5nA rms	Voltage Ou	tput, Only	
Output Voltage (BW = 0.1-10Hz)					
(w OV (AII I's Code; "ZERO")		4µVpk-pk 6uVpkpk			
(w 10V (A11 0's Code; "Full Scale")		9μV pk-pk			
Output Voltage (BW = 100kHz)		30µV rms	20µV rms	40µV rms	
VOLTAGE COMPLIANCE (Amplifier					
Offset, Eos)					
Max Eos Allowed for Bated Accuracy		+ 200 u V max	·		
Initial $E_{OS}$ (Factory Adj.)		$\pm 100 \mu V$	± 50µV	$\pm 20 \mu V$	
E <sub>OS</sub> Drift		±10µV/°C	±5µV/°C	±0.1µV/°C	
Current Output (pin 69)		10.1			
Source Resistance	via inter	nai Schottky Diodes			
Unipolar Mode		>33kΩ			
Bipolar Mode		>5kΩ			
Source Capacitance		150pF			
REFERENCE VOLTAGE (V <sub>REF</sub> )	. ( 00037/14			1	
Noise (BW = $0.1-10$ Hz)	+ 0.000 V (M	3uV nk-nk			
Tempco		5ppm/°C		·	
POWER SUPPLY REQUIREMENTS <sup>3</sup>					
$+5V dc, \pm 5\%$		9mA		95mA	
± 15V dc, ± 5%		± 30mA	± 38mA	± 37mA	
POWER SUPPLY REJECTION (±15V dc)		00.17	10.1.1		
Gain of Oliset vs. FSK Differential Nonlinearity	+ 1/4	80dB I SB per Volt AV.	100dB	75dB	
ENVIRONMENTAL	1/4			·····	
Operating Temperature		0 to + 70°C			
Storage Temperature	-	55°C to + 85°C	- 55°C to + 80°C	55°C to + 85°C	
riundany	5% to 9	o 70, inoncondensing			

NOTES Maximum temperature coefficients guaranteed from 15°C to 35°C, typical from 0 to +70°C. \*Recommended DNL calibration check: 6 months.

<sup>3</sup>Recommended Power Supply Analog Devices: Model 923. Specifications subject to change without notice.

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### **Characteristic Curves**\*











Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for LSB Steps (Essentially Independent of Amplifier Used). With Deglitcher IV, the LSB Step at the Major Carry Settles as Fast as the Typical LSB Step, Following the 11µs Hold Period.

### INPUT CONSIDERATIONS

The DAC1136/1138 may be driven by TTL or CMOS as shown in Figure 2. Note that the TTL input is shown with inputs for both a direct "totem pole" TTL gate and open collector (or "pull-up") configurations.



2a. TTL Totem Pole<sup>1</sup>

2b. Switch or Relay Input<sup>2</sup>



2c. CMOS Input

1. FOR TTL WITH OPEN COLLECTOR, DO NOT USE EXTERNAL PULL-UP. CONVERTERS HAVE INTERNAL 10kΩ PULL-UP ON EACH INPUT TO 3.8V.

2. USE SPST SWITCH OR RELAY TO GROUND, WHEN SWITCH IS OPEN, THE INTERNAL 10kΩ WILL PULL INPUT UP TO 3.8V.

### Figure 2. Input Connections

OUTPUT CONNECTIONS AND GUARDING The DAC1136/1138 output connections for various voltage ranges are shown in Figure 3.

Since an LSB is only  $38\mu$ V (at 10 volts full scale for the DAC1138), care must be exercised to properly guard the current output of the converter from leakage current. Any connection made to the DAC's current output (pin 69) should be guarded. Suggested printed circuit board guarding is shown in Figure 3. The optional Card-Mounted Assemblies of the DAC1136/1138 have been carefully designed for optimum guarding and performance.



Figure 3. Output Voltage Connections and Suggested PCB Guarding (Unipolar and Bipolar)

•NOTE: All curves typical at rated supply voltage. F.S. = Full Scale

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### GAIN AND OFFSET ADJUSTMENTS

The gain and offset adjustments are made with external potentiometers which the user supplies. With the appropriate digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The proper connections for offset and gain are shown in Figure 4. The voltmeter used to measure the output should be capable of stable resolution of 1/4LSB in the region of zero and full scale. Because of the interaction between offset and gain adjustments, the adjustment procedure described below should be carefully followed. Offset adjustment affects gain, but gain adjustment does not affect offset.





### Figure 4. Gain and Offset Adjustments

For unipolar mode, apply a digital input of all "1's" (complementary binary code for zero output) and adjust the offset potentiometer until a 0.00000V output is obtained (see Table I). Once the appropriate offset adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output is obtained (see Table I).

For bipolar mode, apply a digital input of all "1's" (complementary offset binary code for minus full scale) and adjust the offset potentiometer for the proper minus full scale output voltage (see Table I). Once the appropriate minus full scale adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output shown below is obtained.

RANGE	IDEAL OUTPUT			
		DAC1138	DAC1136	
Unipolar	All 111		00	
$0V \rightarrow +10V$	0.00000V	+9.999962V	+9.999848V	
$0V \rightarrow +5V$	0.00000V	+4.999981V	+4.999924V	
Bipolar:				
-10V→+10V	-10.00000V	+9.999934V	+9.999695V	
$-5V \rightarrow +5V$	-5.00000V	+4.999962V	+4.999848V	
		$\sim$	~	
To adjust:	Adjust ZERO pot	Adjust G	AIN pot	

Table I. Full Scale Output

### DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1136/1138 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Before attempting recalibration, it is imperative that the circuit be checked to confirm that all previously described precautions have been taken to insure proper application at the 16- or 18-bit level. Basically, the DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusting, if necessary, for a one LSB positive difference. The top 4 major carries, i.e., MSB minus the sum of bits 2-through-the-LSB, down through bit 4 minus the sum of bits 5-through-the-LSB, can be trimmed using the procedure outlined below. A differential voltmeter capable of 100µV Full Scale should be connected to VOUT of the DAC. This will resolve an LSB which at 18 bits is 38µV (10V range). A Fluke 895A or equivalent is recommended.

- 1. Bit 4 Trim
  - a. Set bit inputs to 11110 . . . 0.
  - b. Read the output voltage by nulling the voltmeter.
  - c. Set bit inputs to 11101 . . . 1.
  - d. Read voltage by nulling voltmeter. This reading should be equal to that of step 1b plus 1LSB. Adjust bit 4 if required (see B4, Figure 6).

#### 2. Bit 3 Trim

- a. Set bit inputs to 1110 . . . 0.
- b. Read output voltage by nulling the voltmeter.
- c. Set inputs to 1101 . . . 1.
- d. Read voltage by nulling the voltmeter. This reading should be equal to that of step 2b plus 1LSB. Adjust bit 3 if required (see B3, Figure 6).
- 3. Bit 2 Trim
  - a. Set bit inputs to 110 . . . 0.
  - b. Read output voltage by nulling the voltmeter.
  - c. Set bit inputs to 101 . . . 1.
  - d. Read voltage by nulling voltmeter. This reading should be equal to that of step 3b plus 1LSB. Adjust bit 2 if required (see B2, Figure 6),
- 4. Bit 1 (MSB) Trim
  - a. Set bit switches to 100 .... 0.
  - b. Read output voltage by nulling the voltmeter.
  - c. Set bit switches to 011 . . . 1.
  - d. Read voltage by nulling voltmeter. This reading should be equal to that of step 4b plus 1LSB. Adjust bit 1 (MSB) if required (see MSB, Figure 6).

If insufficient range exists on any adjustment, then a separate adjustment for the weight of bits 5-through-the-LSB (see Sum  $B5 \rightarrow LSB$ , Figure 6) should be performed. This condition will probably not occur on bit 2, 3 and 4 but might occur on the MSB. If adjustment of the sum of bits 5-through-the-LSB is made, the trim procedure for all bits should be repeated. Obviously, since the procedure affects the weight of individual bits, it affects the overall gain of the DAC. The final step should be adjustment of gain (user supplied adjustment external to module, or pot at edge of mounting card).

### OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



NOTES: 1. PINS: 0.019 ±0.001 DIA.

0.150

2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.

3. PINS 27 AND 29 ARE NOT PRESENT ON DAC1136.

**USING AN EXTERNAL 6V REFERENCE** 

The DAC1136/1138 can be operated with an external reference connected to pin 53 of the module. The current drain on the external reference will be 1.125mA in bipolar mode or 0.125mA in unipolar mode (pin 46 should be left open and not grounded when using an external reference in the unipolar mode). When an external reference is used, pin 52, (the output of the internal reference) is left open.

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Codi Semiconductor manufactures a reference module called Certavolt<sup>1</sup> with a 10 volt output accurate to 0.001%. This output is temperature compensated to within 1ppm/°C from +15°C to +55°C. The Certavolt requires a power supply of +28V dc @ 20mA. To convert the +10 volt output of the Certavolt to the +6 volt reguired by the DAC, the circuit shown in Figure 5 is recommended.

<sup>1</sup>Certavolt is a registered trade name by Codi Semiconductor.



Figure 5. DAC1136/1138 with External Precision Reference

#### OPTIONAL CARD-MOUNTED ASSEMBLY

Analog Devices offers an optional Card-Mounted Assembly designed to provide optimum performance at the 18-bit level. As shown in Figure 6, this 4  $1/2'' \times 6''$  printed circuit card includes the appropriate DAC GAIN and OFFSET adjustment potentiometers, power supply bypass capacitors and input registers. The Card-Mounted Assembly can be ordered with custom code-setting logic, external output amplifiers, and a Deglitcher IV.



Figure 6. Card-Mounted Assembly. Dimensions shown in inches and (mm).

### CARD-MOUNTED ASSEMBLY JUMPER DESIGNATIONS

The output voltage range, reference source, amplifier and deglitcher configurations are programmed at the factory by means of jumpers, resistors, and capacitors (see ordering guide for details). The mounting card can be programmed by the user, if necessary, as shown below.

Output Voltage Range	Install Jumpers
±10V	W10, W5
±5V	W12, W5
+10V	W12, W3
<u>Reference</u> Internal External	Install Jumpers W2 W1
<u>Amplifier</u> Internal External <sup>1</sup> Deglitcher IV <sup>2</sup> Deg. IV with Ext Amp <sup>3</sup>	Install Jumpers W4, W9 W8, W13 W8, W15, W17, W18 W8, W14, W16

NOTES:

- <sup>1</sup> With a 234L amplifier install C7 (0.01μF, 10%, ceramic capacitor). With a 44K amplifier use a variable resistor (typ value ≈ 499Ω, 0.1W, 1%) to adjust the output voltage for a ±100μV reading as measured between pins 69 and 34 of the DAC (this step sets voltage compliance); install this value resistor (R13 position).
- <sup>2</sup>With Deglitcher IV remove R20 (100 $\Omega$ ) and replace the resistor with a jumper.
- <sup>3</sup> With Deglitcher IV and a 234L amplifier remove C6 (6.8pF Capacitor) and install: C7 (0.01 $\mu$ F, 10%, ceramic capacitor), C18 (100pF, 10%, ceramic capacitor), C17 (1000pF, 10%, polystyrene capacitor) and replace R20 (1002) with a jumper. With Deglitcher IV and a 44K amplifier perform the operation described in Note 1, remove C6 (6.8pF capacitor) and install: C18 (100pF, 10%, ceramic capacitor), C17 (1000pF, 10% polystyrene capacitor) and replace R20 (1002) with a jumper.

CONNECTOR J1					
PIN	FUNCTION	PIN	FUNCTION		
Α	BIT 1	U	STROBE		
в	BIT 2	V	BIT 18 <sup>1</sup>		
С	BIT 3	W	+5V		
D	BIT 4	X	+15V		
E	BIT 5	Y	-15V		
F	BIT 6	Z	DIGITAL GND		
н	BIT 7	1-4	NC		
J	BIT 8	5	INTERLOCK		
к	BIT 9	6	INTERLOCK		
L	BIT 10	7-16	NC		
м	BIT 11	17	BIT 171		
N_	BIT 12	18			
P	BIT 13	19			
R	BIT 14	20			
S	BIT 15	21			
T	BIT 16	22			

	CONNECTOR J2
PIN	FUNCTION
1	ANALOG SENSE LOW
2	ANALOG SOURCE LOW
3	NC
4	ANALOG SOURCE HIGH
5	ANALOG SENSE HIGH
6	ANALOG REF. IN/OUT
A	ANALOG REF. IN/OUT
В	ANALOG SENSE HIGH
С	ANALOG SOURCE HIGH
D	NC
E	ANALOG SOURCE LOW
F	ANALOG SENSE LOW

J2 MATES WITH CINCH P.N. 251-06-30-160 (SUPPLIED).

J1 MATES WITH CINCH P.N. 251-22-30-160 (SUPPLIED).

Mounting Card Connector Designations

### **DEGLITCHER IV**

The Deglitcher IV is a precision high-speed, high-isolation sample-and-hold circuit which eliminates the glitches that occur whenever a DAC is dithered through a major carry. Such momentary transients can be of concern in applications such as high-resolution CRT beam positioning, where glitch-free code transitions are often required for optimum display quality and legibility. Oscilloscope photographs in Figures 7a and 7b below show the output of a DAC1136 being dithered up and down through the major carry, between codes 1000000000000000 and 0111111111111111. In Figure 7b, the Deglitcher IV is turned on virtually elminating the glitches and allowing the  $152\mu$ V LSB step to be clearly seen.



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Figure 7a. DAC1136; Major-Carry Dither without Deglitcher IV (BW = 1MHz), Vertical Scale 0.2V/Division



Figure 7b. Same Major-Carry Dither with Deglitcher IV (BW = 1MHz), Vertical Scale, 200µV/Division

The Deglitcher IV utilizes a proprietary sampling technique which isolates the output amplifier during the critical  $10\mu s$ period immediately following a code change. The only discernible difference in DAC performance when used with Deglitcher IV is a delay of approximately  $11\mu s$  after the strobe goes HI before the (deglitched) DAC output voltage starts slewing toward the new value.

### **GLITCH ADJUSTMENT**

There are two "Glitch" adjustment potentiometers, accessible on the Card-Mounted Assembly. The adjustment on the card permits nulling of any Track-to-Hold offset, whereas the adjustment internal to the Deglitcher IV allows for precise nulling of the Hold-to-Track transient. Because of the nearinfinite attenuation of the actual DAC current glitches, no current-glitch transient is visible on the output. For this reason, it is easiest to null the 2 Deglitcher adjustments while strobing the Card with a static digital input.

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### INPUT OPTIONS

The Card-Mounted Assembly contains input registers. The input code ordered by the user is set at the factory by means of various jumpers in the logic circuitry. See ordering guide for details.

Since the Card-Mounted Assembly contains input registers, the card requires a strobe pulse circuit. Strobe characteristics of input registers are:

- 2. The digital input code can be changed at any time up to and including that instant when the strobe command goes HI.
- 3. The actual transfer of the input code to the DAC will occur  $\approx 3\mu s$  after the strobe command; during this  $3\mu s$  the digital input code to the card assembly should not be changed, in order to prevent the possible coupling of logic noise into the DAC output. At  $t_0 + 3\mu s$ , the deglitcher is automatically enabled for the following  $\approx 8\mu s$ . Thus there will be a delay of  $\approx 11\mu s$  before the deglitched output starts slewing to the new value. Actual data transfer to the DAC automatically occurs at  $t_0 + 3.1\mu s$ .

### **OUTPUT OPTIONS**

The Card-Mounted Assembly for the DAC1136/1138 allows for several user-selectable output configurations:

- 1. Internal Output Amplifier inside the DAC Module.
- Analog Devices model 234L; for low noise, low drift applications (2μV, ±0.1μV/°C).

- Analog Devices model 44K; available only with DAC1136; recommended only for high speed or high current applications.
- 4. Deglitcher IV with self-contained precision BI-FET output amplifier (AD542K).
- 5. Deglitcher IV with model 234L output amplifier.
- 6. Deglitcher IV with model 44K output amplifier (recommended with DAC1136 only).

When using an external amplifier, a four terminal output connection can be utilized on the Card-Mounted Assembly in order to allow for compensation of connector contact resistance.



- 1. VOLTAGE DROP BETWEEN SOURCE LO AND SENSE LO MUST OBSERVE CURRENT MODE COMPLIANCE LIMITS FOR RATED ACCURACY.
- THIS CONNECTION SCHEME CANNOT BE USED WITH INTERNAL AMPLIFIER OF THE DAC OR WITH THE AMPLIFIER INTERNAL TO THE DEGLITCHER IV.

### Figure 8. Four-Terminal Output Connections

#### **ORDERING GUIDE**

### WHEN ORDERING THE DAC1136 OR DAC1138, ORDER EITHER:

1. Module only:

DAC1136J DAC1136K DAC1136L DAC1138J DAC1138K

2. DAC1136/1138 as a Card-Mounted Assembly:



DAC1136L, DAC1138 AND DAC1138K.

# 

# Low Cost/High Accuracy 18-Bit D/A Converter

### FEATURES

Integral Nonlinearity:  $\pm 0.00076\%$  FSR max Differential Nonlinearity:  $\pm 0.00076\%$  FSR max Low Differential Nonlinearity T.C.:  $\pm 1ppm/^{\circ}C$  max Wide Power Supply Operation:  $\pm 11.5V$  to  $\pm 16V$ Fast Settling:  $6\mu$ s to  $\pm 0.00076\%$  FSR Small Size 2"  $\times 2" \times 0.4"$ 

### APPLICATIONS

Automatic Test Equipment Digital Audio Sonar Robotics Nuclear Instrumentation

### **GENERAL DESCRIPTION**

The DAC1146 is a low cost, 18-bit resolution (1 part in 262,144), digital-to-analog converter that provides high accuracy, high stability and is contained in a  $2'' \times 2'' \times 0.4''$  module.

Integral and differential nonlinearity are both guaranteed at  $\pm 0.00076\%$  FSR maximum. Additional guaranteed performance features include: differential nonlinearity T.C.  $\pm 1ppm/^{\circ}C$  maximum, offset T.C.  $\pm 30\mu V/^{\circ}C$  maximum, gain T.C.  $\pm 12ppm/^{\circ}C$  maximum, bipolar offset T.C.  $\pm 7ppm/^{\circ}C$  maximum.

The DAC1146 makes use of CMOS integrated circuits, thin-film resistor technology and proprietary CMOS current-steering switches to obtain high resolution, high reliability and small size. The calculated MTBF for the DAC1146 is 275,445 hours, per Mil Handbook 217C.

The DAC1146 can operate with power supplies ranging from  $\pm 11.5$ V to  $\pm 16.0$ V. An internal precision reference is provided, an external reference can be used. The external reference voltage input range is -12V to +12V. The analog output ranges include: +5V, +10V,  $\pm 5$ V,  $\pm 10$ V, -2mA and  $\pm 1$ mA, and are selectable via pin programming (see Figure 1). Digital input coding for unipolar operation is true binary, bipolar input coding is offset binary or 2's complement.

# DAC1146





Figure 1. DAC1146 Functional Block Diagram

# **SPECIFICATIONS** (typical @+25°C, $V_s = \pm 15V$ , $V_{REF} = +10V$ unless otherwise specified)

MODEL	DAC1146	<b>OUTLINE DIMENSIONS</b>
RESOLUTION	18 Bits	Dimensions shown in inches and (mm).
ACCURACY		
Integral Nonlinearity	$\pm 0.00076\%$ FSR <sup>1</sup> (max)	2.01 (51.1) MAX
Differential Nonlinearity	$\pm 0.00076\%$ FSR <sup>1</sup> (max)	
Monotonic (16 Bits)	Guaranteed	0.41
Offset <sup>2</sup>	Adjustable to Zero	
Gain <sup>2</sup>	Adjustable to Full Scale	
STABILITY		
Differential Nonlinearity	$\pm 1$ ppm/°C (max)	0.2 (5.0) MIN
Offset	$\pm 30\mu V/^{\circ}C(max)$	
Bipolar Offset	$\pm 7 \text{ppm/}^{\circ} C(\text{max})$	▶ <b>♦</b> 16 <del>                                     </del>
Gain	$\pm 12$ ppm/°C (max)	
STABILITY Long Term	······································	<b>↓</b> · · · · · · · · · · · · · · · · · · ·
(ppm/1000 hr)		
Differential Nonlinearity	+ lnpm	
Offset	- 199 + 3nnm	
Bipolar Offset	+ 3ppm	
Gain	± 12ppm	ŀ <b>∳┼┼┼┼┼┼┼┼┼┼┼┼┼┼</b> ╋┨
	~ 12ppin	
REFERENCE VOL TAGE (V <sub>REF</sub> )		<b>│<u>╋</u>┼┼┼┼┼┼┼┼┼┼┼┼┼┼┿┥┤ │</b>
Output voltage	$+10.00V \pm 0.3\%$ (max)	▲ 1 + + + + + + + + + + 32 ◆
Output Current	2mA (max)	┠╇┿┾┼┼┼┼┼┼┼┼┼┼┼┼┼┼┥┥
Ext. Rei Voltage Range	-12V to $+12V$	BOTTOMVIEW
Input Resistance	12k1	- 0.1 (2.5) GRID
DYNAMIC PERFORMANCE <sup>4</sup>		TERMINAL PINS INSTALLED ONLY
Settling Time to $\pm 0.00076\%$	. · · · · · · · · · · · · · · · · · · ·	IN SHADED HOLE LOCATIONS
Voltage, Full Scale Step	• • •	MATING CONNECTORS
Unipolar (10V)	бµѕ	MATING CONNECTORS
Bipolar ( $\pm 10V$ )	12µs	AUI584-3 (2 REQUIRED)
Voltage, LSB Step	3µs	
Current	2µs	PIN DESIGNATIONS
DIGITAL INPUTS	CMOS, TTL Compatible	
Codes	•	PIN FUNCTION PIN FUNCTION
Unipolar	Binary (BIN)	1 MSB 32 +15V
Bipolar	Offset Binary (OBIN), Two's Complement	2 MSB   31 - 15V 3 BIT 2   30 ANALOG GROUND
ANALOGOUTPUT		4 BIT3 29 AMPIN
Voltage	$+5V_{2} + 10V_{2} + 5V_{2} + 10V_{3}$	5 BIT4 28 CURRENTOUT
Current	$-2mA_{2} + 1mA_{3}$	6 BILS 27 N.C. 7 BILG 26 REFERENCE OUT
Voltage Compliance	+ 500 mV	8 BIT 7 25 REFERENCE IN
Noise (100kHz B.W.)	30µ.V rms	9 BIT8 24 10k
POWER REQUIREMENTS		10 BIT 9 23 10K 11 BIT 10 22 5k
Voltage (Pated Parformance)	+15V(+50/)	12 BIT 11 21 AMPOUT
Voltage (Operating)	$\pm 15 V (\pm 5\%)$ $\pm 11 5 V to \pm 16 0 V$	13 BIT 12 20 OFFSET
Supply Current Drain	$\pm 11.5 \vee 10 \pm 10.0 \vee$	14 BH 13   19 BH 18(LSB) 15 BH 14   18 BH 17
+ 15V	15mA 25mA	16 BIT 15 17 BIT 16
$\pm 15V$ Total Power (i) V <sub>2</sub> = $\pm 15V$	$+1500$ $\times$	
POWER SUPPLY SENSITIVITY	0.0010/ /0/ - 17	
Offset	$0.001\%/\% \pm V_{\rm S}$	· · · · · · · · · · · · · · · · · · ·
Gain	$0.001\% \pm V_{S}$	
TEMPERATURE RANGE		
Rated Performance	$0 \text{ to } + 70^{\circ}\text{C}$	
Operating	$-25^{\circ}$ C to $+85^{\circ}$ C	
Relative Humidity	Meets MIL STD 202E, Method 103B	
SIZE	$2'' \times 2'' \times 0.4''$	
	$(50.8 \times 50.8 \times 10.16 \text{mm})$	
Weight	33g	
NOTES		

<sup>17</sup>SR means Full Scale Range.
 <sup>2</sup>Offset and gain are adjustable to zero by means of external potentiometers. See Figure 2 for proper connections.
 <sup>3</sup>Rated performance is specified with + 10.0V reference.

<sup>4</sup>See Figure 5 for settling time curves.

Recommended Power Supply: Analog Devices Model 904. Specifications subject to change without notice.

### ANALOG OUTPUT RANGE

In the unipolar mode the DAC1146 provides an output current of -2mA. In the bipolar mode the DAC output current is offset by 1mA, (by connecting pin 25 to pin 24) for an output of  $\pm 1mA$ .

The DAC can be pin programmed for +5V, +10V,  $\pm 5V$  and  $\pm 10V$  by converting the DAC's current output to a voltage. To program the DAC for voltage output ranges (see Figure 1, Figure 2 and Table I).

Output
--------

Voltage Range	Input Code <sup>1</sup>	Connect Pin <sup>2</sup> 25 to Pin	Connect Pin 28 to Pin	Connect Pin 21 to Pin(s)
+ 5V	BIN		29	22, 23, 24
+ 10V	BIN	-	29	23,24
±5V	OBIN, 2's Comp	24	29	22
$\pm 10V$	OBIN, 2's Comp	24	29	23
	· · ·			

<sup>1</sup>For BIN or OBIN codes connect MSB to ground. For 2's comp code connect MSB to + 5V system power.

<sup>2</sup>Connect Pin 25 through a 50Ω potentiometer to either internal reference (Pin 26) or an external reference.

Table I. Analog Output Range Pin Programming

### OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 2. Proper offset and gain calibration requires great care and the use of extremely sensitive and accurate measurement instruments. These instruments should be capable of measuring to within  $1\mu$ V of the adjusted output voltage at both ends of the range. The potentiometers selected should be good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

For unipolar mode, apply a digital input code of all "0's" and adjust the offset potentiometer until a 0.00000V output is obtained (see Table II). Once the appropriate offset adjustment has been made, apply a digital input code of all "1's", and adjust the gain potentiometer until the plus full scale output is obtained (see Table II).

For bipolar mode, apply a digital input code of 100...00 and adjust the offset potentiometer until a 0.00000V output is obtained (see Table II). Once the appropriate offset adjustment has been made, apply a digital input of all "1's", and adjust the gain potentiometer until the proper plus full scale output is obtained.



Figure 2. Offset & Gain Calibration

	Code 000 00	Code 111 11
Unipolar		
+5V	0.00000V	+4.999981V
. + 10V	0.00000V	+9.999962V
	Code 100 00	Code 111 11
Bipolar		
± 5V	0.00000V	+4.999962V
$\pm 10V$	0.00000V	+9.999924V

Table II. Full Scale Calibrated Output Voltages

### PRECISION LOW DRIFT VOLTAGE OUTPUT

The internal output amplifier of the DAC1146 is optimized for high speed applications like digital audio and sonar, that require fast settling time. An external precision operational amplifier like the AD OP-07 can be applied when low offset drift is important. Simply connect the current output (Pin 28) to the inverting input of the amplifier. This connection should be made as close as possible to the DAC. Connect the proper feedback resistors as shown in last two columns of Table I. To avoid decreasing the gain drift performance of the DAC always use the internal feedback resistors, since they are matched to the internal current weighting resistors of the DAC (see Figure 3).

The current drift of the DAC1146 is typically  $350pA/^{\circ}C$  from + 15°C to + 35°C. When using the AD OP-07, the total drift of the output signal will be less than  $2\mu V/^{\circ}C$ .



Figure 3. Low Drift Voltage Output (+ 10V) Application

### DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1146 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Before attempting recalibration, it is imperative that the circuit be checked to confirm that all precautions have been taken to insure proper application. The DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusted if necessary, for a one LSB positive difference. The top four bits can be trimmed using the procedure outlined on next page. A differential voltmeter capable of  $100\mu V$  full scale should be connected to amp out of the DAC. A Fluke 895A or equivalent is recommended (see Figure 4).



Figure 4. Optional Differential Linearity Adjustment Circuit DIGITAL-TO-ANALOG CONVERTERS VOL. II, 10–37

- 1. Start with Bit 4, proceed to Bits 3, 2 and 1 by repeating steps 2 through 5. Set Bits 17 and 18 to "0" for this entire rocedure.
- 2. Set all digital inputs less significant than the bit being adjusted to "1"; set all others to "0".
- 3. Read the output voltage by nulling the voltmeter.
- 4. Set the digital input for the bit being adjusted to "1", set all others to "0".
- 5. Read the output voltage by nulling the voltmeter. This reading should be equal to that of Step 3 plus  $153\mu V$  (10V FSR). If not, adjust the bit.

6. Retrim gain.

### DIGITAL AUDIO APPLICATION

When using a DAC to reconstruct an audio signal, emphasis is placed on important audio parameters. These parameters include: Total Harmonic Distortion, Dynamic Range and Settling Time.

**Settling Time:** Settling time is the total time for the output to settle within an error band around its final value after a change in the input. Settling times for the DAC1146 are specified to  $\pm 0.00076\%$  of full-scale for any step change (see Figure 5).



Figure 5. Voltage Settling Time vs Accuracy

**Dynamic Range:** The DAC1146 has a typical dynamic range of 96dB for a 16-bit input and 100dB for an 18-bit input. The theoretical dynamic range can be expressed as 6dB X N, where N is the number of bits. The theoretical limit would indicate a dynamic range of 108dB for an 18-bit input, however linearity, noise and other errors limit the useful dynamic range to 100dB at 18 bits.

Total Harmonic Distortion: When the DAC1146 is used at 16 bits of resolution with a deglitcher as shown in Figure 6, the Total Harmonic Distortion (THD) for a full scale signal over the entire audio range 20Hz to 20kHz is typically less than 0.002% or -94dB.

Total Harmonic Distortion is defined as the ratio of the square root of the sum of the squares of the rms harmonic value to the rms fundamental values and is expressed in percent dB.

The THD can be calculated from the following formula and verified by testing (see Figure 6).

THD = 
$$\frac{\text{RMS Error}}{\text{RMS Signal}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} \left[E_L(i) + E_Q(i)\right]^2}}{\text{RMS Signal}} \times 100\%$$

where N is the number of samples.

 $E_L(i)$  is the linearity error of the DAC at each sample point.  $E_O(i)$  is the quantization error of the DAC at each

sample point.

### THD TESTING

When testing for THD the test equipment used must be distortion free so as not to mask the true performance of the device under test. The test circuit (see Figure 6) will produce a negligible amount of distortion when generating a test signal.

The PROM contains one cycle of a computer generated sine wave. Frequency select switches program the adder with the number of codes that it should skip on each count. This selection allows any of 2048 discrete frequencies between 12Hz and 25kHz to be generated with a constant 50kHz update rate. The DAC output is deglitched, and displayed on the spectrum analyzer. Total Harmonic Distortion can be computed by comparing the amplitude of the fundamental frequency with the amplitudes of the harmonics.

### TYPICAL THD TEST RESULTS

Dynamic Range	16-Bit Resolution	18-Bit Resolution
Dynamic Range	96dB	100dB
THD at FS	0.002% (-94dB)	0.0015%(-96dB)
THD at -15dB	0.01%(-80dB)	0.0075% (-82dB)
THD at - 20dB	0.02% (-74dB)	0.015%(-76dB)
THD at - 30dB	0.06%(-64dB)	0.045%(-67dB)



Figure 6. Block Diagram Harmonic Distortion Test Circuit

# 

# Ultra High Speed Deglitched D/A Converter MDD SERIES

### FEATURES

Ultra-High Speed: 20MHz Word Rate 8- and 10-Bit Versions Available TTL Compatible Smallest Size Available:  $3'' \times 4'' \times 0.5''$ Completely Self-Contained with Input Register, D/A, Deglitcher, Timing, Internal References, and Output Buffering

### APPLICATIONS

Color-Television Video Reconstruction, Time-Base Correction and Frame Synchronization Graphic Displays Deflection Systems Character Generators High Speed D/A Systems

### **GENERAL DESCRIPTION**

The MDD Series is a subsystem module which contains an input digital register, ultra-high speed current output D/A converter, deglitcher, output buffer amplifier, precision references, and timing circuitry within a  $3'' \times 4'' \times 0.5''$  case. The output of the device is an ultra-linear analog representation of the digital input. Requiring only external gain and offset potentiometers for final calibration, the MDD D/A solves the glitch problem associated with high-speed D/A converters. The incorporation of an internal register virtually eliminates the need for input bit time deskewing. While not totally eliminating the glitch per se, the remnant glitch is very small, and more importantly, constant (and therefore filterable) over the output range.

The MDD Series is available with 8- or 10-bit resolution and in two versions. The basic versions contain a unity gain output buffer and can deliver 2V p-p open circuit (or 1V p-p into a load) when the MDD output is both source and load terminated. The "A" versions contain a very high speed output gain amplifier to allow the MDD to deliver 4V p-p open circuit (or 2V p-p into a load) when the device is source and load terminated. Higher output voltages may be obtained—up to  $\pm 10V$  by external feedback resistor selection. However, settling time degradation must be expected.

### **TV APPLICATION**

The "A" version of the MDD Series deglitched D/A is ideally suited for color television video reconstruction. Its output can directly drive the low impedances normally associated with video baseband transmission. Since the output impedance of



the internal operational amplifier is less than  $1\Omega$ , the transmission-line match obtained with the internal source terminating resistor is almost perfect. Other applications include waveform generation, automatic test equipment, and fast process control systems.

Designed primarily for PC board mounting, these D/A's may also be plugged into pin sockets. The pins are 0.04'' diameter, gold plated, and are on 0.2'' centers. For increased reliability, each module is burned in for 96 hours at  $+25^{\circ}C$  before final test and shipment.



MDD Series Block Diagram

# **SPECIFICATIONS** (typical at +25°C and nominal supply voltages unless otherwise noted)

MODEL	MDD-0820 MDD-0820A	MDD-1020 MDD-1020A	
RESOLUTION	8 Bits	10 Bits	
Accuracy (including linearity) at			
Maximum Word Rate of 20MHz	±0.2%	±0.05%	
Monotonicity	Guaranteed 0 to +7	0°C	
DIGITAL DATA BIT INPUTS			
Logic Level/Load	1 Standard "S" TT	L Load	
Positive Logic-Binary (BIN)	"1" = +2.4V to +5V	/	
	"0" = 0V to +0.4V	·	
DIGITAL STROBE INPUT			
Logic Level/Load	2 Standard "S" TT	L Loads	
Positive Logic	"1" = $+2.4V$ to $+5V$	V	
	"0" = $0V$ to +0.4V		
Risetime and Falltime	10ns max		
Width	15ns min		
Timing	Negative-Going Trailing Edge to Occur a Minimum of 20ns After Last Data Bit Change		
Frequency	20MHz max		
	MDD-0820	MDD-0820A	
001101	MDD-1020	MDD-1020A	
Voltage No Load Uninolar	0 to +2V	Externally Programmable with	
totage, no Load, empoial	0.0.121	Gain and Offset Resistors	
Binolar	$\pm 1$ V to $\pm 1$ V	to ±10V max	
Impedance		to 1107 max	
Pin 23. Low Z	10Ω max	1Ω max	
$Pin 22, 50\Omega$	50Ω ±5%	$50\Omega \pm 1\%$	
$Pin 21, 75\Omega$	75Ω ±5%	$75\Omega \pm 1\%$	
Pin 20, 93Ω	93Ω ±5%	93Ω ±1%	
		1000	
Amplifier Current	$\pm 50$ mA for dc load = $100$ V min,		
DAC Current	dc load = 2.00T + T	LOAD	
	+15mA		
SETTLING TIME			
DAC Current Output (to 0.1%)	15ns	100	
Voltage Output	50ns to 0.1%	120ns to 0.1%	
	2V p-p	4v p-p	
RESIDUAL GLITCH <sup>1</sup>	30mV for 2V p-p F	.S. Output	
	or 1.5% of F.S.		
PEDESTAL	10mV for 2V p-p F	S. Output	
	or 0.5% of F.S.		
OUTPUT ZERO OFFSET	Adjustable to Zero		
OUTDUT ZEDO OFFCEM MENT	100 100		
OUTPUT ZERO OFFSET VS. TEMP	Toobbu/ C		
GAIN	Adjustable		
REFERENCES AVAILABLE	±6.2V		
POWER REQUIREMENTS			
+15V ±3%	120mA		
-15V ±3%	150mA		
+5V ±5%	250mA		
Power Supply Rejection Ratio	0.1%/V		
CASE	Dialfail Dhah-1 (-	MIT M 14	
LASE	Dialiyi Phthalate (p	CEMIL-M-14	
	(ypc 3DG-F)		
TEMPERATURE RANGE			
Operating	0 to +70°C		
Storage	->> C to +85 C	·	

### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



### **PIN DESIGNATIONS**

PIN	FUNCTION	PIN	FUNCTION
1	GROUND*	15	-REF OUT
2	BIT 1 INPUT (MSB)	16	+REF OUT
3	BIT 2 INPUT	17	GROUND*
4	BIT 3 INPUT	18	DEGLITCHER INPUT
5	BIT 4 INPUT	19	D/A OUTPUT
6	BIT 5 INPUT	20	93Ω OUTPUT
7	BIT 6 INPUT	21	75Ω OUTPUT
8	BIT 7 INPUT	22	500 OUTPUT
9	BIT 8 INPUT	23	LO Z OUTPUT
10	NC	24	AMP FEEDBACK
11	BIT 9 INPUT	25	GROUND*
12	BIT 10 INPUT (LSB)	26	-15V POWER INPUT
13	STROBE INPUT	27	+15V POWER INPUT
14	GROUND*	28	+5V POWER INPUT

LL GROUNDS INTERNALLY CORRECTED

NOTES 'Occurs at the update rate.

Specifications subject to change without notice.

### NOTES ON "DEGLITCHING"

An MDD Series D/A converter operating with a full-scale p-p analog output of 1V will typically have a glitch, or transient, in its output which is 15mV in amplitude and is 25ns wide, at the 50% points. These typical values are independent of whether the D/A converter is an 8-bit unit or a 10-bit unit.

This glitch remains constant, regardless of the transition points. In other words, it is the same for the transition from 0000000001 to 1000000000 as it is for the transition from 1000000000 to 1000000001 or any other two input words.

A constant glitch is the purpose of the deglitcher circuits. They are intended to hold the area under the curve at a constant value; they are not intended to get rid of all glitches per se.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line; i.e., a singleline spectrum at the sample rate frequency, and harmonics of the sample frequency.

If the glitch is a function of signal dynamics, as it is in the case of a D/A converter output which is not deglitched, a multitude of intermodulation products are formed. Some of



Figure 1. Pedestal/Glitch Relationship







Figure 3. D/A Current Equivalent Circuit

these IM products appear in the video pass-band as spurious signals and increased noise level. The deglitcher circuits effectively eliminate these products. When they do, the S/N ratio approaches that of an ideally-quantized signal, where the rms noise is  $Q/\sqrt{12}$ , when frequencies above Nyquist are filtered out.

In summary then:

- The residual glitch for an MDD Series D/A converter is typically 15mV for a full-scale 1V p-p output; this is 1.5% of F.S.
- The glitch width is typically 25ns at the 50% points.
- The amplitude and width of the glitch are constant, and independent of:
  - -the magnitude of change in successive transitions
  - -number of bits of digital output
  - -input (update) data rates

D/A converters without deglitching circuits have smaller, shorter glitches, on the average; but this type of converter has larger glitches at the major crossings, especially at the midscale transition.

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Figure 4. Spectrum of 10-bit D/A Operating at 11MHz Update Rate Without Deglitching — Unfiltered



Figure 5. Spectrum of 10-bit D/A Operating at 11MHz Update Rate With Deglitching — Unfiltered



Figure 6. Unipolar Output Configuration Basic Versions



Figure 7. Bipolar Output Configuration Basic Versions



NO LESS 1. SELECT RGAIN TO GIVE DESIRED OPEN CIRCUIT OUTPUT VOLTAGE. THE INPUT VOLTAGE TO THE OP AMP IS APPROXIMATELY O TO +2V. THE OUTPUT OF THE OF AMP IS THEREFORE (IZ × RGAIN/5002) VOLTS p.p.

- . THE LOGIC IS INVERTED INTERNALLY FOR THE "A" VERSIONS SUCH THAT ALL "1'S" AT THE DIGITAL INPUTS YIELDS A FULL-SCALE POSITIVE VOLTAGE AT THE OP AMP OUTPUT.
- FOR POSITIVE UNIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY  $800\Omega,$  MAKING A 2000Ω POTENTIOMETER IDEAL



Figure 9. Typical A/D-D/A Back-to-Back Connections for Video Applications or Testing

The typical video differential phase and gain errors (disregarding quantization effects) for the configuration shown are 3° and 3%, respectively, using an encode command frequency of three times the NTSC color subcarrier (10.74MHz). For applications requiring digitization at frequencies of four times NTSC (14.32MHz) or three times PAL (13.29MHz) the MATV-0816 A/D Converter should be substituted. For applications requiring digitization at four times PAL (17.74MHz), the MATV-0820 A/D Converter should be substituted. Results are applicable for either NTSC or PAL test signals using the 20 IRE modulated ramp.

Due to the inherently stable characteristics of the output operational amplifier, the "A" versions are recommended for driving properly terminated video terminated lines.

### ORDERING INFORMATION

For 8-Bit Models,	MDD-0820 without output amplifier
Order:	MDD-0820A with output amplifier
For 10-Bit Models,	MDD-1020 without output amplifier
Order:	MDD-1020A with output amplifier

Mating pin socket connectors for the MDD Series is model MSB-2. Prototyping socket is MSD-1.

The MDD Series D/A's are normally burned-in at +25°C for a minimum of 96 hours. For extended burn-in, consult the factory. All of Analog Devices' data acquisition products are covered by a one-year warranty.

Figure 8. Output Configuration - "A" Versions

# 

# Ultra High Speed Multiplying D/A Converter MDMS SERIES

### FEATURES

Small Size:  $2'' \times 2'' \times 0.4''$ High Multiplying Accuracy: Maintains Monotonicity and Linearity for any Analog Input within the Specified Range High Current Output: 10mA Full Scale High Reliability, Hybrid Microcircuit Construction Guaranteed Operation:  $-30^{\circ}$ C to  $+85^{\circ}$ C

### APPLICATIONS CRT Displays Waveform Generation Vector Generation Fast Digital Attenuator



### **GENERAL DESCRIPTION**

The MDMS series is an ultra-high speed, one or two-quadrant, multiplying D/A converter capable of 10MHz operation and 11-bit precision. The settling time for both analog and digital inputs is 100ns, and the large signal bandwidth of the analog input is in excess of 10MHz. The module is designed for the needs of the graphic display field and other applications requiring high-accuracy, high-speed multiplying operation.

The current output of the MDMS series D/A is precisely proportional to the analog input signal multiplied by the digital input code. The analog input signal may be any voltage between 0V and -10V, and can be a sine wave, triangle wave, sawtooth, or other waveform. The D/A output is an accurate scaled version of the input waveform, the scale factor being the digital input code. Alternatively, the analog input voltage may be used to scale a digitally generated signal. Various offsetting provisions are made so that the analog signal, digital signal, and output may be made bipolar or unipolar in order to accommodate various uses requiring one or two-quadrant operation.

The output impedance of the D/A is 200 ohms so that a twovolt output swing is possible with no load. Loading the output with 200 ohms results in a 1 volt p-p output. If an external operational amplifier such as the Analog Devices' HOS-050, HOS-050A, or HOS-060 op amp is connected to the output of the D/A, output voltages up to 20V p-p are obtainable at a small sacrifice in speed.

### **ORDERING INFORMATION**

Order Model Number MDMS-0801, MDMS-1001, or MDMS-1101. Ruggedized versions with extended burn-in are also available. Consult the factory.



MDMS Series - Block Diagram

# SPECIFICATIONS (typical @ +25°C and nominal power supply voltages unless otherwise noted)

MODEL	MDMS-0801	MDMS-1001	MDMS-1101
RESOLUTION	8 Bits	10 Bits	11 Bits
LSB Weight	40µA	10µA	5μΑ
ACCURACY (ADJUSTABLE TO)	±0.2%	±0.05%	±0.025%
Monotonicity	Guaranteed	•	•
Linearity	20µA, ±1/2LSB	5µA, ±1/2LSB	2.5µA, ±1/2LSB
ANALOG INPUT			
Voltage Range	0 to ~10V	•	•
Impedance	4kΩ ±2%	.•	•
Transfer Function (inverting)	0V input scales -10V input scale	D/A output to minimum outp es D/A output to maximum ou	ut; utput.
DIGITAL INPUT (TTL)			
Positive Logic, "1" =	+2.4V to +5.0V		
	0V to 0.4V	•	
Loading, 2 Std. IIL Loads	-5m A	•	•
0 =	-5mA	•	•
	JOHN		·
CODING (PARALLEL INPUT DATA)	DIM	•	•
Unipolar	BIN	•	•
All "1'-" Incut	UDIN	Arrighter Positive Output	
All "O's" Input		Animum Negative Output	
OUTPUT (CURRENT)	0	•	•
Dinolog	+5mA	•	•
Compliance Valtage	±15V -2V	•	•
Compliance voltage	2000 +1%	•	•
Loading	20000, 21/0	200Ω for 0 to 1V p-p Out	
Loading	-	Ω for 0 to 2V p-p Out	
Zero Offset (max)	50nA	•	. •
DYNAMIC CHARACTERISTICS			
Settling Time (digital & analog)	90ns to 0.2% F.	S. 100ns to 0.1% F.S.	130ns to 0.05% F.S.
Bandwidth (analog in)	10MHz	•	•
TEMPERATURE COEFFICIENTS			
Linearity	2ppm/°C	•	•
Monotonicity	·· (	Guaranteed -30°C to +85°C	•
POWER REQUIREMENTS			······································
+15V ±10%	60m A	•	•
-15V ±10%	20m A	•	•
Power Supply Rejection Ratio	0.005%/V	•	•
TEMPERATURE RANGE			·······
Operating	-	-30°C to +85°C	
Storage	-	-55°C to +125°C	
BUYSICAL CHARACTERISTICS	····		
Case	1	Diallyl Phthalate per MIL-	
	1	N-14 Type SDG-F	

NOTES

\*Specifications same as MDMS-0801

Specifications subject to change without notice.



Figure 1. The MDMS-1101 Multiplying D/A Used as a Digital Waveform Generator with Digital Attenuator Control



OUTLINE DIMENSIONS Dimensions shown in inches and (mm).

PINS ARE GOLD PLATED PER MIL-G-5204 TYPE II

### **MATING SOCKET MSA-1**

### PIN DESIGNATIONS

PIN	FUNCTION
1	BIT 1 INPUT (MSB)
2	BIT 2 INPUT
3	BIT 3 INPUT
4	BIT 4 INPUT
5	BIT 5 INPUT
7	BIT 6 INPUT
8	BIT 7 INPUT
9	BIT 8 INPUT
10	BIT 9 INPUT
11	BIT 10 INPUT
12	BIT 11 INPUT LSB
19	ANALOG INPUT
21	OFFSET ADJ
23	-15V POWER INPUT
25	+15V POWER INPUT
28	GROUND
30_	BIPOLAR OFFSET
32	ANALOG OUTPUT



Figure 2. Operation of Multiplying D/A Circuit

# **Analog-to-Digital Converters**

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•New product since publication of 1982-1983 Databook Update.

# Selection Guide Analog-to-Digital Converters

## 8-Bit A/D Converters





### AD570

Complete A/D Converter with Reference and Clock Fast Successive Approximation Conversion –  $25\mu s$ No Missing Codes Over Temperature 0 to +70°C – AD570J -55°C to + 125°C – AD570S

Digital Multiplexing – 3 State Outputs 18-Pin Ceramic DIP

### AD670

Complete 8-Bit A/D Converter Fast Conversion Time: 10µs Full Microprocessor Bus Interface Flexible Input Stage: Instrumentation Amp Front End Provides Differential Inputs and Good Common-Mode Rejection No User Trims Required No Missing Codes Over Temperature Single +5V Supply Required Convenient Input Ranges Small 20-Pin Package Vol. I 10-85

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### AD673

Complete 8-Bit A/D Converter with Reference, Clock and Comparator **Full Microprocessor Bus Interface** Fast Successive Approximation Conversion - 20µs No Missing Codes Over Temperature

Operates on +5V and -12V to -15V Supplies



No Missed Codes Over Full Temperature Range Fast Conversion Time: 15µs Interfaces to µP like RAM, ROM or Slow Memory Low Power Dissipation: 30mW **Ratiometric Capability** Single +5V Supply

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# Selection Guide Analog-to-Digital Converters

# 8-Bit A/D Converters



### AD7581

8-Bit Resolution On-Chip 8 × 8 Dual-Port Memory No Missed Codes Over Full Temperature Range Interfaces Directly to Z80/8085/6800 CMOS, TTL Compatible Digital Inputs Three-State Data Drivers Ratiometric Capability Interleaved DMA Operation Fast Conversion A/D Process Totally Transparent to µP Page

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### HAS-0802

Conversion Times as Low as 1.2µs Resolution: 8 Bits Exceptional Accuracy: 0.012% of F.S. Low Power Contained in Glass or Metal 32-Pin DIP Adjustment-Free Operation Vol. I 10–201


## **10-Bit A/D Converters**



## AD579

Complete 10-Bit A/D Converter with Reference and Vol. I Clock Fast Successive Approximation Conversion: 1.8µs Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±40ppm/°C max Max Nonlinearity: < ± 0.048% Low Power: 775mW

### **HAS-1002**

Conversion Times as Low as 1.7µs **Resolution: 10 Bits** Exceptional Accuracy: 0.012% of F.S. Low Power **Contained in Glass or Metal 32-Pin DIP Adjustment-Free Operation** 

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## Selection Guide Analog-to-Digital Converters

## **10-Bit A/D Converters**



### AD571

Complete A/D Converter with Reference and Clock Fast Successive Approximation Conversion – 25µs No Missing Codes Over Temperature 0 to +70°C – AD571K -55°C to +125°C – AD571S Digital Multiplexing – 3 State Outputs 18-Pin Ceramic DIP Low Cost Monolithic Construction Page

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### AD573

Complete 10-Bit A/D Converter with Reference, Clock and Comparator Full 8- or 16-Bit Microprocessor Bus Interface Fast Successive Approximation Conversion – 15µs No Missing Codes Over Temperature Operates on +5V and - 12V to - 15V Supplies

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# AD575 Page Complete 10-Bit A/D Converter with Reference, Clock and Comparator Vol. I Serial Output 10-67 Fast Successive Approximation Conversion – 20µs No Missing Codes Over Temperature Operates on +5V and – 12V to – 15V Supplies Low Cost Monolithic Construction Internal/External Clock Option Triggered or Continuous Conversions Automatic Shunt Cycle Option Low Cost Monolithic Supplies

### AD7571

10-Bit Plus Sign Resolution
No Missed Codes Over Full Temperature Range
Conversion Time 80µs
Differential Analog Voltage Inputs, ±10V Range
Serial and Parallel Data Outputs
Easy Interface to Most Microprocessors
Internal Clock Oscillator
Single Supply Operation for Positive-Only Signals
Monolithic Construction

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## Selection Guide Analog-to-Digital Converters

## 12-Bit A/D Converters





## AD572

#### True 12-Bit Operation: Max Nonlinearity <±0.012% Low Gain T.C.: <±15ppm/°C (AD572B) Low Power: 900mW Fast Conversion Time: <25μs

Monotonic Feedback DAC Guarantees No Missing Codes

### AD574A

Complete 12-Bit A/D Converter with Reference and Clock

Full 8- or 16-Bit Microprocessor Bus Interface 250ns Bus Access Time

**Guaranteed Linearity Over Temperature** 

0 to +70°C - AD574AJ, AK, AL

-55°C to +125°C - AD574AS, AT, AU

No Missing Codes Over Temperature

Fast Successive Approximation Conversion – 25µs Buried Zener Reference for Long-Term Stability and Low Gain T.C.

Low Gain T.C.

10ppm/°C max AD574AL 12.5ppm/°C max AD574AU Low Profile 28-Pin Ceramic DIP

Low Power: 390mW

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### AD578

Complete 12-Bit A/D Converter with Reference and	Vol. I
Clock	10-73
Fast Conversion: 3µs (max)	
Buried Zener Reference for Long Term Stability and	
Low Gain T.C.: ±30ppm/°C max	
Max Nonlinearity: < ± 0.012%	
Low Power: 775mW	
Hermetic Package Available	
Positive-True Parallel or Serial Logic Outputs	
Short Cycle Capability	
Precision + 10V Reference for External Applications	
Adjustable Internal Clock	
"Z" Models for ±12V Supplies	

### AD5200 SERIES

AD5200: 50µs Conversion Time AD5210: 13µs Conversion Time

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True 12-Bit Operation: ±1/2LSB max Nonlinearity **Totally Adjustment-Free** 

**Guaranteed No Missing Codes Over the Specified Temperature Range** 

Hermetically-Sealed Package

Standard Temperature Range: -25°C to +85°C

Extended Temperature Range: -55°C to +125°C

Serial and Parallel Outputs

Monolithic DAC with Scaling Resistors for Stability Low Chip Count for High Reliability Industry Standard Pin Out Small 24-Pin DIP

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## Selection Guide Analog-to-Digital Converters

## 12-Bit A/D Converters





### AD5240

Complete 12-Bit A/D Converter with Reference and Clock Fast Successive Approximation Conversion: 5us

Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C

Max Nonlinearity: <±0.012%

Low Power: 775mW Typical

Hermetic Package Available

Low Chip Count – High Reliability

Pin Compatible with AD ADC84/AD ADC85

"Z" Models for ±12V Supplies

### AD ADC80

True 12-Bit Operation: Max Nonlinearity ±0.012%	Vol. I
Low Gain T.C.: ±30ppm/°C max	10-183
Low Power: 800mW	
Fast Conversion Time: 25µs	
Precision 6.3V Reference for External Application	
Short-Cycle Capability	
Serial or Parallel Data Outputs	
Monolithic DAC with Scaling Resistors for Stability	
Low Chip Count – High Reliability	
Industry Standard Pin Out	
"Z" Models for ±12V Supplies	

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## AD ADC84/AD ADC85

"Z" Models for ±12V Operation Available

Industry Standard Pin Out

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Complete 12-Bit A/D Converter with Reference and Clock Fast Successive Approximation Conversion: 10µs Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C Max Nonlinearity: <±0.012% Low Power: 880mW Typical Hermetic Package Available Low Chip Count – High Reliability

### HAS-1201

12-Bit Resolution 1MHz Word Rate T/H and Timing Circuits Included Single Hybrid Package

APPLICATIONS Radar Systems Medical Instrumentation Electro-Optics Systems Test Systems Vol. I 10–205

## Selection Guide Analog-to-Digital Converters

## High Resolution A/D Converters





### AD ADC71/AD ADC72

Complete 16-Bit Converter with Reference and Clock ±0.003% Maximum Nonlinearity

No Missing Codes to 14 Bits Fast Conversion – 45µs (14 Bit) Short Cycle Capability Parallel or Serial Logic Outputs Page

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### AD ADC816

10-Bit Resolution 800ns Conversion Time Six Input Ranges Unipolar and Bipolar Operation Vol. 1 10-199



### HAS-1409

14-Bit Resolution 125kHz Word Rates Internal Track-and-Hold 40-Pin DIP

APPLICATIONS FDM/TDM Transmultiplexers CAT/NMR Scanners PCM Systems Digital Audio

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### AD7552 ·

12-Bit Binary with Polarity and Overrange Accuracy ± 1LSB Microprocessor Compatible Ratiometric Operation Low Power Dissipation Vol. I 10–127

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## Selection Guide Analog-to-Digital Converters

## **High Resolution A/D Converters**







## ADC1130/ADC1131

14-Bit Resolution and Accuracy Fast 12µs Conversion Time (ADC1131J/K) Low 10ppm/°C Maximum Gain TC User Choice of Input Range No Missing Codes Page

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### ADC1140

Low Cost 16-Bit A/D Converter Guaranteed Nonlinearity:  $\pm 0.003\%$  FSR max 35µs Maximum Conversion Time Small Size 2" × 2.4" Wide Power Supply Operation:  $\pm 12V$  to  $\pm 17V$  Vol. II 11-31

### ADC1143

High Performance 16-Bit A/D Converter Low Power Consumption:  $175 \text{mW} \text{max}, V_{\text{S}} = \pm 15 \text{V}$ 150mW max,  $V_S = \pm 12V$ **Guaranteed Nonlinearity:** ±0.006% FSR max (ADC1143J) ±0.003% FSR max (ADC1143K) **Guaranteed Differential Nonlinearity:** ±0.006% FSR max (ADC1143J) ±0.003% FSR max (ADC1143K) Low Differential Nonlinearity T.C.: ±2ppm/°C max (ADC1143J) ± 1ppm/°C max (ADC1143K) **Fast Conversion Time:** 70µs max (ADC1143J) 100µs max (ADC1143K) Wide Power Supply Operation:  $V_{s} = \pm 11.4V$  to  $\pm 18.0V$  $V_{\rm D} = +3.0V$  to +18.0V

### Vol. II 11–35



Video A/D Converters

#### OVERFLOW 63 62 <u>та</u> мse 157 -113 BIT 2 PARATO LATCH OUTPUT -<u>(1</u>) вт з <u>,</u> Мит 4 (1) BIT 5 3 ற்க R3 1 R2 ANALO GROUN (TIE TO AD9000 0

### AD5010/AD6020

Scan Frequency to 100MHz (AD5010KD) Low 450mW Power Dissipation ±1/4LSB Linearity ECL Logic Compatible No Sample & Hold Required Overflow Output for Extended Resolution

APPLICATIONS Video Data Conversion High Speed Data Acquisition Radar/Sonar Data Conversion

### 9000 SERIES

6-Bit, 75MHz Minimum Word Rates No T/H Required -55°C to + 125°C Temperature Overflow Bit for Cascading Units

APPLICATIONS Image Processing Video Digitizing Radar Digitizing Military Systems Page

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## Selection Guide Analog-to-Digital Converters

## Video A/D Converters





### CAV-0920

9-Bit Resolution 20MHz Word Rate Single 35-In<sup>2</sup> PC Board ECL Compatible No External Circuits Required

APPLICATIONS Television Digitizing Radar Digitizing Medical Instrumentation Digital Communications Spectrum Analysis

### CAV-1040

10-Bit Resolution 40MHz Word Rate Single 35-In<sup>2</sup> PC Board ECL Compatible No External Circuits Required

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## CAV-1210

12-Bit Resolution 10MHz Word Rate Single 35-In<sup>2</sup> PC Board ECL Compatible No External Circuits Required

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## Selection Guide Analog-to-Digital Converters

## **Video A/D Converters**





### MATV-0811/MATV-0816

MATV-0811: 11MHz Word Rates MATV 0816: 16MHz Word Rates

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8-Bit Accuracy – Guaranteed Monotonic Most Economical Video A/D Smallest Available Complete A/D – 5.5"×4.38"×0.85" Self Contained – Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

#### APPLICATIONS

Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies

Video Time Base Correction and Frame Synchronization

Radar Signal Processing

Real Time Transient and Continuous Spectrum Analysis

### **MATV-0820**

8-Bit Accuracy – Guaranteed Monotonic Ultra-High Speed – dc to 20MHz Word Rates Most Economical Video A/D Smallest Available Complete A/D – 5.5"×4.38"×0.85"

Self Contained – Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

#### APPLICATIONS

Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies

Video Time Base Correction and Frame

Synchronization

**Radar Signal Processing** 

Real Time Transient and Continuous Spectrum Analysis

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### **MOD-1005**

10 Bits @ 5MHz Word Rate One-27 Sq. In. PC Board Built-In Track-and-Hold – 25ps Aperture Uncertainty 20MHz Analog Input Bandwidth TTL Compatible Low (10-Watt) Power Dissipation Signal-to-Noise Ratio Greater Than 58dB Noise Power Ratio Greater Than 49dB Completely Repairable

APPLICATIONS Radar Digitizing Digital Communications Real Time Spectrum Analysis High Resolution TV

### **MOD-1020**

10 Bits @ 20MHz Word Rates One-35 Sq. In. PC Board Built-In Track-and-Hold – 25ps Aperture 15MHz Large-Signal Input Bandwidth ECL Compatible Signal-to-Noise Ratio Greater Than 56dB Noise Power Ratio Greater Than 45dB

APPLICATIONS Television Digitizing Radar Digitizing Medical Instrumentation Digital Communications Spectrum Analysis Sonar Digitizing

### MOD-1205

12 Bits @ 5MHz Word Rate One-27 Sq. In. PC Board Built-In Track-and-Hold – 25ps Aperture Uncertainty 15MHz Analog Input Bandwidth TTL Compatible Low (13-Watt) Power Dissipation Signal-to-Noise Ratio Greater Than 66dB Noise Power Ratio Greater Than 56dB Completely Repariable

APPLICATIONS Radar Digitizing Digital Communications Real Time Spectrum Analysis Signature Analysis

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## **Orientation** Analog-to-Digital Converters

#### FACTORS IN CHOOSING AN A/D CONVERTER

In the two volumes of this catalog, there are listed some 34 different families of analog-to-digital converters (ADCs). If one were to consider all the variations, there would be considerably more than 92 different types to choose among (excluding digital panel meters and data-acquisition systems, which are catalogued elsewhere). The reason for so many different types is the number of degrees of freedom in selection—technological, functional, performance, and package. Complete information on converters may be found in the 250-page book, *Analog-Digital Conversion Notes*, published by Analog Devices and available for \$5.95 from P.O. Box 796, Norwood, MA 02062.

#### **TECHNOLOGICAL FACTORS**

The technologies represented here include modules (cards and potted circuits) and integrated circuits—monolithic and hybrid. Modules generally can provide the extremes of performance as well as arbitrary levels of functional completeness. For example, the 12-bit 5MHz MOD-1205 is built on a card that includes a track-hold amplifier.

The technical data in this volume embrace exceptionally high performance (high-resolution and high-speed) A/D converters, in the form of encapsulated modules and printed-circuit cards. As the Selection Guide indicates, there is also a universe of technical data, to be found in Volume I, on a wide range of monolithic and hybrid A/D converters, including many microprocessor-compatible types.

Besides the products in this section, analog-to-digital conversion functions in this Volume (at various levels of system integration) are also inherent in the sections devoted to Data-Acquisition Subsystems, Digital Panel Instruments, Microcomputer Interface Boards, Intelligent Measurement-and-Control Subsystems, and MACSYM. A/D conversion functions are also performed by products in the Voltage-to-Frequency and Synchro-Digital Conversion sections.

#### FUNCTIONAL CHARACTERISTICS

Block diagrams illustrating the various conversion techniques appear on individual data sheets.

The moderate-speed converters described in this volume (<1MHz) employ two fundamental techniques—successive approximations, for moderate-to-high resolution at moderate-to-high speed, and integration, for high resolution at modest speeds. The ADC1143 and ADC1140 are examples of the former, the converters used in DPMs, the latter.

Like a chemist's balance with binary weights (1/2, 1/4, 1/8, etc.), the successive-approximation converter compares the unknown input with sums of accurately-known binary fractions of full scale, starting with the largest  $(2^{-1})$ , and rejecting any that change the comparator's state ("tip the scale"). At the end of conversion (EOC), the output of the converter is a digital word, representing the ratio of the input to full scale by a fractional-binary code.

Integrating types count pulses for a period proportional to the input. Most-frequently used are *dual slope* types, which count off the period required for the integral of the reference to become equal to the average value of the input (over a fixed period). Integrating types can be made insensitive to drift by storing errors during an error-correcting cycle and subtracting them during the input-measuring cycle. This correction can be performed in analog fashion, using capacitance for storage, or digitally—using the information stored in a counter for correction (AD7550).

The video converters described here (MATV, MOD-1205, etc.) employ two basic encoding techniques: simultaneous, or *flash* conversion, and serial-Gray-code conversion. High resolution and high speed are obtained by *subranging*, i.e., by performing an n-bit conversion in two steps; Analog Devices has perfected a form of subranging, known as DCS-digitally corrected subranging-which permits accurate resolutions of 12 bits and more.\*

In flash conversion, the analog signal is compared against  $2^n - 1$  graded voltage levels, using as many comparators, and the comparator output logic levels are processed by a priority encoder, which converts the "thermometer" output to a binary (or Gray) code. Since the whole conversion occurs essentially simultaneously, it is the fastest means of conversion, but it requires many accurate comparators and large numbers of gates.

In serial-analog-parallel-digital conversion, there are a number of cascaded stages, each having a gain of +2 for signals less than one-half the reference, and a gain of -2 for signals between one-half the reference and full scale. At each stage, a decision is made as to whether the signal is larger (1) or smaller (0) than one-half the reference; the stage's analog output becomes the input to the next stage. The complete time for one conversion is determined by the propagation delay of the analog signal through all stages; however, since the decision of each stage can be latched as soon as the stage has settled (and a new conversion can, in principle, be started as soon as the first bit has been latched), the rate at which conversions come out of the pipeline is considerably faster than the time for one sample to go through the conversion process. Though fast, this process is difficult to implement accurately for more than a few bits, because of the compounding of gain (hence errors).

A subranging converter digitizes to a group of more-significant bits, and stores them in a latch. A fast, very-high-accuracy D/A converter converts them to an analog signal, which is then subtracted from the input. The difference, or residue, is amplified and digitized, and (in DCS) the result is combined digitally in such a way as to correct for mid-scale conversion errors.

Whatever the technique, these A/D converters comprise several essential functions: an analog section, a digital data-generating section, data outputs, and digital controls. Some video converters also include an on-board track-hold function.

\*A considerable amount of useful information about video conversion can be found in "Understanding High-Speed (Video) A/D Converter Specifications", available upon request.

#### Analog Section

This section requires a reference, one or more high-gain comparators, and either a D/A converter (successive approximations and subranging) or a controllable integrator. The reference may be internal or external, fixed or variable, and of a specified polarity/sense in relation to the analog input. In ratiometric conversion, the reference is usually external and variable.

In successive-approximation converters, the comparator is generally used in the current-summing mode; that is, the current output of the DAC is summed with the current developed in the DAC's "feedback resistor" by the input voltage (of opposite polarity), and the balancing action of the converter tends to bring the summing junction towards a voltage null (much like that of an op amp) at the end of conversion. The typical DAC feedback options, when applied in an ADC, provide input-scaling choices. When the bipolar-offset connection is jumpered to the summing point, input signals of both polarities can be handled. The current-switching action of the DAC, at the typically fast clock-rates used in successive-approximation converters, can disturb the output of the analog signal source, especially if it is a slow high-precision op amp. In such cases, buffering may be necessary; some of the modules, have on-board analog buffer-followers, and the card-mounted video converters have on-board track-hold-buffer amplifiers.

In integrating types, absolute-value and polarity-sensing circuitry may be required at the front end to handle both polarities of input. Outputs are usually sign-magnitude BCD.

#### **Digital Data-Generating Section**

In successive-approximation types, this section consists of a discrete or integrated successive-approximations register (SAR), its controls, and inputs from the comparator and clock (which is on-board, but in many cases permits external clock pulses, frequency adjustment, and/or control). In integrating types, this section consists of the clock-pulse generator, the counter(s), the input from the comparator, and the associated controls.

#### **Data Outputs**

Factors to consider here include coding, resolution, overrange information, levels, format, validity, and timing. Coding is usually binary, including jumper-connected offset-binary and/ or two's complement for bipolar input signals. For some types, BCD is available, with sign-magnitude for bipolar inputs. Output coding specs should always be checked for digital polarity (positive- or negative-true) of both magnitude and sign information. The resolution (number of output bits) must be sufficient for the application; in addition, the specifications must be checked to ascertain that not only will all 2<sup>n</sup> (binary) output codes be present (no missing codes), but they must all be present at any temperature in the operating range and related to the input with sufficient accuracy. Integrating types generally have no problems with missing codes (except sometimes at zero, with sign-magnitude coding); nevertheless, nonlinear integration can cause the conversion relationship to become nonlinear. Successive-approximation types have no

way of determining *overrange*; they simply fill up. However, counter types roll over and put out a carry flag to signal overrange.

The *data levels* available at the converter output must be checked (TTL, low-voltage CMOS, high-voltage CMOS, ECL), as must the load-driving capability and fanout, and the supply conditions under which appropriate output levels will be furnished. The available choice of output *formats* must also be as desired—parallel, serial, byte-serial, and/or pulse-train. If the converter is intended to communicate directly with a data bus, the output should have three-state capability, and parallel outputs must be enabled in bytes of appropriate widths. If the output is serial NRZ (non-return-to-zero), it should be accompanied by a set of synchronized clock-pulses.

A status (or busy or EOC or "data ready") output changes state to indicate when the data becomes valid. The exact nature of this transition should be specified—polarity, timing, levels, etc. For serial data, the exact relationship between the data and the synchronizing clock should be specified, to indicate when each bit becomes valid, and for how long. In general, the *timing* of the whole conversion process must be clearly understood, especially if high speeds are necessary, either for conversion, or for communication with a processor (or both). The timing diagrams on specification sheets are usually accompanied by adequate descriptions of the conversion process and specifications of the critical interface parameters.

#### Controls

The functions, action (levels or edges), polarity, and timing of all control inputs and outputs should be clearly understood, as well as their loading characteristics and dependence on the supply. In addition to the essential *start-conversion-command* input and a *status* output, various control commands may be available, such as *clock inbibit*, *bigb (low)-byte enable*, *status enable*, and—for speeding up conversion at the cost of resolution in successive-approximation converters—*short-cycle*.

#### **Power Supplies**

Appropriate power supplies should be made available, considering the logic levels and analog input signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specifications should be provided. Any recommended external protection circuitry should be planned for. In many cases, separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

For video converters, use massive, low-impedance ground systems. The analog and digital grounds are connected together inside converters of these types, so bus bars are essential for system grounding and power distribution; use lots of ground plane on PC boards.

#### **Application Checklist**

The designer will generally require specific information in the following categories, before proceeding to the selection process:

- Accurate description of input and output
  - 1. analog signal range and source or load impedance

2. digital code needed – binary, offset binary, 2's complement, BCD, etc.

- 3. logic level system, i.e., TTL/DTL/ECL compatible
- What are the needed analog bandwidth and data throughput rate?
- What are the control interface details?
- What does the system error budget allow for the converter?
- What are environmental conditions temperature range, time, supply voltage – over which the converter should operate to the desired accuracy?

For A/D converters, the following considerations are typical.

- What is the analog input voltage range, and to what resolution must the signal be measured?
- What is the requirement for linearity error (or relative accuracy error)?
- To what extent must the various sources of error be minimized as environmental temperature changes?
- How much time can be allowed in the system for each complete conversion? What aperture uncertainty and acquisition time are needed for the sample-hold?
- How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
- Can the system tolerate missed codes under any conditions?
- What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? Is aliasing a potential problem?

#### SPECIFICATIONS & TERMS

Definitions of performance specifications, and related information, are to be found on the following pages, in alphabetical order.\*

• For video converters, there are a number of additional applicationoriented specifications pertaining to the device's use in a system (e.g., noise power ratio, differential phase, differential gain, signal-tonoise ratio). Some useful references for understanding such specifications can be found in the following publications, available from Analog Devices, Computer Labs Division 7810 Success Road, Greensboro NC 27409.

- Kester, W.A., "PCM Signal Codecs for Video Applications", SMPTE Journal, Volume 88, November 1979, pp 770-778.
- Pratt, W.J., "Test A/D Converters Digitally", Electronic Design, December 6, 1975
- Smith, B.F. and Pratt, W.J., "Understanding High-Speed A/D Converter Specifications", Computer Labs, 1974

#### Accuracy, Absolute

The error of an A/D converter at a given output code is the difference between the theoretical and the actual analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see Quantizing Uncertainty), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code. For example, if 5 volts ( $\pm$ 1.2mV) will theoretically produce a 12-bit half-scale code of 100000000000, then a converter for which any voltage from 4.997V to 4.999V will produce that code will have absolute error of 1/2(4.997 + 4.999) - 5 volts = -2mV.

Absolute error comprises gain error, zero error, and nonlinearity, together with noise, Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

#### Accuracy, Relative

Relative accuracy error, expressed in %, ppm, or fractions of an LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

The "discrete points" of an A/D transfer characteristic may be the midpoints of the quantization bands at each code (see Accuracy, Absolute), or—for convenience— the ideal transitions, which are displaced by 1/2LSB.

#### Aperture Time

This is the interval between the application of the *bold* command to a sample/track-hold and the actual opening of the switch. The aperture time consists of a delay (which depends on the logic and the switching device-50ns for SHA1144) and an uncertainty (due to jitter-20ps max rms for HTS-0025). When a sample-hold is used in an application where timing is critical, the timing of the hold command can be advanced to compensate for the known component of aperture delay. The jitter, however, imposes the ultimate limitation on timing accuracy. When a sample-hold is used with an ADC, the timing uncertainty of the conversion process is reduced by the ratio of aperture jitter to the conversion time, i.e., the maximum frequency which can be handled with less than 1LSB error due to timing is  $2^{-n}/(\pi \tau_{au})$  instead of  $2^{-n}/(\pi \tau_c)$ , where  $\tau_{au}$  is the aperture uncertainty and  $\tau_c$  is the conversion time.

#### **Common Mode Rejection (CMR)**

The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 1,000,000 to 1 means that a 1V common-mode voltage passes through the amplifier as through it were a differential signal of one microvolt at the input.

#### **Conversion Time and Conversion Rate**

The time required for a complete measurement by an ADC is called *conversion time*. For most converters (assuming no significant additional systemic delays), this is identical to the inverse of *conversion rate*. However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined; thus, for example, the MOD-1205 can provide 12-bit output data at a 5MHz word rate (200ns/conversion), even though the time for any one conversion, from start to finish, is two clock periods plus 275ns, or 675ns, at 5MHz.

#### **Dual-Slope Converter**

An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time-interval meter (i.e., counter) is generally used as the output indicator.



#### Feedthrough

Undesirable signal-coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedtbrough error* in a multiplexer. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

#### "Flash" Converter

A converter in which all the bit choices are made at the same time. It requires  $2^n - 1$  voltage-divider taps and comparators, and a comparable amount of priority encoding logic. An extremely fast scheme, it requires large numbers of precision components. Flash converters are often used for partial conversions in subranging converters.

#### Gain Adjustment

The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g., 10V full scale, in a fixed-reference converter, or 100% of full-scale in a ratiometric converter. Gain- and zero-adjustment principles are discussed under zero.

#### Least Significant Bit (LSB)

In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or  $2^3 + 2^2 + 0 + 2^0$ ), the rightmost "1" is the LSB. Its analog weight, relative to full scale, is  $2^{-n}$ , where n is the number of binary digits. It represents the smallest change that can be resolved by an n-bit converter.

#### Linearity Error

Linearity error of a converter, expressed in percent or partsper-million of full-scale range, or fractions of a least-significant bit, is the deviation of the analog values from a straight line, in a plot of the measured conversion relationship. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated. Sometimes referred to as "end-point" nonlinearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Accuracy, Relative). Linearity has two components*differential* and *integral* nonlinearity.

#### Linearity, Differential and Integral

A digital output code should correspond to a quantum of analog input values exactly 1 LSB in width  $(2^{-n} \text{ of full scale},$ for an n-bit converter). Any deviation of the measured "step" from the ideal width is called Differential Nonlinearity. It is an important specification, because a differential nonlinearity error greater than 1 LSB can lead to nonmonotonic behavior of of a D/A converter, and missed codes in an A/D converter employing such a DAC. A flagrant example of differential nonlinearity is shown here. 11



In the illustration, the horizontal bars represent the measured DAC output values corresponding to 6 adjacent digital codes. The DAC is nonlinear, in that the next-least-significant bit (XX010) is 1½ LSB too large. Thus, instead of the five quanta, or steps, being all equal (= 1 LSB), quantum 2 is 2½ LSB and quantum 4 is -½ LSB. The differential linearity error, the difference between the actual quantum width and the ideal 1 LSB, is +1½ LSB for quantum 2 and -1½ LSB for quantum 4.

When this DAC is used in successive-approximations conversion, it will lead to a missed code. Analog inputs slightly larger than the value of XX100 will be converted to XX100, and analog inputs slightly less than the value of XX100 will be converted to XX010. The code XX011 will not exist; it will be a missed code.

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of "no missed codes", which implies a differential nonlinearity less than 1 LSB.

While differential nonlinearity deals with errors in step size, *integral nonlinearity* has to do with deviations of the overall shape of the conversion response. Even converters that are not subject to differential linearity errors (e.g., integrating types) have integral linearity (sometimes just "linearity") errors.

#### **Power-Supply Sensitivity**

The sensitivity of a converter to dc changes in power-supply voltages is normally expressed in terms of percentage change in analog input value (or fractions of the analog equivalent of 1 LSB), corresponding to a given code, for a 1% dc change in the power supply, e.g.,  $0.05\%/\%\Delta V_S$ ). Power-supply sensitivity may also be expressed in relation to a specified dc shift of the supply voltage. High-accuracy ADCs intended for battery operation require excellent rejection of large supply-variations.

#### Quad-Slope Converter

This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter. For example, the 13-bit singlechip AD7550 is a CMOS quad-slope A/D converter with typical tempcos (gain and zero temperature coefficients) of 1ppm/°C.

#### Quantizing Uncertainty (or "Error")

The analog continuum is partitioned into  $2^n$  discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of  $\pm \frac{4}{2}$  LSB, in addition to the actual conversion errors. In integrating converters, this "error" is often expressed as " $\pm 1$  count."

#### **Ratiometric Converter**

The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage (e.g., the voltage applied to a bridge), it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation. Ratiometric conversion can also serve as a substitute for analog signal division (where the denominator changes but little during the conversion).

#### Stability

Stability of a converter, usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see "Temperature Coefficients").

#### Subranging Converters

In this type of converter, an extremely fast conversion produces the most-significant portion of the output word. This portion is converted back to analog with a fast high-accuracy D/A converter and subtracted from the input. The resulting residue is converted to digital at high speed and combined with the results of the earlier conversion to form the output word. In *digitally corrected subranging* (DCS), the two bytes are combined in a manner that corrects for the error of the LSB of the most-significant byte. For example, using 8-bit and 5-bit conversion, and this proprietary technique, a full-accuracy high-speed 12-bit converter can be built.

#### Successive Approximations

Successive approximations is a high speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, 1/16 gram, etc. The weights are tried in order, starting with the largest. Any weight that tips the scale is removed. At the end of the process, the sum of the weights remaining on the scale will be within one LSB of the actual weight ( $\pm$ ½ LSB, if the scale is properly biased — sce zero).

#### **Temperature Coefficients**

In general, temperature instabilities are expressed in %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include gain, linearity, offset (bipolar), and zero. The last three are expressed in % or ppm of full-scale range per Celsius degree.

**Gain Tempco:** Two factors principally affect converter gain instability with temperature:

a) In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of an AD581L is typically 5ppm/°C.

b) The ratiometric circuitry has a sensitivity to temperature.

**Linearity Tempco:** Sensitivity of linearity to temperature over the specified range. To avoid missed codes, it is sufficient that the differential nonlinearity error be less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a specified temperature range, and/or implied by a statement that there are no missed codes when operating within a specified temperature range.

**Offset Tempco** The temperature coefficient of the all-DAC-switches-off (minus full-scale) point, of a bipolar successive-approximations converter, is dependent on three variables:

1) The tempco of the reference source

2) The voltage stability of the input buffer and the comparator

3) The tracking capability of the bipolar-offset resistors and the gain resistors.

Unipolar Zero The zero tempco of an ADC is dependent only on the zero stability of the integrator and/or the input buffer and the comparator. It may be expressed in  $\mu V/^{\circ}C$ , or in percent or ppm of full-scale per degree C.

#### Zero- and Gain-Adjustment Principles

The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at  $\frac{1}{2} \times 2^{-n}$  of nominal full-scale. The gain is set for the final transition



to all-bits-on to occur at F.S.  $(1 - \frac{3}{2}x 2^{-n})$ . The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at -F.S.  $(1 - 2^{-n})$  and the last transition at +F.S.  $(1 - 3x 2^{-n})$ . The data sheet instructions should be followed.





### VOL. II, 11-26 ANALOG-TO-DIGITAL CONVERTERS

# 

## 14-Bit High Speed Analog-to-Digital Converters

## ADC1130, ADC1131

#### FEATURES

14-Bit Resolution and Accuracy Fast 12µs Conversion Time (ADC1131J/K) Low 10ppm/°C Maximum Gain TC User Choice of Input Range No Missing Codes

#### APPLICATIONS

Wide Band Data Digitizing Multi-Channel Computer Interface High Accuracy Data Acquisition X-Ray Tomography Nuclear Accelerator Instrumentation

#### GENERAL DESCRIPTION

The ADC1130 and ADC1131 are high speed analog-to-digital converters packaged in a small 2" x 4" x 0.4" (51 x 102 x 10mm) module, which perform complete 14-bit conversions in 25 $\mu$ s and 12 $\mu$ s respectively. Using the successive approximations technique, they convert analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V,  $\pm$ 10V,  $\pm$ 5V. The user selects the desired range by making appropriate connections to the module terminals. The ADC1130 and ADC1131 can also be connected so as to perform conversions of less than 14 bit resolution with a proportionate decrease in conversion time.

#### TIMING

As shown in Figure 1, the leading edge of the convert command set the MSB output to Logic "0" and the CLOCK OUT, STATUS, MSB, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-toanalog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 14 (LSB) com-



parison is completed. At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the fourteen "0" to "1" clock transitions.



Figure 1. Timing Diagram

## **SPECIFICATIONS**

#### (typical @ +25°C unless otherwise noted)

	HIGH SPEED 12µs		MEDIUM SPEED 25µs
VODE	ADC1131		ADC1130 D
MODEL	J	ĸ	
RESOLUTION, BITS	14	14	14
CONVERSION TIME (max)	12µs	12µs	25µs
ACCURACY Integral Nonlinearity Error (LSB) Differential Nonlinearity Error (LSB) Missing Codes	±1/2 (max) ±1/2 (1 max) No missing codes	• ±1/2 (max) •	• ±1/2 (1 max) •
TEMPERATURE COEFFICIENTS Gain ppm/°C Unipolar Offset Bipolar Offset	±12 (max) ±0.7 (±3 max) ±3 (±7 max)	±7 (+10 max) •	±12 max •
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V	•	•
INPUT IMPEDANCE (10V RANGE)	2500Ω	•	•
CONVERT COMMAND	Positive Pulse, 200ns min, 400ns max Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible	•	•
PARALLEL DATA OUTPUT Unipolar Bipolar	Positive True Binary Positive True Offset Binary, Two's Complement	•	•
SERIAL DATA OUTPUT			
Unipolar Bipolar	Positive True Binary Positive True Offset Binary	•	•
STATUS OUTPUT	"1" During Conversion. Complement also available TTL/DTL Compatible.	•	• N
LOGIC FANOUTS AND LOADINGS Convert Command Input Clock Input Short Cycle Input Parallel Data Outputs Serial Data Output STATUS Output STATUS Output Clock Output	1TTL Unit Load 3TTL Unit Loads 1TTL Unit Loads 3TTL Unit Loads/Bit 8TTL Unit Loads/Bit 2TTL Unit Loads 12TTL Unit Loads 4TTL Unit Loads	•	
POWER REQUIREMENTS	+15V ±5% @ 40mA -15V ±5% @ 60mA +5V ±5% @ 250mA	•	
POWER SUPPLY SENSITIVITY To ±15V Tracking Supplies Gain Zero To ±15V Non-Tracking Supplies Gain Zero	<sup>±4.5ppm/%ΔVS</sup> ±4.5ppm/%ΔVS ±10ppm/%ΔVS ±7ppm/%ΔVS	•	1 0 3 0 5 0 6 0
TEMPERATURE RANGE Operating Storage	0 to +70°C -55°C to +85°C	•	•

\*Same Specifications as ADC1131J.

NOTES 'Offset (zero) and gain errors are adjustable to zero by means of external potentiometers. See Figure 5 for proper connection. <sup>a</sup> Recommended power supply: Analog Devices model 923.

Specifications subject to change without notice.



mensions shown in inches and (mm).



#### DTE:

rminal pins installed only in shaded hole cations.

odule weight: 3.5 ounces (99.3 grams). II pins are gold plated half-hard brass IIL-G-45204), 0.019" ±0.001" (0.48 .03mm) dia.

or plug-in mounting card order Board . AC1578.

#### **BLOCK DIAGRAM** AND PIN DESIGNATIONS



#### ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1130 and ADC1131 are shown in block diagram form.



Figure 2. Input Circuit Block Diagram

When the converters are connected as a unipolar device, Pin 19 is left open circuit and, thus, no offset current is applied to the comparator input. The 0 to +10V input signal applied to Pin 6 (or the 0 to +20V input signal applied to Pin 5) develops a 0 to +4mA current which is compared to the 0 to -4mA output of the D/A converter. A voltage between +15V and -15V can be applied to Pin 20 from the wiper of a 100k $\Omega$  potentiometer to adjust the zero point by ±40LSB. To reduce the range of this trim padding resistors should be used.

With the offset output, Pin 22, connected to Pin 19, a +2mA offset current is applied to the comparator input. The ADC1130 and ADC1131 will then accept bipolar inputs of  $\pm 5V$  at Pin 6, or  $\pm 10V$  at Pin 5 and compare the 0 to +4mA sum of the offset and input signal currents to the 0 to -4mA D/A converter output. The offset adjustment potentiometer is once again used as described in the preceding paragraph.

Signal ground sense, Pin 23, should normally be jumpered to analog ground, Pin 3. In the event that an offset voltage is developed in the ground wiring, it may be possible to eliminate its effect by connecting Pin 23 directly to the signal or analog ground of the device feeding the analog input signal to the ADC. In any case, Pin 23 must not be left open.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer.

#### PARALLEL DATA OUTPUT

These converters produce natural Binary Coded outputs when configured as a unipolar device. As a bipolar device, they can produce either Offset Binary or Two's Complement output codes. The most significant bit is represented by Pin 72 (MSB output) for Binary and Offset Binary codes, or by Pin 70 (MSB output) for the Two's Complement code. Tables I and II illustrate the relationship between analog input and digital output for all three codes.

ANALOG INPUT		DIGITAL OUTPUT	
0 to +10V 0 to +20V Range Range		Binary Code	
+9.9994V	+19.9988V	1111111111111111	
+5.0000V	+10.0000V	10000000000000	
+1.2500V	+2.5000V	00100000000000	
+0.0006V	+0.0012V	000000000000001	
+0.0000V	+0.0000V	00000000000000	

Table I. Nominal Unipolar Input-Output Relationships

## Applying the ADC1130, ADC1131

±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.9994V	+9.9988V	1111111111111111	01111111111111
+2.5000V	+5.0000V	11000000000000	01000000000000
+0.0006V	+0.0012V	100000000000001	000000000000000000000000000000000000000
+0.0000V	+0.0000V	10000000000000	000000000000000000
-5.0000V	-10.0000V	000000000000000	10000000000000

Table II. Nominal Bipolar Input-Output Relationships

#### SERIAL DATA OUTPUT

The serial data output, available on Pin 32, is of the non-returnto-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the converter.



Figure 3. Serial Data Transmission

The timing diagram presented in Figure 4 shows that the conyerter's clock output must be delayed by an amount of time greater than or equal to the sum of the receiving shift register setup time plus the 20ns clock output to serial output delay.



#### Figure 4. Serial Data Timing Diagram

The 50ns span between the time that the last serial output bit is available and the time that the STATUS output returns to zero insures that the data in the shift register will be valid on the "1" to "0" transition of the STATUS signal.

#### GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 5. Note that a jumper



#### Figure 5. Adjustment Connections

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is connected between Pin 19 and Pin 22 for bipolar operation; these pins *must* be left open for unipolar operation.

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within  $1\mu V$  of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment is made first. These adjustments are not made with zero and full scale input signals and it may be helpful to understand why. An A/D converter will produce a given digital output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the output of the converter to be on the verge of switching from one digital value to the adjacent digital value, the unit can be calibrated so that it does change values at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' Analog-Digital Conversion Notes gives more detailed information on testing and calibrating A/D and D/A converters.

#### OFFSET CALIBRATION

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V; for 0 to +20V units set it to +0.0006V. Adjust the zero potentiometer until the converter is just on the verge of switching from  $00 \dots 0$  to  $00 \dots 1$ .

For the  $\pm 5V$  bipolar range set the input voltage precisely to -4.9997V; for  $\pm 10V$  units set it to -9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . 0 to 00 . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

#### GAIN CALIBRATION

Set the input voltage precisely to  $\pm 19.9982V$  for 0 to  $\pm 20V$ units,  $\pm 9.9991V$  for 0 to  $\pm 10V$  units,  $\pm 4.9991V$  for  $\pm 5V$ units, or  $\pm 9.9982V$  for  $\pm 10V$  units. Note that these values are  $\pm 125B's$  less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from  $\pm 11...0$  to  $\pm 11...1$ and two's complement coded units are just on the verge of switching from  $\pm 0.11...1$ 

#### POWER SUPPLY AND GROUNDING CONNECTIONS

These converters do not have an internal connection between analog power ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. One suggested approach is shown in Figure 6.



Figure 6. Power Supply and Grounding Connections

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The  $\pm 15V$  and  $\pm 5V$  power supplies must be externally bypassed with  $15\mu$ F ( $\pm 35V$  tantalum) capacitors. These capacitors should be connected between Pin 27 and Pin 3, between Pin 25 and Pin 3, and between Pin 29 and Pin 30. Capacitor connections should be made as close to the module pins as possible.

#### **CLOCK CONNECTIONS**

When the converters are used with their own internal clock, Pin 36 is simply jumpered to Pin 35. When the internal clock is not used, Pin 36 is grounded and an external clock capable of driving three TTL loads is connected to Pin 35. The convert command should be synchronized with the external clock.

#### **REPETITIVE CONVERSIONS**

When making repetitive conversions, a new convert command may be initiated any time after the "1" to "0" transition of the STATUS output. The STATUS output may not, however, be connected directly to the CONVERT COMMAND input for the purpose of automatically generating convert command pulses.

#### SHORT CYCLE CONNECTIONS

When the converters are operated as a 14-bit device, Pin 37 is left open. If, however, it is to perform conversions of less than 14 bits, Pin 37 is connected to the N+1 bit output (where N is the number of bits in the conversion). The conversion time in this mode of operation is  $T_C \ge N/14$  where  $T_C$  is the conversion time of the particular model when operated at 14-bit resolution.

#### THE AC1578 MOUNTING CARD

The AC1578 mounting card is specifically designed to be used with Analog Devices high resolution, high speed analog-todigital converters, models ADC1130 and ADC1131. This  $4.5'' \times 3.56''$  (114  $\times$  90mm) printed circuit card, shown in Figure 7, has sockets which allow the converter to be plugged directly onto it. It contains an input buffer that can be programmed using on-board jumpers to provide the input ranges of 0-10 volts, ±10 volts, or ±5 volts. Additionally, a 0-20 volt input range can be achieved by wiring the AC1578 without utilizing the buffer.

The analog information has been isolated from the digital information by the use of two separate connectors, one at the top (designated "P1") and one at the bottom (designated "P2") of the AC1578. Both connectors P1 and P2 are supplied with each card. Whenever feasible, the top connector should be used for analog interfacing to eliminate crosstalk.

Additional wiring information and calibration procedure are contained in a separate data sheet for the AC1578 which is shipped with the card and is available on request.



Figure 7. AC1578 Mounting Card



## Low Cost 16-Bit Analog-to-Digital Converter

ADC1140

#### **FEATURES**

Guaranteed Nonlinearity:  $\pm 0.003\%$  FSR max 35 $\mu$ s Maximum Conversion Time Small Size 2"  $\times$  2"  $\times$  0.4" Wide Power Supply Operation:  $\pm 12V$  to  $\pm 17V$ 

#### APPLICATIONS

Process Control Data Acquisition Seismic Data Acquisition Nuclear Instrumentation Medical Instrumentation Pulse Code Modulation Telemetry Industrial Scales Robotics



#### **GENERAL DESCRIPTION**

The ADC1140 is a low cost 16-bit successive-approximation analog-to-digital converter having a 35 $\mu$ s maximum conversion time. This converter provides high accuracy, high stability and low power consumption all in a 2"  $\times$  2"  $\times$  0.4" module.

High accuracy performance such as integral and differential nonlinearity of  $\pm 0.003\%$  FSR max are both guaranteed. Guaranteed stability such as differential nonlinearity TC of  $\pm 2ppm$ /°C maximum, offset TC of  $\pm 30\mu V/°C$  maximum, gain TC of  $\pm 12ppm/°C$  maximum and power supply sensitivity of  $\pm 0.002\%$  of FSR/% V<sub>S</sub> are also provided by the ADC1140. The ADC1140 makes extensive use of both integrated circuit and thin-film components to obtain excellent performance, small size and low cost. The internal 16-bit DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary CMOS current-steering switches. A low noise reference, low power comparator and low power successive-approximation register are also used to optimize the ADC1140's design (shown in Figure 1).

The ADC1140 can operate with power supplies ranging from  $\pm 12V$  to  $\pm 17V$  and has provisions for a user supplied external reference. Four analog input voltage ranges are selectable via pin programming:  $\pm 5V$ ,  $\pm 10V$ , 0 to  $\pm 5V$  and 0 to  $\pm 10V$ . Bipolar coding is provided in the offset binary and two's complement formats with unipolar coding displayed in true binary.

ADC1140 FUNCTIONAL BLOCK DIAGRAM



## **SPECIFICATIONS** (typical @ +25°C $\pm$ V<sub>S</sub> = $\pm$ 15V, V<sub>CC</sub> = +5V, V<sub>REF</sub> = +10.0V unless otherwise specified)

Model	ADC1140
RESOLUTION	16 Bits
CONVERSION TIME	35µs max
ACCURACY <sup>1</sup>	
Nonlinearity Error	±0.003% FSR <sup>2</sup> max
Differential Nonlinearity Error	±0.003% FSR <sup>2</sup> max
STABILITY	
Differential Nonlinearity	±2ppm/°C max
Gain (with internal reference)	±12ppm/°C max
(without internal reference)	±4ppm/°C max
Unipolar Offset	$\pm 30\mu V/^{\circ}C$ max
Bipolar Offset	±7ppm/°C max
POWER SUPPLY SENSITIVITY	±0.002% FSR/% V <sub>S</sub>
ANALOG INPUT	
Voltage Ranges	
Bipolar	±5V, ±10V
Unipolar	0 to $+5V$ , 0 to $+10V$
Input Resistance	A 11 O
0 to +5V	2.5k12
$0 to +10V, \pm 5V$	5.0K32
External Deferonce Input <sup>3</sup>	10.0832
Voltage Range	$0 \pm 12V$
Input Resistance	2 5kΩ
	2, J K 12
Convert Command	Positive Pulse, 100ns Width min
Convert Communa	Negative Edge Triggered
Logic Loading	1TTL Load
DIGITAL OUTPUT	
Parallel Output Data	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN) Two's Complement
Output Drive	1TTL Load
Status	Logic "1" During Conversion
Output Drive	1TTL Load
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%
External Load Current	
(Rated Performance)	2mA max
Temperature Stability	±8.5ppm/ C max
POWER REQUIREMENTS*	· · · · · · · · · · · · · · · · · · ·
Voltage (Rated Performance)	$\pm 15V \pm 3\%, \pm 5V \pm 3\%$
Voltage (Operating)	$\pm 12V$ to $\pm 17V$ , $\pm 4.75V$ to $\pm 5.25V$
Supply Current Drain ±15 V	±25mA
+3 V	
TEMPERATURE RANGE	0 m 170°C
Specified	
Storage	$-25$ C to $+85^{\circ}$ C
SIZE	2 X 2 X 0.4 (51 X 51 X 10,4mm)
weight	1.2 02 (33g)

NOTES

<sup>1</sup>Offset and gain error are adjustable to zero by means of external potentiometers. See Figure 3 for proper connection.

<sup>2</sup> FSR means Full Scale Range.

<sup>3</sup>Rated performance is specified with +10.0V reference.



**OUTLINE DIMENSIONS** Dimensions shown in inches and (mm).

5	BIT 2	28 ANALOG IN 2
6	BIT 3	27 ANALOG IN 3
7	BIT 4	26 +10V REFOUT
8	BIT 5	25 REFERENCE IN
9	BIT 6	24 OFFSET ADJUST
10	BIT 7	23 NOT USED
11	BIT 8	22 STATUS
12	BIT 9	21 CONVERT COMMAND
13	BIT 10	20 NOT USED
14	BIT 11	19 LSB
15	BIT 12	18 BIT 15
1 16	BIT 13	17 BIT 14

#### OTHER HIGH RESOLUTION PROD-UCTS FROM ANALOG DEVICES:

- 14-Bit/15-Bit Sampling A/D Converters; DAS1152/53
  - 25kHz (14-Bit)/20kHz (15-Bit) throughput rates
  - Second Source to A/D/A/M824 and A/D/A/M825 Modules
- 14-Bit/15-Bit Low Level Data Acquisition Systems: DAS1155/56
  - 25kHz (14-Bit)/20kHz (15-Bit) throughput rates
  - High Performance PGIA (1V/V-1000V/V), SHA and A/D Converter
- 14-Bit Sample-Hold Amplifier: SHA1144

- Acquisition Time: 8µs max to ±0.003% (20V step)

Recommended Power Supply: Analog Devices Model 923. Specifications subject to change without notice.

## Applying the ADC1140

#### **OPERATION**

For operation, the only connections to the ADC1140 that are necessary are the power supplies, internal or external reference, input voltage pin programming, convert command and digital output. Refer to Table I for input pin programming and Figure 3 for offset and gain calibration.



Figure 2. Analog Input Block Diagram

#### ANALOG INPUT PROGRAMMING

The analog input section consists of three analog input terminals. Analog input range selection is accomplished by pin programming as shown in Table I.

In the unipolar mode, a 0 to +10V or a 0 to +5V input signal develops a 0 to +2mA current that is compared to the 0 to -2mA (shown in Figure 2) current output of the DAC.

In the bipolar mode, a +1mA offset current from the reference is applied to the comparator input via pin programming connections. The ADC1140 can then accept either  $\pm 5V$  or  $\pm 10V$ inputs. These inputs again will be converted to current and compared with the DAC's 0 to -2mA current output.

Input Signal Range	Coding	Connect Input Signal To Pin(s)	Connect Pin 26 To Pin*	Connect Pin 30 To Pin(s)
±10V	OBIN, Two's Comp	28	27	29, 2
±5V	OBIN, Two's Comp	29	27	28,2
0 to +5V	BIN	27, 28, 29	Open	2
0 to +10V	BIN	27, 28	Open	29, 2

<sup>4</sup>If Internal Reference is used, Pins 25 and 26 must be connected together through a 50 $\Omega$  potentiometer or 24.9 $\Omega$  fixed resistor (see Figure 3 and the gain calibration section).

Table I. Analog Input Voltage Pin Programming

#### **OPTION OFFSET & GAIN CALIBRATION**

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of an accurate and stable voltage reference. The voltage standard used as a signal source must be very stable. It should be capable of being set to within  $1\mu$ V of the desired value at both ends of its range. The potentiometers selected should be of the good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

By adjusting the offset first, gain and offset adjustments will remain independent of each other.



Figure 3. Offset and Gain Calibration

#### OFFSET CALIBRATION

For 0 to +10V range, set the input voltage precisely to  $+76\mu$ V; for 0 to +5V range, set it at  $+38\mu$ V. Adjust the zero potentiometer until the binary coded converter is just on the verge of switching from 000...01.

For  $\pm 5V$  range, set the input voltage precisely to -4.999924V; for  $\pm 10V$  range, set it at -9.999847V. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000...00 to 000...01 and the two's comp. coded units are just on the verge of switching from 100...0 to 100...1.

#### GAIN CALIBRATION

Set the input voltage precisely at +9.99977V for 0 to +10Vinput range, +4.99977V for  $\pm 5V$  input range, +9.99954V for  $\pm 10V$  input range, or +4.99988V for 0 to +5V input range, adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from  $111 \dots 0$ to  $111 \dots 1$  and two's comp. coded units are just on the verge of switching from  $011 \dots 10$  to  $011 \dots 11$ . Note that these values are 1 1/2 LSBs less than nominal full scale.

#### POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally. The connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1140 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.



Figure 4. Power Supply and Grounding Techniques

#### ADC1140 TIMING

Conversion is initiated with the negative going edge of the Convert Command pulse as shown in Figure 5. The Convert Command pulse width must be a minimum of 100ns. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the Convert Command pulse, all internal logic is reset. The MSB is set low with the remaining digitial outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 16-bit conversion taking  $35\mu$ s maximum. At this time, the STATUS line goes low signifying that the low conversion is complete.



Figure 5. ADC1140 Timing Diagram

#### ANALOG INPUT/OUTPUT RELATIONSHIPS

The ADC1140 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is displayed on pin 4 for the binary and offset binary codes or on pin 3 for the two's complement code. Table II shows the unipolar analog input/digital output relationships. Table III shows the bipolar analog input/digital output relationships for offset binary code and two's complement codes.

Analog Ing	out	Digital Output
0 to +5V	0 to +10V	
Range	Range	Binary Code
+4.999924V `	+9.99985V	1111 1111 1111 1111
+2.50000V	+5.00000V	1000 0000 0000 0000
+1.25000V	+2.50000V	0100 0000 0000 0000
+0.62500V	+1.25000V	0010 0000 0000 0000
+0.000076V	+0.000153V	0000 0000 0000 0001
+0.00000V	+0.00000V	0000 0000 0000 0000

Table II. Unipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	2's Complement Code
+4.99985V	+9.99970V	1111 1111 1111 1111	0111 1111 1111 1111
+2.50000V	+5.00000V	1100 0000 0000 0000	0100 0000 0000 0000
+0.000153V	+0.000305V	1000 0000 0000 0001	0000 0000 0000 0001
+0.00000V	+0.00000V	1000 0000 0000 0000	0000 0000 0000 0000
-5.00000V	-10.00000V	0000 0000 0000 0000	1000 0000 0000 0000

Table III. Bipolar Input/Output Relationships

#### HIGH RESOLUTION DATA ACQUISITION SYSTEM

Shown in Figure 6 is a high resolution data acquisition system. Here the SHA1144, a high resolution sample-hold amplifier, is used to drive the ADC1140. Conversion is initiated by the

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negative edge of the convert command pulse. At this time the STATUS pulse goes low causing the SHA1144 to go from the sample mode to the hold mode. When the conversion is complete,  $35\mu$ s later, the STATUS pulse goes low, thus placing the SHA1144 in the sample mode.



Figure 6. High Resolution Data Acquisition System

#### EXTERNAL REFERENCE

The ADC1140 is capable of operating with an external +10.0V reference. Simply disconnect the gain trim potentiometer from pin 26 and connect it to the external reference as shown in Figure 7. The external reference output must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained. Gain error is adjusted as previously discussed in the gain calibration section.



#### Figure 7. External Reference

The ADC1140 is factory tested and calibrated with the internal +10.0V reference voltage but nonstandard external voltages can be used with the digital output coding being determined by the formula shown in Figure 7.

#### PIA INTERFACE

The ADC1140 can be used with a PIA to interface directly to a microprocessor. As shown in Figure 8 the 16-bit output of the ADC1140 is split into two 8-bit bytes. Part A of the PIA is programmed to read the eight most-significant-bits while Part B reads the eight least-significant-bits. Output CB2 is used to start the ADC1140 conversion process. CB1, of the PIA, is used to sense the STATUS of the ADC1140 so that the end of conversions can be determined. The control bus, address bus, and data bus are then connected directly to the microprocessor.

With the use of PIAs, control of one or more ADC1140s can be accomplished in many different configurations.



Figure 8. ADC1140 Interface to PIA

# 

## Low Power/High Performance 16-Bit A/D Converter

## ADC1143

#### FEATURES

Low Power Consumption:  $175 \text{mW} \text{ max}, \text{V}_{\text{S}} = \pm 15 \text{V}$  $150 \text{mW} \text{max}, \text{V}_{\text{S}} = \pm 12 \text{V}$ **Guaranteed Nonlinearity:** ±0.006% FSR max (ADC1143J) ±0.003% FSR max (ADC1143K) **Guaranteed Differential Nonlinearity:** ±0.006% FSR max (ADC1143J) ±0.003% FSR max (ADC1143K) Low Differential Nonlinearity T.C.: ±2ppm/°C max (ADC1143J) ±1ppm/°C max (ADC1143K) **Fast Conversion Time:** 70µs max (ADC1143J) 100µs max (ADC1143K) Wide Power Supply Operation:  $V_{s} = \pm 11.4V$  to  $\pm 18.0V$  $V_{\rm D} = +3.0V$  to +18.0V

APPLICATIONS Seismic Data Acquisition Oil Well Instrumentation Portable Industrial Scales Portable Test Equipment Robotics

#### **GENERAL DESCRIPTION**

The ADC1143 is a low power 16-bit successive-approximation analog-to-digital converter with a maximum power consumption of 175mW at  $V_S = \pm 15V$ , 150mW at  $V_S = \pm 12V$ , and is contained in a  $2'' \times 2'' \times 0.4''$  module.

High performance like integral nonlinearity of  $\pm 0.006\%$  FSR (ADC1143J)/ $\pm 0.003\%$  FSR (ADC1143K) and differential nonlinearity of  $\pm 0.006\%$  FSR (ADC1143J)/ $\pm 0.003\%$  FSR (ADC1143K) are guaranteed. Additional guaranteed performance includes: differential nonlinearity T.C. of  $\pm 2ppm^{\rho}C$  (ADC1143J)/ $\pm 1ppm^{\rho}C$  (ADC1143K), offset T.C.  $\pm 40\mu$ V/°C and gain T.C.  $\pm 12ppm^{\rho}C$ .

The ADC1143 makes extensive use of CMOS integrated circuits and thin-film components to obtain low power consumption, excellent performance and small size. The internal 16-bit CMOS DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary current steering switches. CMOS successive-approximation registers, low power comparator and low noise reference are also used to optimize the performance of the ADC1143 (shown in Figure 1).



The ADC1143 can operate with power supply voltages ranging from  $\pm 11.4V$  dc to  $\pm 18.0V$  dc for V<sub>S</sub> and +3V dc to +18Vdc for the V<sub>D</sub> supply. An internal voltage reference is provided, but an external reference can be used. Five analog input voltage ranges are selectable via user pin programming: +5V, +10V, +20V,  $\pm 5V$  and  $\pm 10V$ . Digital output coding in unipolar operation is true binary; for bipolar operation, the coding is offset binary or two's complement. Digital outputs are provided in both parallel and serial formats.



Figure 1. ADC1143 Functional Block Diagram

## **SPECIFICATIONS** (typical @ +25°C, V<sub>s</sub> = $\pm 15$ V, V<sub>p</sub> = +5V, V<sub>REF</sub> = +10V unless otherwise specified)

MODEL	ADC1143J	ADC1143K
RESOLUTION	16 Bits	*
CONVERSION TIME	70µs(max)	100µs(max)
ACCURACY		
Integral Nonlinearity	$\pm 0.006\%$ FSR <sup>1</sup> (max)	± 0.003% FSR <sup>1</sup> (max)
Differential Nonlinearity	$\pm 0.006\%$ FSR <sup>1</sup> (max)	± 0.003% FSR' (max)
13 Bits	Guaranteed	
14 Bits		Guaranteed
STABILITY		
Differential Nonlinearity	$\pm 2ppm/^{\circ}C(max)$	± lppm/°C(max)
Bipolar Offset	$\pm 40\mu V/C (max)$ $\pm 9ppm/^{\circ}C (max)$	*
Gain	$\pm 12 \text{ppm/}^{\circ}C(\text{max})$	*
ANALOG INPUT		
Voltage Range		. ,
Unipolar Bipolar	+5V, +10V, +20V +5V, +10V	*
Input Resistance	254, 2104	
+ 5V	2.5kΩ	*
$+10V, \pm 5V$	5.0kΩ	*
+ 20V, ± 10V External Reference Input	10.0812	•
Voltage Range <sup>2</sup>	0 to + 12V	*
Input Resistance	<u>10kΩ</u>	*
DIGITAL INPUTS		
Convert Command	Positive Pulse, 1µs width (min)	*
Logic Loading	CMOS Compatible	*
DIGITAL OUTPUTS	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·
Parallel Output Data		
Unipolar	Binary (BIN)	*
Bipolar Output Drive	CMOS Comp. 21 STTL Loads	*
Status	"0" During Conversion	*
Output Drive	CMOS Comp, 2LSTTL Loads	*
Serial Output Output Drive	CMOS Comp 11 STTL Lord <sup>3</sup>	*
Clock Output	CMOS Comp, I LSI I L Load	
Output Drive	CMOS Comp, 1 LSTTL Load	*
INTERNAL REFERENCE ( $V_{REF}$ )		
Voltage	$+10V, \pm 0.3\%$	* . *
Temperature Stability	$\pm 8.5$ ppm/°C max	*
POWERREQUIREMENTS		<u></u>
Voltage (rated performance)	$\pm 15V(\pm 5\%)$ , + 5V( $\pm 5\%$ )	*
Voltage (operating)	$\pm 11.4$ V to $\pm 18$ V, $+ 3$ V to $+ 18$ V	*
$+ V_c = + 15V$	4mA	*
$-V_{s} = -15V$	5mA	*
$+V_{D} = +5V$	4mA	*
Total Power $V_{-} = \pm 12V$ , $V_{-} = \pm 5V$	150mW/may	*
$V_{S} = \pm 15V, V_{D} = +5V$ $V_{S} = \pm 15V, V_{D} = +5V$	175mW max	*
POWER SUPPLY SENSITIVITY		
Offset	$\pm 0.001\%$ FSR/% $\pm V_S$	*
Gain	$\pm 0.001\%$ FSR/% $\pm V_{S}$	*
TEMPERATURE RANGE	0.00 + 70%	*
Operating	$-25^{\circ}$ C to $+85^{\circ}$ C	*
Storage	-25°C to +85°C	* 1
Relative Humidity	Meets MIL-STD 202E, Method 103B	*
SIZE	2"×2"×0.4"	
Weight	(50.8 × 50.8 × 10.16mm) 33σ	*
NOTES	Offset and gain errors are adjustable to zero h	y means of external potentiometers
<sup>1</sup> FSR Means Full Scale Range. <sup>2</sup> Rated performance is specified with ± 10.0V or for	See Figure 3 for proper connections.	Model 973
<sup>3</sup> LSTTL drive requires 2.2k Ω pulldown resistor.	*Specifications same as ADC1143J	
	Specifications subject to change without not	ce.

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



#### MATING CONNECTORS AC1584-3 (2 REQUIRED)

#### **PIN DESIGNATIONS**

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	-15V
3	MSB	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	CLOCK OUT
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	SERIAL OUT
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

## Applying the ADC1143

#### OPERATION

For operation, the only connections to the ADC1143 that are necessary are the power supplies, internal or external reference, input voltage pin programming, convert command and digital output. Refer to Table I for input pin programming and Figure 3 for offset and gain calibration.



Figure 2. Analog Input Block Diagram

#### ANALOG INPUT RANGE

The analog input voltage section of the ADC1143 consists of three analog input terminals (see Figure 2). Analog input voltage range selection is accomplished by pin programming as shown in Table I.

In the unipolar mode, a +5V, +10V or +20V input signal can be applied. These input voltages develop a 0 to +2mA current which is compared to the 0 to -2mA current output of the internal reference DAC in the ADC1143. In the bipolar mode, a  $\pm$ 5V or  $\pm$ 10V input signal can be applied. These input voltages develop a  $\pm$ 1mA current which is compared to a 0 to -2mA current of the internal reference DAC which is offset by +1mA, to produce a  $\pm$ 1mA current.

#### OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage reference used as a signal source must be very stable and have the capability of being set within  $\pm 1\mu V$  of the desired value. The potentiometers should be good quality cermet type. Multiturn potentiometers having ten to fifteen turns and  $\pm 100 \text{ppm}^{/2}\text{C}$  temperature coefficients will be adequate. The temperature coefficient contribution will be less than  $\pm 0.1 \text{ppm}^{/2}\text{C}$ .

By adjusting the offset first, gain and offset adjustment will remain independent of each other.

#### OFFSET CALIBRATION

For + 5V range, set the input voltage to precisely  $+38\mu$ V; for + 10V range, set it to  $+76\mu$ V; for + 20V range, set it to  $+153\mu$ V.



Figure 3. Offset and Gain Calibration

Adjust the offset potentiometer until the binary output code is on the verge of switching from 000 . . . 00 to 000 . . . 01.

For  $\pm 5V$  range, set the input voltage to precisely -4.999924V; for  $\pm 10V$  range, set it to -9.999847V. Adjust the offset potentiometer until the offset binary code is on the verge of switching between 000...00 and 000...01, and two's complement coded units are switching from 100...00 to 100...01.

#### GAIN CALIBRATION

For +5V range, set the input voltage to precisely +4.99988V; for +10V range, set it to +9.99977V; for +20V range, set it to +19.9995V. Adjust the gain potentiometer until the binary output code is on the verge of switching from  $111 \dots 10$  to 111 $\dots 11$ .

For  $\pm 5V$  range, set the input voltage to precisely  $\pm 4.99977V$ ; for  $\pm 10V$  range, set it to  $\pm 9.99954V$ . Adjust the gain potentiometer until the offset binary code is on the verge of switching from 111 ... 10 to 111 ... 11, and the two's complement coded units are switching from 011 ... 10 to 011 ... 11.

#### POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally in the ADC1143, thus the connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1143 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.



Figure 4. Power Supply and Grounding Techniques

Input Voltage Range	Output Coding	Connect Input Signal To Pin(s)	Connect Pin* 26 to Pin #	Connect Pir 30 to Pin(s)
+ 5V	BIN	27, 28, 29	open	2
+ 10V	BIN	27,28	open	2,29
+ 20V	BIN	27	open	2,28,29
$\pm 5V$	OBIN, 2's Comp	29	27	2,28
$\pm 10V$	OBIN, 2's Comp	28	27	2,29

\*If internal reference is used, Pins 25 and 26 must be connected together through a 100Ω potentiometer or 49.9Ω fixed resistor (see Figure 3 and Gain Calibration Section).

Table I. Analog Input Voltage Range Pin Programming

#### **EXTERNAL REFERENCE**

The ADC1143 is capable of operating with an external reference. Simply disconnect the gain trim potentiometer from Pin 26 and connect it to the external reference as shown in Figure 5. The ADC1143 is tested and specified with a +10.0V reference. An external reference with a voltage of 0 to +12V can be applied. The external reference must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained.

When using an external reference, the digital output coding can be determined by the formula shown in Figure 5.



Figure 5. External Reference

#### ADC1143 TIMING

Conversion is initiated with the negative going edge of the convert command pulse as shown in Figure 6. The convert command pulse width must be a minimum of  $1\mu$ s. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the convert command pulse, all internal logic is reset. The MSB is set high with the remaining bits set to logic low. The status line is set low and remains low through the full conversion cycle.

During conversion, each bit starting with the MSB is set high on the rising edge of the internal clock. The ADC's internal DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete conversion of the ADC1143J and ADC1143K



#### Figure 6. ADC1143 Timing Diagram

taking  $70\mu$ s max and  $100\mu$ s max respectively. The parallel output data is valid on the rising edge of the status line.

Serial output data is valid for each bit at the completion of clock cycle used to make the bit decision as shown in Figure 6.

#### SEISMIC DATA ACQUISITION APPLICATION

The ADC1143's low power consumption and high performance make it ideally suited for portable seismic data acquisition systems like the one shown in Figure 7. In seismic data acquisition systems, geophones are used to receive reflected shock waves from subsurface strata, induced by controlled discharge of explosives. These reflected signals may travel several miles before reaching the geophones and are difficult to discern from noise or other interference like ground roll. The low level signals from the geophones are amplified and filtered appropriately to remove the undesired signals. The conditioned signal is amplified by the PGA then held by SHA and converted to digital form by the ADC1143. The digital data is stored on an on-site recorder for later data collection and processing.



Figure 7. Seismic Data Acquisition System Block Diagram

## **ANALOG** DEVICES

**No External Circuits Required** 

FEATURES 9-Bit Resolution 20MHz Word Rate Single 35-In<sup>2</sup> PC Board ECL Compatible

APPLICATIONS Television Digitizing Radar Digitizing Medical Instrumentation Digital Communications Spectrum Analysis

## 9-Bit Video Analog-to-Digital Converter

CAV-0920

#### **GENERAL DESCRIPTION**

The Analog Devices model CAV-0920 A/D converter combines performance, size, and economy to achieve a remarkable solution for high-speed digitizing problems.

The unit provides digital data with 9-bits of resolution at word rates from dc through 20MHz. It is a complete answer to the question of digitizing video, radar, and other high-frequency inputs; it includes a track-and-hold, along with encoding and timing circuits. The CAV-0920 is a "system solution" for the designer who wants to avoid the need to combine the plethora of components necessary to make IC encoders operate as functional A/D converters.

The unique digital correcting subranging (DCS) conversion technique used in the design virtually eliminates the errors normally associated with subranging A/D converters.

The CAV-0920 is constructed on a single PC board intended for mounting on a "mother" board in the user's system. Its small size makes it adaptable to a wide range of mother board sizes and allows room for including other (signal conditioning, processing, memory, etc.) circuits adjacent to the converter.

All inputs and outputs are ECL compatible. The A/D requires only an encode command and external power supplies for operation. Analog input impedance is 500 ohms/volt, making it easy to match lower impedances within the system.

Gain and offset potentiometers on the PC card permit adjusting the input for optimum system operation.

With the exception of having two less pins (Bit 10 true and complement outputs), the CAV-0920 is pin-for-pin compatible with the MOD-1020.

Hybrid microcircuits, ICs, and discrete components are combined in the design, to obtain the maximum benefits of all technologies. The CAV-0920 is factory repairable and backed by Analog Devices' limited one-year warranty.



Differential Phase – Model CAV-0920 A/D and Deglitched HDS-1015E D/A in Back-to-Back Arrangement; 15MHz Word Rate



Differential Gain – Model CAV-0920 A/D and Deglitched HDS-1015E D/A in Back-to-Back Arrangement; 15MHz Word Rate

The waveforms above were obtained using a Tektronix Model 149A N.T.S.C. Test Signal Generator with a 20-IRE TV test signal output. The display (output) was obtained using a Tektronix Model 520A Vectorscope.

## **SPECIFICATIONS** (typical at + 25°C with nominal power supplies unless otherwise noted)

---

Model	Units .	CAV-0920		
RESOLUTION (FS = Full Scale)	Bits (% FS)	9(0.2)		
LSBWEIGHT	mV	2 or 4 (Depending on Input)		
ACCURACY				
(Including Linearity) (a de	$\%$ FS $\pm 1/2$ LSB	0.1		
Monotonicity		Guaranteed 0 to + 70°	C	
Nonlinearity vs. Temperature	% of FS/°C	0.001		
Bubbe with out a backgroup of	% 01 F3/ C	0.02		
DYNAMIC CHARACTERISTICS	JD L J Tel			
AC Linearity (dc to IMHz) (1MHz to 5MHz)	dB below FS.	50		
(5MHz to 10MHz)		45		
Conversion Time <sup>2</sup>	ns (max)	$180(\pm 20)$		
Conversion Rate <sup>3</sup>	MHz	20		
Aperture Uncertainty (Jitter)	ps, rms	± 25		
Aperture Time (Delay) Signal to Noise Pation	ns Jp	10		
Signal to Noise Ratio <sup>5</sup>	dB dB	52		
Noise Power Ratio <sup>6</sup>	dB	41		
Transient Response <sup>7</sup>	ns .	50		
Overvoltage Recovery <sup>8</sup>	ns	50		
Input Bandwidth				
Small Signal, 3dB <sup>9</sup>	MHz, min	30		
Large Signal, 3dB <sup>10</sup>	MHz, min	15		
(60kHz: 62kHz)	dB below FS	55		
(4.998MHz; 5.000MHz)	dB below FS	50		
(9.996MHz; 9.998MHz)	dB below FS, min	45		
Differential Gain <sup>11,12</sup>	%	2 '		
Differential Phase <sup>11,12</sup>	Degree	1		
ANALOG INPUT				
Voltage Range	v	1 p-p or 2 p-p, Depend	ling on Jumper Option	
Input Type	v, max	±4 Uninglan on Binglan		
Impedance	Ohms	500 or 1000 Dependi	ng on Jumper Ontion	
Offset	ennis	Adjustable to Zero W	ith On-Board Potentiometer	
Offset vs. Temperature	% of FS/°C	0.01		
ENCODE COMMAND INPUT				
Logic Levels, ECL-Compatible	v	"0" = -1.7		
(Balanced Input)		"1" = -0.9		
Impedance	Ohms, max	100 Line-to-Line		
Min	<b>n</b> c	10		•
Max	70% Encode Command	Period		
Frequency	MHz	20		
(Calibration Frequency is Customer-Spe	cified; See Ordering Infor	mation.)		
DIGITAL OUTPUT				
Format	Bits	9 Parallel; NRZ		
Logic Levels, ECL-Compatible	v	0'' = -1.7		
(Balanced Output)		"1" = -0.9		
Drive Time Skow	Onms, min	/5, Line-To-Line		
Coding	115, 111ax	Binary (BIN): 2's Con	nplement (2SC)	
DATARFADYOUTPUT				
Logic Levels, ECL-Compatible	v	"0" = $-1.7$		
(Balanced Output)		"1" = -0.9	NOTES	
Drive	Ohms, min	75, Line-to-Line	1AC Linearity expressed in 1	erms of spurious in-band signals generated at
Rise and Fall Time	ns, max	5	20MHz encode rate at anale	og input frequencies shown in ( ).
Duration	ns(max)	25(±5)	Ready; use trailing edge to	strobe output data into external circuits.
POWER REQUREMENTS <sup>14</sup>			<sup>3</sup> To be specified by custome	r. See Ordering Information
$+15V \pm 5\%$	mA(max)	198 (205)	<sup>5</sup> Peak-to-peak signal to rms	o with 500kHz analog input.
$-130 \pm 5\%$ + 5V + 5%	mA (max)	260 (265)	<sup>6</sup> DC to 8.2MHz white noise	bandwidth with slot frequency of 1.248MHz;
$-5.2V \pm 5\%$	A (max)	1.8(1.9)	and encode rate of 20MHz.	hit accuracy attained in anasified time
Power Consumption	W(max)	16.7 (17.4)	*Recovers to 9-bit accuracy i	n specified time after $2 \times FS$ input
TEMPERATURE RANGE			overvoltage.	
Operating	°C	0 to + 70	With analog input 40dB bel <sup>10</sup> With FS analog input: large	ow FS. -signal bandwidth flat within 0.2dB. do
Storage	°C	- 55 to + 85	to 10MHz.	i i i i i i i i i i i i i i i i i i i
Cooling Air Requirements	LFPM	500	"Applies to units optimized I Information	or video applications. See Ordering
(Linear Feet Per Minute)			<sup>12</sup> Measured with 20-IRE Unit	Reference, modulated ramp.
MEAN TIME BETWEEN FAILURES <sup>15</sup>			<sup>13</sup> Transition from digitial "0"	to "1" initiates encoding.
(MTBF)	Hours	$7.5 \times 10^4$	and track over temperature.	qual and opposite within 200mV
			1525°Ambient.	

Specifications subject to change without notice.

#### VOL. II, 11-40 ANALOG-TO-DIGITAL CONVERTERS
### **Physical Characteristics**



CAV-0920 Block Diagram

**OUTLINE DIMENSIONS** 







#### PIN FUNCTION GROUND 1 ENCODE COMMAND ENCODE COMMAND 2 3 4 GROUND 5 - 5.2V + 15V 6 - 15V GROUND 7 8 9 ANALOG INPUT #1 10 ANALOG INPUT #2 11 +5V 12 GROUND 13 GROUND 16 BIT 9 BIT 9 17 18 BIT 8 19 BIT 8 BIT 7 20 BIT 21 BIT 6 22 23 BIT 6 24 BIT 5 25 BIT 5 BIT 4 26 27 BIT 4 BIT 3 28 29 BIT 3 BIT 30 31 BIT 2 32 BIT 1 33 BIT 1 DATA READY 34 35 GROUND DATA READY 36

ALL GROUNDS ARE CONNECTED TOGETHER INTERNALLY

#### **CAV-0920 ANALOG INPUT RANGE OPTIONS**

For 1V p-p input range, connect analog input to pin 10, and connect pins 9 and 10 together. Unterminated input impedance is 500 ohms. For 2V p-p input range, connect analog input to pin 10; pin 9 is left disconnected. Unterminated input impedance is 1,000 ohms.

To obtain the desired terminated input impedance, connect the appropriate external terminating resistor between the analog input pin(s) and ground as shown in the examples. Input impedances greater than 1,000 ohms will result in loss of input bandwidth and should be avoided.

The OFFSET potentiometer (R7) has sufficient range to allow the user to operate the A/D in either the unipolar or bipolar mode.



1V p-p Input Option





2Vp-pInputOption



#### OFFSET AND GAIN ADJUSTMENT

When adjusting the offset and gain of the A/D in the system, the OFFSET control (R7) is adjusted first. The CAV-0920 can be operated in either a unipolar or bipolar mode. For a standard binary output, adjustments for each mode are:

#### Bipolar

- 1. Apply 0V to analog input.
- Adjust R7 OFFSET control while observing MSB (Bit 1). Adjust until digital output has MSB "toggling" between "0" and "1".

- 3. Apply desired maximum positive voltage to analog input.
- Adjust R15 GAIN control while observing LSB (Bit 9). Adjust until digital output has Bits 1-8 solid "1" with LSB "toggling."

#### **Unipolar Positive**

- 1. Apply 0V to analog input.
- Adjust R7 OFFSET control while observing LSB (Bit 9). Adjust until digital output has Bits 1-8 solid "0" with LSB "toggling".
- 3. Apply desired maximum positive voltage to analog input.
- Adjust R15 GAIN control while observing LSB (Bit 9). Adjust until digital output has Bits 1-8 solid "1" with LSB "toggling".



Part of CAV-0920

#### **ORDERING INFORMATION**

The encode (word) rate of the CAV-0920 A/D converter is specified by the customer, as outlined below.

Order by model number CAV-0920-XXX; in this model number, XXX is specified by the customer to indicate the desired word rate in MHz. The decimal place is assumed (but not shown) between the second and third places. CAV-0920-160, for example, indicates calibration at 16.0MHz.

The CAV-0920 will maintain 9-bit accuracy within  $\pm 12\%$  of this specified word rate when the requested word rate is higher than 10MHz. In the example for a 16MHz word rate cited above, the CAV-0920 could be operated at 4 X burst frequency in either NTSC (3.58MHz) or PAL (4.43MHz) systems without readjustment.

For encode rates below 10MHz, the CAV-0920-100 maintains full accuracy through 10MHz.

If later applications of the converter require word rates outside the limits of the original calibration, the unit can be returned to the factory for calibration at the new frequency; there is a nominal charge for this service.

Mating sockets for the CAV-0920 are model number MSB-2 (thru hole) MSB-3 (closed end). These are individual solder-type pin sockets for mounting in PC boards; one is required for each of the 34 pins of the converter.



### 10-Bit Video Analog-to-Digital Converter

**CAV-1040** 

#### PRELIMINARY TECHNICAL DATA

FEATURES 10-Bit Resolution 40MHz Word Rate Single 35-In<sup>2</sup> PC Board ECL Compatible No External Circuits Required

APPLICATIONS Radar Digitizing Medical Instrumentation Digital Communications Spectrum Analysis

#### GENERAL DESCRIPTION

The Analog Devices model CAV-1040 A/D converter is a "system solution" which combines 10-bit resolution, 40MHz word rates, and small size to solve high-speed digitizing problems. Its design is based on proven concepts introduced in the MOD-1020 and MOD-1205 A/D converters and takes advantage of recent technology to achieve exceptional cost/performance tradeoffs.

It is pin-for-pin compatible with the industry's first 10-bit, 20MHz A/D, the MOD-1020. But it *doubles* the word rate of its predecessor, making it possible for system designers to upgrade their systems without new layouts.

This remarkable converter is a complete answer to the question of digitizing radar, video, and/or other high-frequency inputs; it includes a track-and-hold, along with encoding and timing circuits. The CAV-1040 is an ideal choice for the designer who needs state-of-the-art performance in high-resolution, ultra-high-speed A/D conversion.

All inputs and outputs are ECL compatible. Analog input impedance is  $500\Omega$  on 1V range;  $250\Omega$  on 2V range. The A/D requires only an encode command and external power supplies for operation.

Hybrid microcircuits, IC's, and discrete components are combined to obtain the maximum benefits of all technologies. The CAV-1040 is factory repairable and backed by Analog Devices' limited oneyear warranty.



CAV-1040 Block Diagram

### SPECIFICATIONS (unical at + 250° with partial names supplies unless otherwise poted)

		with noninial power sup		
Model	Units	CAV-1040	OUTLINE DIMENSIONS	
RESOLUTION (FS = Full Scale)	Bits %FS	10 0.1	Dimensions shown in inches and (mm).	
LSBWEIGHT		<b>,</b>	1	0.3 ± 0.02
IV p-pFS 2V p-pFS	mV	2	MAX COMPONENT AREA	
ACCURACY			• • • • • • • • • • • • • • • • • • •	U
(Including Linearity)@dc	% FS ± 1/2LSB	0.05	0.2 (5.06) - 3.3 (63.6) - 2 (5.06) - 0.2 (5.02)	
Monotonicity		Guaranteed 0 to +70°C		मन
DYNAMIC CHARACTERISTICS				330
In-Band Harmonics <sup>1</sup>				⊞ III
(dcto1MHz)	dB below FS	60 55		
(IMHZ to SMHZ) (SMHz to 20MHz)	dB below FS	50		
Conversion Time <sup>2</sup>	ns	90 + 1 clock period	<b>₽</b> <u></u>	
Conversion Rate	MHz, max	40		
Aperture Uncertainty (Jitter)	ps, max	± 25		ŦŦ
Signal to Noise Ratio (SNR) <sup>3</sup>	dB, min	50 50(48)		╪╡╞╟
Input Bandwidth	and (tunn)	50(48)	<mark>┥┥┝┝┝┝┝┝┝┝┝</mark> ┝┝┝┥┥┥┥┥┥┥┥┥┥┥┥┥┥┥┥┥	#1
Small Signal, 3dB <sup>5</sup>	MHz	30		<b>#</b>
Large Signal, 3dB <sup>6</sup>	MHz	15		
ANALOGINPUT		•		찌륵
Voltage Range				0.11
Input Pins 9 & 10 Connected	V, p-p FS	1	TO HOLE CENTERLINES	0.23
Input Pin 9 or 10	V, p-pFS	2 + 4		(5.64)
Input Type	Either Unipolar or H	Bipolar		
Impedance			DIN DESIGNATIONS	
1V Input Range	Ω	250	PIN DESIGNATIONS	
2V Input Range	Ω	500		
Uliset	Adjustable to Zero v	0 025	1 GROUND 19 BIT B	
V3. Temperature	//0115/ C	0.025	2 ENCODE COMMAND 20 BIT 7	
Logic Levels ECL Compatible	v	"0" = <u>1</u> 7	4 GROUND 22 BIT 6	
(Balanced Input)	v	"1" = -0.9	5 -5.2V 23 BIT 6	4
Impedance(Line-to-Line)	$\Omega, \max$	100	6 +15V 24 Bit 5 7 -15V 25 Bit 5	
Rise and Fall Times	ns, maz	5	8 GROUND 26 BIT 4	
Width		10	9 ANALOG INPUT #1 27 BIT 4 10 ANALOG INPUT #2 28 BIT 3	
Mar Mar	70% of Encode Corr	mand Period	11 +5V 29 BIT 3	
Frequency	MHz	. 40	13 GROUND 31 BIT 2	
DIGITAL OUTPUT			- 14 BIT 10 32 BIT 1	
Format	Bits	10 Parallel; NRZ	16 BIT 9 34 DATA READY	
Logic Levels, ECL-Compatible	v	"0" <b>=</b> −1.7	17 BIT 9 35 GROUND	
(Balanced Output)	V .	"1" = -0.9	18 BIT 6 JOATA READT	
Drive (Line-to-Line)	· 11, min	/5	ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN TH	E ADC.
Coding	113, 11114	Binary (BIN);		
		2's Complement (2SC)		
DATA READY OUTPUT			•	
Logic Levels, ECL-Compatible	v	"0" = -1.7		
(Balanced Output)	V	"1" = -0.9		
Drive (Line-to-Line)	Ω, min	75		
Rise and Fall Time	ns, max	$\frac{5}{20(+5)}$		
DURANCIA DOWNED REQUIDEMENTS			•	
$+15V \pm 5\%$	mA(max)	390 (425)	NOTES	
- 15V ± 5%	mA (max)	175 (200)	<sup>1</sup> In-Band Harmonics expressed in terms of sourious in-hand	
+5V ±5%	mA (max)	20(25)	signals generated at 40MHz encode rate at analog inputs	
$-5.2V \pm 5\%$	A (max)	2.5 (2.8)	shown in ( ). <sup>2</sup> Meanward from leading adap Encode Command to trailing adapt Date	
Power Consumption	W (max)	Z1(24)	<ul> <li>Ready; use trailing edge to strobe cutput data into external circuits.</li> </ul>	
TEMPERATURE RANGE		0	<sup>3</sup> RMS signal to rms noise ratio with 500kHz analog input.	
Operating	τυ •C	0 to + 70	LOL to 8.2MHz white noise bandwidth with slot frequency of 3.886M and encode rate of 40MHz.	lHz;
Cooling Air Requirements	LFPM	500 + 85	With analog input 40dB below FS.	
comptain and moments	(Linear Feet Per M	inute)	With FS analog input. (Large-signal bandwidth flat within 0.2dB, dc	:
CONSTRUCTION			<ul> <li>to smitz).</li> <li><sup>7</sup>Transition from digital "0" to digital "1" initiates encoding</li> </ul>	
Single Printed Circuit Card	Inches	7.0×5.0×0.5	Specifications subject to change without notice	



### 12-Bit Video Analog-to-Digital Converter

### CAV-1210

#### FEATURES 12-Bit Resolution 10MHz Word Rate Single 35-In<sup>2</sup> PC Board ECL Compatible No External Circuits Required

APPLICATIONS Radar Digitizing Medical Instrumentation Digital Communications Spectrum Analysis



#### **GENERAL DESCRIPTION**

The Analog Devices model CAV-1210 A/D converter combines performance, size, and economy to achieve a remarkable solution for high-speed digitizing problems.

The unit is capable of 12 bits of resolution at word rates through 10MHz. It is a complete answer to the question of digitizing radar, video, and/or other high-frequency inputs; it includes a track-and-hold, along with encoding and timing circuits. The CAV-1210 is a "system solution" for the designer who wants to avoid the need for combining the plethora of components necessary to make IC encoders operate as functional A/D converters.

The unit uses the unique digital correcting subranging (DCS) conversion technique, pioneered by Analog Devices, which virtually eliminates the errors normally associated with subranging A/D converters.

The CAV-1210 is constructed on a single PC board intended for mounting on a "mother" board in the user's system. Its small size makes it adaptable to a wide range of mother board sizes and allows room for including other (signal conditioning, processing, memory, etc.) circuits adjacent to the converter.

All inputs and outputs are ECL compatible; analog input impedance is 1000 ohms. The A/D requires only an encode command and external power supplies for operation.

Hybrid microcircuits, ICs and discrete components are combined in the design, to obtain the maximum benefits of all technologies. The CAV-1210 is repairable and backed by Analog Devices' limited one-year warranty.

**OUTLINE DIMENSIONS** 

Dimensions shown in inches and (mm).



### **SPECIFICATIONS**

(typical at  $+25^{\circ}$ C with nominal power supplies unless otherwise noted)

Model	Units	CAV-1210
RESOLUTION (FS = Full Scale)	Bits (% FS)	12(0.024)
LSB WEIGHT	mV	0.5
ACCURACY		
(Including Linearity)@ dc	$\%$ FS $\pm 1/2$ LSB	0.0125
Monotonicity		Guaranteed 0 to + 70°C
Nonlinearity vs. Temperature	% of FS/°C	0.000125
Gain vs. Temperature	% of FS/°C	0.005
DYNAMIC CHARACTERISTICS		-
AC Linearity' (dc to IMHz)	dB below FS	/0
(IMHZ to SMHZ) Conversion Time <sup>2</sup>	ns(max)	225(+20)
Conversion Rate <sup>3</sup>	MHz	10
Aperture Uncertainty (Jitter)	ps	±25
Aperture Time (Delay)	ns	6
Signal to Neise Ratio (SNR) <sup>4</sup>	dB	62
Signal to Noise Ratio (SNR) <sup>3</sup>	dB dB (m/m)	71
Noise Power Ratio (NPR) <sup>5</sup>	ab (min)	55(52) 100
Overvoltage Recoverv <sup>8</sup>	ns. max	200
Input Bandwidth		
Small Signal, 3dB <sup>9</sup>	MHz	35 .
Large Signal, 3dB <sup>10</sup>	MHz	30
Two-Tone Linearity (@ Input Frequencies)		
(60kHz; 62kHz)	dB below FS, min	/0
(2.498MHZ; 2.500MHZ) (4.996MH2: 4.998MH2)	dB below FS, min	60
	ub ociow i oynini	
ANALUG INPU I Voltage Pange	VFS	+1
(+1V  input = all "1s"; -1V  input = all "0s")	V, TS V. max	±2
Input Type	.,	Bipolar
Impedance	Ohms	1000
Offset		
Initial (Set at Factory)	mV, max	±1
vs. Temperature	% of FS/°C	0.02
ENCODE COMMAND INPUT <sup>11</sup>		"o" 17
(Palanand Innut)	v	"0" = -1.7 "1"0.9
Impedance	Ohms, max	100 Line-to-Line
Width	••••••	
Min	ns	10
Max	70% of Encode Comman	d Period
Frequency	MHz	10
(Calibration Frequency is Customer-Spec	itied; See Ordering Inforn	nation.)
DIGITAL OUTPUT		
Format	Bits	12 Parallel; NRZ
(Palanand Output)	v	$0^{\circ} = -1.7$
(Balanced Output)	Ohms, min	75. Line-To-Line
TimeSkew	ns, max	5
Coding		Offset Binary (OBN);
		2's Complement (2SC)
DATA READY OUTPUT		
Logic Levels, ECL-Compatible	v	"0" = -1.7
(Balanced Output)	·	"1" = -0.9
Drive Biss and E-UTime	Ohms, min	75, Line-to-Line
Duration	ns(max)	25(+5)
	10 (max)	
+15V + 5%	mA (max)	185 (205)
$-15V \pm 5\%$	mA (max)	240(265)
$+5V \pm 5\%$	mA (max)	120(135)
$-5.2V \pm 5\%$	A (max)	2.1(2.3)
Power Consumption	W(max)	18(19.7)
TEMPERATURE RANGE		
Operating <sup>13</sup>	°C	0 to + 70
Storage	°C	- 55 to + 85
Cooling Air Requirements	LFPM	500
(Linear Feet Fer Minute)	1_11111	·····
MEAN TIME BETWEEN FAILURES <sup>14</sup>		
(MTBF)	Hours	$1.06 \times 10^{\circ}$

#### NOTES 1AC Linearity expressed in terms of spurious in-band signals generated at 10MHz encode rate at analog input frequencies shown in (). <sup>3</sup>Measured from leading edge Encode Command to trailing edge Data Ready, use' trailing edge to strobe output data into external circuits. <sup>3</sup>To be specified by customers. See Ordering Information. <sup>4</sup>Rms signal to rms noise ratio with 500kHz analog input. <sup>4</sup>Peak-to-peak signal to rms noise ratio with 500kHz analog input. <sup>4</sup>Peak-to-peak signal to rms noise ratio with 500kHz analog input. <sup>4</sup>Peak-to-peak signal to rms noise ratio with 500kHz analog input. <sup>4</sup>Peak-to-peak signal to rms noise ratio with 500kHz analog input. <sup>4</sup>Peak-to-peak signal to rms noise ratio with 500kHz analog input. <sup>4</sup>Peak-to-peak signal to rms noise ratio with 500kHz analog input. <sup>4</sup>Peak-to-peak signal to rms noise ratio with 500kHz analog input. <sup>4</sup>Peak-to-peak as the peak signal to rms noise ratio with 500kHz analog input 40dB below FS. <sup>4</sup>With FS analog input (Large-signal bandwidth flat within 0.2dB, dc to 5MHz. <sup>11</sup>Transition from digital "0" to digital "1" initiates encoding. <sup>12</sup>±15V must be equal and opposite within 200mV and track over temperature. <sup>13</sup>Some spec degradation may occur outside a "window" of 50° centered at +25°C. <sup>14</sup>25'Ambient.

Specifications subject to change without notice.



CAV-1210 Block Diagram

#### THEORY OF OPERATION

Refer to the block diagram of the CAV-1210.

The analog input signal to be digitized is applied first to a trackand-hold (T/H) amplifier, which is normally operated in the "track" mode, following all changes in analog input as they occur. The user of the CAV-1210 determines the point at which the analog signal is to be digitized by applying an Encode Command.

The leading edge of the encode command causes the track-and-hold circuit to switch momentarily to the "hold" mode of operation, "freezing" the analog input long enough to begin the digitizing process. The "held" value of the analog signal is applied to a 6bit A/D encoder, and (through a buffer amplifier) to an analog delay circuit whose delay is equal to the time required for the first digitizing/reconstruction step of the encoding process.

The analog output of the T/H is now digitized and resolved to 6-bit accuracy and applied through registers to a 6-bit D/A converter, which has 12-bit accuracy. Via a second set of registers, the same 6-bit digitized signal is applied to the digital correction logic circuits. The value stored in the second bank of registers will ultimately represent Bits 1-6 of the final digital output of the CAV-1210.

The digitized signal applied to the fast-settling D/A converter is reconverted to an inverted analog signal and is applied with the delayed analog input to a wideband, fast-settling operational amplifier. The op amp output represents the residue signal which remains after a 6-bit representation of the analog input has been subtracted from that input.

This residue, or error, signal is digitized by a second encoder to a resolution of 7 bits and applied to the digital correction logic circuits along with Bits 1-6.

The correction circuits use a combination of the 6-bit and 7-bit signals to compensate for possible nonlinearities and other errors to assure the final 12-bit digital output will be 12-bit accurate.

Oversimplified, the digital correction circuits use the information contained in the 7-bit signal to determine whether or not Bits 1-6 need to be modified.

Basically, the correction circuits use the information contained in the MSB of the 7-bit byte to determine what action needs to be taken with regard to the first six bits. Depending upon its value, the circuits will pass the 6-bit information as it is, or add a value of binary "1" to it. Bits 2-7 of the 7-bit information become Bits 7-12 of the digital output of the CAV-1210.

This unique use of 13 bits to achieve an accurate 12 bits of resolution compensates for a multitude of potential errors which otherwise could be eliminated only by incorporating expensive, high precision parts into the design. Digitally corrected subranging (DCS) used in the CAV-1210 does not prevent such anomalies as gain error, track/hold droop error, linearity error, or offset error. But it obviates the effects of these problems and makes high-speed, high resolution digitizing an economic reality.

#### ANALOG-TO-DIGITAL CONVERTERS VOL. II, 11–47

#### ORDERING INFORMATION

The CAV-1210 A/D converter will meet all specifications shown in the Specifications table of the data sheet at encode (word) rates through 10MHz.

For standard CAV-1210 units intended to operate with specified performance over the full range through 10MHz, order model number CAV-1210-100.

If desired, the customer can order the unit calibrated at the factory for optimum performance at some specified rate within this range for those applications in which the unit will generally be operated at the same word rate.

Order by model number CAV-1210-XXX; in this model number, XXX is specified by the customer to indicate the desired optimized word rate. The decimal place is assumed (but not shown) between the second and third places. CAV-1210-050, for example, indicates final calibration and, consequently, optimum performance at 5.0MHz; but the unit will operate through 10MHz.

Optimum performance will be achieved within a  $\pm 12\%$  band of frequencies around the selected word rate, but the user must keep in mind the upper performance specification of 10MHz. "Optimum" final calibration at 9.8MHz, for example, is not meant to imply optimum performance at word rates above 10MHz. The unit will operate beyond 10MHz, but accuracy, NPR, SNR, and/or other specifications may be outside the limits shown on Specifications page.

If later applications require word rates outside the limits of the original optimum frequency, the unit can be returned to the factory for calibration at a new optimum; there is a nominal charge for this service.

Mating sockets for the CAV-1210 are model number MSB-2 (thru hole) or MSB-3 (closed end). These are individual solder-type pin sockets for mounting in PC boards; one is required for each of the 40 pins of the converter.

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	21	BIT 9
2	<b>ENCODE COMMAND</b>	22	BIT 8
3	<b>ENCODE COMMAND</b>	23	BIT 8
4	GROUND	24	BIT 7
5	5.2V	25	BIT 7
6	+ 15V	26	BIT 6
7	– 15V	27	BIT 6
8	GROUND	28	BIT 5
9	ANALOG INPUT	29	BIT 5
10	GROUND	30	BIT 4
11	+5V	31	BIT 4
12	GROUND	32	BIT 3
13	GROUND	33	BIT 3
14	BIT 12 (LSB)	34	BIT 2
15	BIT 12 (LSB)	35	BIT 2
16	BIT 11	36	BIT 1 (MSB)
17	BIT 11	37	BIT 1 (MSB)
18	BIT 10	38	DATA READY
19	BIT 10	39	GROUND
20	BIT 9	40	DATA READY

#### CAV-1210 Pin Designations

# 

### Ultra High Speed 8- and 10-Bit A/D Converters

### MAH-0801, -1001

#### **FEATURES**

High Speed at Low Cost 8-Bits @ 750ns max 10-Bits @ 1µs max Monotonic Over Temperature Differential Nonlinearity ±1/4LSB typ Parallel and Serial Outputs Pin and Function Compatible with 4130, 4131 APPLICATIONS High Speed Data Acquisition Real Time Waveform Analysis Radar Signal Processing Analytical Instruments

#### **GENERAL DESCRIPTION**

The MAH series of high-speed analog-to-digital converters represent the latest "state-of-the-art" in high speed successive approximation technology. They are the fastest and most accurate complete converters of their type, featuring internal reference, clock, timing, encoding, and control logic functions. The MAH series A/Ds should be considered in applications where completeness of design function, ease of interface, and speed are required. These modules make maximum use of the latest monolithic and hybrid parts to minimize total parts complexity and increase reliability. They are designed to be form, fit, and function compatible with the T.P. 4130 and 4131, with advantages over the latter in overall accuracy without any sacrifice in speed.

In almost all applications, these A/Ds require the use of fast sample-and-hold. Depending upon the application, either the ADI THC or THS series of ultra-fast sample-and-holds are recommended.



MAH-0801 and MAH-1001 Block Diagram





DOT ON TOP INDICATES POSITION OF PIN 1

### SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	UNITS	MAH-0801	MAH-1001
RESOLUTION FS @ Full Scale	Bits	8	10
ACCURACY (Relative to Full Scale)	±% FS	0,2	0.05
Quantization Error	LSB	±1/2	*
Nonlinearity	LSB (max)	±1/4	±1/2
Differential Nonlinearity	LSB (max)	±1/4	±1/2
	LSB (typ)	±1/8	±1/4
Missing Codes		No Missing Codes 0	to +70°C
Monotonicity		Monotonic U to +/U	
TEMPERATURE COEFFICIENTS	0 -	1. State 1.	
Differential Nonlinearity	±ppm/°C	3	
Gain	±ppm/°C	20	
Zero Offset (Unipolar)	$\pm \mu V / C$	10	
Zero Offset (Bipolar)	±ppm/ C	15	-
INPUT		· · · ·	
Ranges (Full Scale)		`	• ·
MAH-XXXX-1	V	0 to -5	:
MAH-XXXX-2	v	0 to -10	
	V	I) +10	•
MAH-XXXX-4 MAU XXXX 6	V.	±10 +1.024	•
Impedance (Function of Option)	ν Ω/V	100	•
	V	To Twice Peak Inp	ut ES Without Damage.
		10 1 wild 1 cak inp	1000
CONVERSION TIME	ns max	750	950
<u> </u>	nstyp	700	<i>730</i>
ENCODE COMMAND			
Logic Levels (1 Standard TTL Load)	v	" $0$ " = 0 to +0.4, "1" = +2 to +5.5	
Function		Positive-going edge	resets converter.
		Trailing edge starts	conversion.
Duration (Width)	ns min (max)	50 (150)	
Rise and Fall Limes	ns max	20	•
Repetition Rate	KHZ MAX	1333	1000
LOGIC OUTPUTS			
Levels TTL (Same as Encode Command)			
Drive Capability		Data and Data Rea	dy-10 Std TTL Loads,
Parallel Data		Clock-IU IIL Los	ids hold workil second of
Faranei Data		s or To lines of dat	a neid until start of
Coding (Unipolar)		CBN	*
(Binolar)		COB/C2SC	
Serial Data		MSB first successiv	e pulse output during
		conversion, NRZ.	e pane catpat annig
Coding		Same as parallel ou	put except 2SC not
		available.	1 1
Clock		Pulse train of 9 or 1	1 internal clock pulses,
		gated on during the	conversion period.
POWER REQUIREMENTS			
+14.5V to +15.5V	mA max	50	. •
-14.5V to -15.5V	mA max	30	•
+5V ±5%	mA max	250	•
TEMPERATURE RANGE			
Operating	°c	0 to +70	•
Storage	°č	-55 to +85	
Case		Dially! Phthalate ne	r MIL-M-14 Type SDG-F
		Dianyi i nuiaiate pe	a mining type obd-r

NOTES <sup>1</sup> Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.

Specifications subject to change without notice.

#### **OUTPUT CODING**

The logic output coding is shown true relative to the analog input to the A/D. If an inverting track and hold—such as the Analog Devices THC series—or an inverting op amp is used alread of the A/D, the true logic coding is inverted relative to the system input. This yields the systemic coding as follows:

Scale	Input Voltage	Complementary Straight Binary
-FS -1LSB	-9.9900V	1111 1111 11
-3/4 FS	-7.5000V	1100 0000 00
-1/2 FS	-5.0000V	1000 0000 00
-1/4 FS	-2.5000V	0100 0000 00
-1LSB	-0.0010V	0000 0000 01
0	0.0000V	0000 0000 00

NOTE

(0 to -10V) for MAH-1001-2; LSB = 10mV for MAH-1001-1, apply input voltage factor of 1/2.

Table I. MAH-0801 and MAH-1001 Unipolar Operation for Options 1 and 2 Binary (BIN) in place of Complementary Binary (CBN) for options 1 and 2; Offset Binary (OBN) in place of Complementary Offset Binary (COB) for options 3, 4 and 5; Two's Complement (2SC) in place of Complementary Two's Complement (C2SC).

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-4.9900V	1111 1111 11	0111 1111 11
-3/4 FS	-3.7500V	1110 0000 00	0110 0000 00
-1/2 FS	-2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
+1/2 FS	+2.5000V	0100 0000 00	1100 0000 00
+3/4 FS	+3.7500V	0010 0000 00	1010 0000 00
+FS -1LSB	+4.9900V	0000 0000 01	1000 0000 01
+FS	+5.0000V	0000 0000 00	1000 0000 00

NOTE

(-5V to +5V) for MAH-1001-3; LSB = 10mV for MAH-1001-4 apply input voltage factor of 2.

Table II. MAH-0801 and MAH-1001 Bipolar Operation for Options 3 and 4

Scale	Input	Complementary Con	mplementary
	Voltage	Offset Binary Two	's Complement
-FS -1LSB	-1.022V		
0	-0.000V	1000 0000 00 00	00 0000 00
+1/2 FS	+0.512V	0100 0000 00 11	00 0000 00
+FS	+1.024V	0000 0000 00 10	00 0000 00

NOTE

(-1.024V to +1.024V) for MAH-1001-5; LSB = 2mV.

Table III. MAH-0801 and MAH-1001 Bipolar Operation for Option 5

#### CALIBRATION AND ADJUSTMENT





PROCEDURE:

- 1. APPLY ENCODE COMMAND PULSE TO THE ENCODE COMMAND INPUT (PIN 3).
- 2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE FOR +1/2LSB. VARY THE ZERO ADJUST POTENTIOMETER FOR AN LSB FLUTTER (THIS WILL APPEAR AS AN EQUAL UNCERTAINTY AT THE OUTPUT BETWEEN THE CODES 0000 .... 0000 AND 0000 .... 0001).
- 3. WITH THE PRECISION VOLTAGE SOURCE ADJUSTED TO -FS +1/2LSB, ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN CODES 1111 .... 1110 AND 1111 .... 1111.

#### Unipolar Operation

- PROCEDURE: 1. APPLY AN ENCODE COMMAND TO THE ENCODE COM-MAND INPUT (PIN 3).
- CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE TO +FS -1/2LSB. THE ZERO ADJUST POTENTIOMETER FOR A FLUTTER BETWEEN VARY CODES 0000 .... 0000 AND 0000 .... 0001.
- 3. ADJUST THE VOLTAGE SOURCE TO -FS +1/2LSB. AD-JUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN THE CODES 1111 .... 1110 AND 1111 .... 1111.

**Bipolar Operation** 

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#### TIMING DIAGRAM



Figure 2. MAH-0801 and MAH-1001 Timing Diagram

#### APPLICATIONS



Figure 3. Depicts a Complete 8-Bit, 1MHz Conversion System Using the THS-0060 Track-and-Hold and the MAH-0801-5 Low-Voltage Input A/D Converter

#### NOTES ON USAGE

The use of a large ground plane is highly recommended. Tie all grounds for both the ADC and T&H together. Make the distance from the ADC to the system ground as short as possible with as low an impedance as possible. Bypass each power supply run with a ceramic  $(0.1\mu F)$  and tantalum  $(3.3\mu F)$  capacitor. Keep the analog input as far away from the digital outputs as practical. Avoid the use of twisted pair cables for

> PIN DESIGNATIONS MAH-0801, MAH-1001

PIN	FUNCTION	PIN	FUNCTION
1	DATA READY OUT	15	BIT 9 OUT
2	INTERNAL CLOCK OUT	16	BIT 10 OUT (LSB)
3	ENCODE COMMAND IN	17	BIT 1 OUT (MSB)
4	SERIAL OUTPUT	19	ANALOG INPUT
5	BIT 1 OUT (MSB)	20	ANALOG GROUND
6	BIT 2 OUT	30	GAIN ADJUST
7	BIT 3 OUT	31	GAIN ADJUST
8	BIT 4 OUT	32	OFFSET ADJUST
11	BIT 5 OUT	33	POWER GROUND
12	BIT 6 OUT	34	-15V POWER IN
13	BIT 7 OUT	35	+15V POWER IN
14	BIT 8 OUT	36	+5V POWER IN

NOTES

On Model MAH-0801, Pins 15 and 16 are deleted. Power and Analog grounds are internally connected.



Figure 4. Depicts the MAH-1001-2 A/D Converter Used with the THC-0300 Track-and-Hold

digital outputs wherever possible. The use of coax cable for analog inputs is recommended wherever practical to avoid digital feedback.

#### **ORDERING INFORMATION**

The 8- and 10-bit versions of the MAH series may be ordered with various options according to the chart below.

<u>MAH-0801</u>	<u>-1</u>
RESOLUTION	ANALOG INPUT
AND ACCURACY	RANGE
MAH-0801 = 8 Bits	-1 0 to -5V FS
MAH-1001 = 10 Bits	-2 0 to -10V FS
	-3 ±5V FS
	-4 ±10V FS
	-5 ±1.024V FS

## 

### Ultra High Speed 8-, 10-, and 12-Bit A/D Converters MAS-0801, -1001, -1202

FEATURES

High Speed at Low Cost 8 Bits 1µs max 10 Bits 1.5µs max 12 Bits 2µs max No Missing Codes Over Temperature Low Power Industry Standard Pin Out Parallel and Serial Outputs

APPLICATIONS

High Speed Data Acquisition Real Time Waveform Analysis Radar Signal Processing Analytical Instruments

#### GENERAL DESCRIPTION

The MAS series of high speed analog-to-digital converters represent the "state of the art" in application of the successive approximation conversion technique by providing highest speed at lowest cost. With monotonicity guaranteed over temperature these reliable modules are form, fit and function compatible with popular industry standards from Datel and Philbrick (for new designs consider the HAS series of hybrid converters).

In most applications these A/Ds should be used with a fast sample hold such as the THS/THC series.



MAS-0801 and MAS-1001 Block Diagram





MAS-1202 Block Diagram

### **SPECIFICATIONS** (typical @ +25°C unless otherwise noted)

Model	Units	MAS-0801	MAS-1001	MAS-1202
RESOLUTION FS = Full Scale	Bits	8	10	12
ACCURACY (Relative to Full Scale)	±% FS	0.2	0.05	0.012
Quantization Error	LSB	±1/2	•	•
Nonlinearity	LSB (max)	±1/2	•	•
Differential Nonlinearity	LSB (max)	±1/2	•	•
Missing Codes		No Missing C	odes 0 to +70°C	
TEMPERATURE COEFFICIENTS			•	
Differential Nonlinearity	±ppm/°C	3	*	•
Gain	±ppm/°C	20	•	30
Gain (Option-P)	±ppm/°C	5	•	NA
Zero Offset (Unipolar)	±µV/°C	10	•	100
Zero Offset (Bipolar)	±ppm/°C	15	•	•
Zero Offset (Option-P)	±ppm/°C	5	*	NA
INPUT				
Ranges (Full Scale)	Options MA	S-0801 and MAS	5-1001 ONLY	STANDARD
MAS-XXXX-1	v	0 to -5	•	0 to +10/±5
MAS-XXXX-2	v	0 to -10	+	NA
MAS-XXXX-3	v	±5	•	NA
MAS-XXXX-4	v	±10	•	NA
MAS-XXXX-5	v	±1.024	<b>`</b> •	NA
Impedance (Function of Option)	$\Omega/V$	100	•	1150Ω
OVERVOLTAGE	v	To Twice Peak	Input FS Withou	t Damage.
CONVERSION TIME <sup>1</sup>	lis may	1	15	2
CONVERSION TIME	us typ	0.8	1.3	1.8
ENCODE COMMAND	p	••••		
Logic Levels (1 Standard TTL Load) Function	v	"0" = 0 to +0.4, "1" = +2 to +5.5 Positive-going edge resets converter, Trailing edge starts conversion for 8-		
Duration (Width)	ns min	50	*	100
Rise and Fall Times	ns max	20	•	*
Repetition Rate	kHz max	1000	666	500
LOGIC OUTPUTS Levels TTL (Same as Encode Command) Drive Capability Parallel Data Coding (Unipolar) (Bipolar) Serial Data Coding Clock		Data and Data Clock – 6TTL 8, 10 or 12 lin Encode Comm CBN COB/2SC MSB first, succ conversion, NF Same as paralle available. Pulse train of 9 pulses, gated o period.	Ready – 4 Std T Loads es of data held ur and * esssive pulse outp RZ. el output except 2 0, 11 or 13 intern n during the com	TL Loads, htil next BIN OBN/2SC ut during 2SC not al clock version
POWER REQUIREMENTS				
+14.5V to +15.5V	mA	70	•	80
-14.5V to -15.5V	mA	30	•	20
+5V ±5%	mA	150	•	•
TEMPERATURE RANGE				
Operating	°c	0 to +70	. •	•
Storage	°c	-55 to +85	•	•
PHYSICAL CHARACTERISTICS Case		Diallyl Phthal	ate per MIL-M-14	Type SDC-F

NOTES

<sup>1</sup> Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.

\*Specifications same as MAS-0801.

Specifications subject to change without notice.

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).





#### PIN DESIGNATIONS MAS-0801, MAS-1001

PIN	FUNCTION	PIN	FUNCTION
1	DATA READY OUT	15	BIT 9 OUT
2	INTERNAL CLOCK OUT	16	BIT 10 OUT (LSB)
3	ENCODE COMMAND IN	19	ANALOG INPUT
4	SERIAL OUTPUT	20	ANALOG GROUND
5	BIT 1 OUT (MSB)	30	REFERENCE OUT
6	BIT 2 OUT	31	REFERENCE INPUT
7	BIT 3 OUT	32	OFFSET
8	BIT 4 OUT	33	POWER GROUND
11	BIT 5 OUT	34	-15V POWER IN
12	BIT 6 OUT	35	+15V POWER IN
13	BIT 7 OUT	36	+5V POWER IN
14	BIT 8 OUT		

#### PIN DESIGNATIONS MAS-1202

Γ	PIN	FUNCTION	PIN	FUNCTION	
Γ	1	DATA READY	16	BIT 10 OUT	1
	2	INTERNAL CLOCK OUT	17	BIT 11 OUT	
1	3	BIT 1 OUT (MSB)	18	BIT 12 OUT (LSB)	
L	4	SERIAL DATA OUT	19	ANALOG INPUT	1
	5	BIT 1 OUT (MSB)	20	ANALOG GROUND	
	6	BIT 2 OUT	29	ENCODE COMMAND IN	
I.	7	BIT 3 OUT	30	GAIN ADJUST	
1	8	BIT 4 OUT	31	BIPOLAR OFFSET	
	11	BIT 5 OUT	32	UNIPOLAR ZERO	
	12	BIT 6 OUT	33	POWER GROUND	
Ł	13	BIT 7 OUT	34	-15V POWER IN	
	14	BIT 8 OUT	35	+15V POWER IN	
	15	BIT9OUT	36	+5V POWER IN	1
1			1	1	

#### ORDERING INFORMATION

The 8- and 10-bit versions of the MAS series may be ordered with various options according to the chart below.

MAS-0801	-1	-CBN
	- <u>T-</u> -	
RESOLUTION	ANALOG INPUT	LOGIC OUTPUT
AND ACCURACY	RANGE	CODING
		(See Note 1)
MAS-0801 = 8 Bits	-1 0 to -5V FS	CBN = Complementary
MAS-1001 = 10 Bits	-2 0 to -10V FS	Binary (Options
	-3 ±5V FS	1 and 2)
	-4 ±10V FS	COB = Complementary
	-5 ±1.024V FS	Offset Binary
		(Options 3, 4 and 5)
		C2SC = Complementary
		Two's Comple-
	•	ment (Options
		3, 4 and 5)

#### NOTES

1. For 12-bit performance order the MAS-1202 which has no options.

2. The mating connector for the MAS series is the MSA-1.

#### **OUTPUT CODING**

The logic output coding is shown true relative to the analog input to the A/D. If an inverting track and hold-such as the Analog Devices THC series-or an inverting op amp is used ahead of the A/D, the true logic coding is inverted relative to the system input. This yields the systemic coding as follows:

Scale	Input Voltage	Complementary Straight Binary
-FS -1LSB	-9.9900V	1111 1111 11
-3/4 FS	-7.5000V	1100 0000 00
-1/2 FS	-5.0000V	1000 0000 00
-1/4 FS	-2.5000V	0100 0000 00
-1LSB	-0.0010V	0000 0000 01
0	0.0000V	0000 0000 00

NOTE

(0 to -10V) for MAS-1001-2; LSB = 10mV for MAS-1001-1, apply input voltage factor of 1/2.

Table I. MAS-0801 and MAS-1001 Unipolar Operation for Options 1 and 2

Scale	Input Complementary Comple Voltage Offset Binary Two's C		Complementary Two's Complement
-FS -1LSB	-1.022V	1111 1111 11	0111 1111 11
-1/2 FS	-0.512V	1100 0000 00	0100 0000 00
0	-0.000V	1000 0000 00	0000 0000 00
+1/2 FS	+0.512V	0100 0000 00	1100 0000 00
+FS	+1.024V	0000 0000 00	1000 0000 00

NOTE

(-1.024V to +1.024V) for MAS-1001-5; LSB = 2mV.

Table III. MAS-0801 and MAS-1001 Bipolar Operation for Option 5

Binary (BIN) in place of Complementary Binary (CBN) for options 1 and 2; Offset Binary (OBN) in place of Complementary Offset Binary (COB) for options 3, 4 and 5; Two's Complement (2SC) in place of Complementary Two's Complement (C2SC).

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-4.9900V	1111 1111 11	0111 1111 11
-3/4 FS	-3.7500V	1110 0000 00	0110 0000 00
-1/2 FS	-2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
+1/2 FS	+2.5000V	0100 0000 00	1100 0000 00
+3/4 FS	+3.7500V	0010 0000 00	1010 0000 00
+FS -1LSB	+4.9900V	0000 0000 01	1000 0000 01
+FS	+5.0000V	0000 0000 00	1000 0000 00

NOTES:

(-5V to +5V) for MAS-1001-3; LSB = 10mV for MAS-1001-4 apply input voltage factor of 2.

In Table II, complementary 2SC is accomplished by factory option.

Scale	Input Voltage	Straight Binary
+FS -1LSB	+9.9976V	1111 1111 1111
+7/8 FS	+8.7500V	1110 0000 0000
+3/4 FS	+7.5000V	1100 0000 0000
+1/2 FS	+5.0000V	1000 0000 0000
+1/4 FS	+2.5000V	0100 0000 0000
+1LSB	+0.0024V	0000 0000 0001

0.0000V

Table II.	MAS-0801	and MAS-1001	Bipolar Operation
for Optio	ns 3 and 4		

NOTE

0

Unipolar Operation (0 to +10V)

Table IV. MAS-1202 Unipolar Operation (0 to +10V)

0000 0000 0000

Scale	Input Voltage	Straight Binary	Two's Complement
+FS -1LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
+1/2 FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
-3/4 FS	-3.7500V	0010 0000 0000	1010 0000 0000
-FS +1LSB	-4.9976V	0000 0000 0001	1000 0000 0001
-FS	-5.0000V	0000 0000 0000	1000 0000 0000

NOTE

In Table V, TWO'S COMPLEMENT (2SC) is accomplished by using the MSB output for Bit 1.

Table V. MAS-1202 Bipolar Operation (-5V to +5V)



### 8-Bit Video Analog-to-Digital Converter

### MATV-0811, -0816, -0820

#### FEATURES

8-Bit Accuracy – Guaranteed Monotonic Ultra-High Speed – dc to 20MHz Word Rates Most Economical Video A/D Smallest Available Complete A/D –  $5.5'' \times 4.38'' \times 0.85''$ Self Contained – Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

#### APPLICATIONS

Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies

Video Time Base Correction and Frame Synchronization Radar Signal Processing

**Real Time Transient and Continuous Spectrum Analysis** 

#### **GENERAL DESCRIPTION**

The Analog Devices' MATV series of A/D converters represent a major breakthrough in high-speed A/D technology. Providing conversion word rates from dc to 11MHz, 16MHz and 20MHz the MATV-0811, MATV-0816 and MATV-0820 are the lowest cost A/D converters in their performance class. As complete devices, they require only the addition of external power to accomplish precision video A/D conversion.

The use of internal hybrid microcircuit construction allows these modular A/D's to occupy a volume of only 21 cubic inches. They are housed in metal cases which not only shield the circuits from external RF interference, but aid in efficient heat dissipation. A choice of analog input voltages is available, including the industry standard 0 to +1V at 75 $\Omega$ . The encode command input, data ready output, and the digital bit outputs are all TTL compatible. Designed to operate from either ±12V or ±15V analog and +5V digital supplies (MATV-0811 and MATV-0816 also require -5.2V), the MATV series dissipate less than 8 watts. Their weight is < 10 ounces due to enclosure rather than encapsulation. This technique facilitates rapid, inexpensive factory repair and aids in reliable printed circuit board mounting by the customer without extensive mechanical constraints or system engineering.

Relative dc accuracy is 0.2% of full scale  $\pm 1/2LSB$  when operating over the frequency range of dc to 20MHz. The MATV series is designed to digitize color television signals at rates up to 20MHz and is also ideally suited for other analog to digital conversion requirements, such as radar signal processing, laser pulse analysis, transient analysis, and medical electronics applications where real-time analysis and display of large quantities of information are required.





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MATV-0811, MATV-0816 Block Diagram



MATV-0820 Block Diagram

### SPECIFICATIONS

(typical @ +25°C and nominal power supply voltages unless otherwise noted)

MODEL	UNITS	MATV-0811	MATV-0816	MATV-0820
	B1		•	
LSB Weight	Bits/% FS	8/0.4	•	•
LSB weight	% F3	0.4		·
ACCURACY (relative) at dc	typ	±0.15% ±1/2LSB	•1	•
	max	±0.2% ±1/2LSB	•1	
Monotonicity	·	GUARANTEED		· · · · · · · · · · · · · · · · · · ·
Linearity and Cain vs Temperature	% FS/ C	0.01		0.005
Enterny and Gam vs Temperature	70 F 5/ C	0.02		0.01
DYNAMIC CHARACTERISTICS	·			
AC Linearity @ Encode Rate"	MHz	11	15	20
Analog Input Frequency	Consigna Cionale a			•
DC to 5.0MHz	> dR balow ES	FO 50	•	•
3 6MHz to 5 5MHz	> ub below F5	45	•	•
Conversion Rate (Encode Word Rate)	MHz max	11	16 <sup>1</sup>	20
Conversion Time <sup>3</sup>	ns	150±20	120±20	35 ±10 + l/Encode Rate
Aperture Uncertainty (Jitter)	ps max	±30	•	•
Aperture Time	ns	3	•	12
Signal to Noise Ratio				
(rms signal to rms noise)	dB min	48	•	•
(peak signal to rms noise)	dB min	58	•	•
Noise Power Ratio	dB min	37	•	•
Transient Response	ns	50	:	
Differential Caie?	ns	60		
Differential Gain	% Degrees	5	•	•
Bandwidth	Degrees	• •		
Small Signal 3dB	MH7	20	•	•
Large Signal 3dB	MHz	15	•	•
Flat ±0.1dB, dc through	MHz	5.5	•	• •
INIDI ITS				
Voltage Range				
Unipolar (Pin 5 Grounded)	v	0 to 1	•	•
Bipolar (Pin 5 open)	v	±0.5	•	•
Impedance (Terminated to Ground)	Ω	75	•	•
ENCODE COMMAND INPUT <sup>8</sup>				· · · · · · · · · · · · · · · · · · ·
Logic Levels TTL Compatible		"0" = 0 to $\pm 0.4V$	•	•
Dogie Devens, 11D Companiole		"1" = +2.4V  to  +5V	1 •	•
Impedance (terminated to ground)	Ω	75 ± 5%	•	•
Rise and Fall Times (10% to 90%) max	ns	10	•	•
Duration/Width 50% points (see timing diagram)	ns min	10	•	. 20
	ns max	50% duty cycle	40	•
Frequency (random or periodic)	dc to MHz	11	16	20
DIGITAL DATA OUTPUT <sup>8</sup>				
Format		Eight Paral	lel Bits NRZ	
Logic Levels, TTL		(Same as End	code Command)	
Drive Capability (not short circuit protected)	TTL Loads	10 Std	10 Schottky	
Time Skew	ns max	15	10	10
Coding		Straight Bi	nary (BIN)	
DATA READY OUTPUT				
Format <sup>9</sup>		RZ	•	•
Logic Levels, TTL		(Same as End	code Command)	
Drive Capability		10 Std	10 Schottky	
Width	ns	40±10	35±5	25±5
POWER REQUIREMENTS <sup>10</sup> MATV-0811 MATV-0816/MATV-0820				
+15V +2%/+11 8V to +15 5V	m A mer	210	•	70
-15V +2%/-11 8V to -15 5V	mA may	180	•	400
+5V ±5%/+5V +5%	mA max	450	540	200
-5.2V ±5%	mA max	280	*	N/A
TEMPERATURE RANGE				
Operating (case)	°c	0 to +70	•	•
Storage	°C	-55 to +85	•	•
D*		5510.05		

\*Same as MATV-0811.

NOTES

NOTES Applies to a customer specified operating frequency, ±10%. Outside this range, accuracy may degrade to ±0.3% ±1/2L5B. AC linearity expressed in terms of spurious in-band signals generated at specified encode rates. Pipeline delay not related to encode rate. DC to 5MHz while noise BW with slot frequency at 500kHz. Time to achieve 8-bit (0.2%) accuracy after F.S. step inpout. For signals not exceeding 10% overvoltage, the A/D will recover to 8-bit accuracy within 60ns after the signal returns to the specified range. Overvoltage inputs greater than 150% of F.S. may damage input circuits and should be avoided. Act maximum encode rate, 20 IRE units subcarrier, not including quantization effects. Consult factory for other voltage, impedance and logic level options.

<sup>9</sup> The leading edge of the data ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

<sup>9</sup> For MATV-0811, the leading edge of the Data Ready pulse occurs approximately 15ns before output data changes. The trailing edge is recommended for strobing data into external circuits. For MATV-0816, the leading edge of the Data Ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

For MATV-0820, the leading edge of the Data Ready pulse occurs approximately simultaneously with output data changes. The trailing edge is recompresed for strong probability annutation with output data changes. The trailing edge is recommended for strong data into external circuits. This provides a minimum of 20ns set-up time for external registers. "I The A/D's are calibrated at the factory at either ±120 or ±150 vas no-cost option. Other

operating voltages within this range may be specified by the user at slight additional cost. See application section for more information. Specifications subject to change without notice.



MECHANICAL OUTLINE AND DIMENSIONS

TINS ARE GULD FLATED FEM MICL-3204, TYPE II NOTES: DIMENSIONS AND LOCATION OF HOLD DOWN HOLES FOR MATV-0820 ARE SHOWN ON THE MECHANICAL OUTLINE FIGURE BELOW. NOT AVAILABLE ON MATV-0811 AND -0816.

DOT ON TOP INDICATES POSITION OF PIN 1.



DOT ON TOP INDICATES POSITION OF PIN 1.



PIN	FUNCTION	COMMENTS
1	POWER GROUND	•
2	- POWER INPUT	-11.8V (MIN); -16.5V (MAX)
3	+ POWER INPUT	+11.8V (MIN); +16.5V (MAX)
4	ANALOG GROUND	•
5	RANGE SELECT	UNIPOLAR = GROUND
		BIPOLAR - OPEN
6	ANALOG GROUND	•
7	ANALOG INPUT	OPTIONAL
8	ENCODE GROUND	•
9	ENCODE COMMAND	TTL, +5V (MAX)
10	POWER GROUND	
11	NO CONNECTION 0820	
	-5.2V POWER INPUT	1
	0811,0816	-5V (MIN), -5.5V (MAX)
12	+5V POWER INPUT	+4.75V (MIN); +5.25V (MAX)
13	DATA READY OUTPUT	TTL LEVELS
14	BIT 1 OUTPUT (MSB)	TTL LEVELS
15	BIT 2 OUTPUT	TTL LEVELS
16	BIT 3 OUTPUT	TTL LEVELS
17	BIT 4 OUTPUT	TTL LEVELS
18	BIT 5 OUTPUT	TTL LEVELS
19	BIT 6 OUTPUT	TTL LEVELS
20	BIT 7 OUTPUT	TTL LEVELS
21	BIT 8 OUTPUT (LSB)	TTL LEVELS
22	DIGITAL LOGIC GND.	•

ALL GROUNDS ARE INTERNALLY CONNECTED



Figure 1. MATV-0811 Timing Diagram at Maximum Sample Rate of 11MHz







Figure 3. MATV-0820 Timing Diagram Shown at an Encode Frequency of 20MHz

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Figure 4. Typical Differential Gain of MATV-0816 Operating at 15MHz Word Rates

#### **ORDERING INFORMATION**

Each MATV series A/D converter will be calibrated at  $\pm 15V$  as a standard. Order by model number either MATV-0811, MATV-0816 or MATV-0820.

#### **Optional Versions**

The MATV series A/D's are available with a variety of options, including analog input range and impedance, encode command input impedance, encode word rate, power supply voltage calibration, etc. Any option other than what is shown on the data sheet will have longer delivery, since each non-standard device is built on a per order basis.

A complete listing of optional designators is available from either the factory or your local Analog Devices' sales office.



Figure 5. Typical Differential Phase of MATV-0816 Operating at 15MHz Word Rates

#### **Device Marking**

The MATV series A/D that you order will be marked with a series of alphanumerics which specifically designate the options built into the device. For the standard devices, these will be as follows:

- MATV-0811 will be marked MATV-0811-1-BIN-15 for older devices, or MATV-0811-AA150 for newer devices.
- MATV-0816 will be marked MATV-0816-0175 BIN 75143150 for older devices, or MATV-0816 ABBA143150 for newer devices.
- MATV-0820 will be marked MATV-0820-0175 BIN 75 for older devices, or MATV-0820 ABAA for newer devices.

This information is provided so that there will be no confusion as to why information other than the basic model number appears on the device identification label, which might cause problems at a customers' incoming inspection.



### 10-Bit Video Analog-to-Digital Converter

### MOD-1005

#### FEATURES

10 Bits @ 5MHz Word Rate One-27 Sq. In. PC Board Built-In Track-and-Hold – 25ps Aperture Uncertainty 20MHz Analog Input Bandwidth TTL Compatible Low (10-Watt) Power Dissipation Signal-To-Noise Ratio Greater Than 58dB Noise Power Ratio Greater Than 49dB Completely Repairable

APPLICATIONS Radar Digitizing Digital Communications Real Time Spectrum Analysis High Resolution TV

#### **GENERAL DESCRIPTION**

Analog Devices' model MOD-1005 is a very high-speed A/D converter capable of digitizing video input signals to 10-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1005 is truly a breakthrough in high-speed A/D technology. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

The MOD-1005 is constructed on a single printed circuit card which is intended for mounting on a system mother-board, and occupies only 27 square inches. Within this A/D is the required sample/track and hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. <u>NO</u> external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1005 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1005 is backed by Analog Devices' limited one year warranty.





Block Diagram

### **SPECIFICATIONS** (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1005
RESOLUTION (FS = FULL SCALE)	10 Bits (0.1% FS)
LSB WEIGHT	4mV
ACCURACY (INCLUDING LINEARITY) @ DC	±0.05% Full Scale ±1/2LSB
Monotonicity	Guaranteed
Differential Nonlinearity vs. Temperature	0.0005% of FS/°C
Gain vs. Temperature	0.01% of FS/ C
DYNAMIC CHARACTERISTICS	
AC Linearity	Spurious Signals >59dB below FS
Conversion Time	See Text
Aperture Uncertainty (Litter)	425ns max
Aperture Time	45ns (±10ns from unit to unit)
Signal to Noise Ratio (rms signal to rms noise)	58dB min at 500kHz analog input
Noise Power Ratio <sup>2</sup>	49dB min
Transient Response (Full Scale Step Input)	10-Bit (0.05%) Accuracy within 50ns
Overvoltage Recovery Time	
Recovers to 10-bit accuracy after	
2 X FS input overvoltage in	200ns 20MHz min
Input Bandwidth (large signal 3dB)	15MHz min flat within ±0.1dB
input bandwidtin (large signal, 54D)	dc through 5MHz
INPUT Valtara Banga	+2 049V ES
voltage Kange	+4V Absolute max
Impedance	50Ω
Offset Voltage	Adjust to 0 with On Board Potentiometer
Offset vs. Temperature	0.01% Full Scale/°C
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = $+2.4V$ to $+5V$
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration Min/Max	20ns/60% of Duty Cycle
Sample Delay	45ns (unit to unit tolerance is ±10ns)
	This (unit to unit totelance is =1005)
DIGITAL DATA OUTPUT	10 Barallal Bits NP7
Format Logic Levels TTL Compatible	"0" = 0  to  +0.4V
Logic Levels, TTL Companyie	"1" = +2.4V to $+5V$
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or
	2 Standard TTL Loads
Time Skew	10ns max
Coding	2's Complement (2SC)
Conversion Time	See Text on the Next Page
POWER REQUIREMENTS <sup>3</sup>	typ/max
+15V ±5%	150/170mA
$-15V \pm 5\%$	150/170mA
-0V 14%	350/400m A
-5V ±5%	500/550mA
Power Consumption	10 Watts
TEMPERATURE RANGE	·····
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	100 Linear Feet Per Min (LFPM)
MTBF <sup>4</sup>	7.62×10 <sup>4</sup> Hours
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card
NOTES	· · · · · · · · · · · · · · · · · · ·

NOTES <sup>1</sup> AC linearity expressed in terms of spurious in-band signals generated as specified encode rates, with dc to 2.5MHz analog input. <sup>2</sup> DC to 2.4MHz white noise BW with Slot frequency of 512kHz. <sup>3</sup> LfS vapplies must be equal and opposite within 200mV and track over temperature. <sup>4</sup> MTBF based on 30°C ambient; ground; benign.

Specifications subject to change without notice.

#### OUTLINE DIMENSIONS

Dimensions shown in inches (mm).



#### CONVERSION TIME

Output data is valid two encode command clock periods plus 200ns after application of an initial encode command pulse. Due to the pipeline delay effect of the A/D, a total of three encode command pulses are required to shift the data to the output of the A/D. For example, with a 5MHz encode rate, data is valid 600ns after the application of the first encode

#### PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	-5V	16	BIT 7
2	ENCODE COMMAND	17	BIT 8
3	GND*	18	BIT 9
4	+5V	19	BIT 10 LSB
5	GND*	20	+15V
6	GND*	21	-15V
7	-6V	22	GND*
8	-6V	23	GND*
9	BIT 1 MSB	24	GND*
10	BIT 2	25	GND*
11	BIT 3	26	GND*
12	BIT 4	27	GND*
13	BIT 5	28	GND*
14	BIT 6	29	GND*
15	GND*	30	GND*
		31	ANALOG INPUT

\*ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE MOD-1005

#### ORDERING INFORMATION

•

Order model number MOD-1005 A/D converter. Mating pin sockets for the MOD-1005 are model number MSB-2 (31 required per A/D).

command pulse – assuming that two pulses occur after the first.

Use of the trailing edge of the encode command is recommended for strobing output data into external register (see Figure 1).



DATA T<sub>N</sub> (THE RESULT OF ENCODE COMAND T<sub>N</sub>) OCCURS TWO CONVERSION PERIODS PLUS 200ns AFTER ENCODE COMMAND T<sub>N</sub>. FOR A 5MHz WORD RATE AS SHOWN, DATA IS VALID 200ns AFTER THE THIRD ENCODE COMMAND PULSE OT N + 600ns. IN ALL CASES, THREE ENCODE COMMAND PULSES ARE REQUIRED FOR TRANSFER OF DATA TO THE OUTPUT, DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D. NO DATA READY PULSE IS SUPPLIED.

Figure 1. MOD-1005 Timing Diagram

#### **GROUND CONNECTIONS**

It should be noted that the MOD-1005 PC board has 13 ground pins. These are all connected to the ground plane on the board. For best results it is recommended that ALL of these pins be connected to a massive system or "mother board" ground plane.

#### **CALIBRATION PROCEDURE (MOD-1005)**

The MOD-1005 A/D is precisely calibrated at the factory before shipment, and should need no further calibration. However, if slight readjustments of the A/D are required in the system, the following procedure should be followed. It should be remembered that the output coding of this A/D is 2SC.

#### Offset Adjustment

The offset is adjusted by varying potentiometer R33 with 0 volts applied to the analog input. To obtain the proper output

code, observe that the digital output is changing between 1111111111 and 000000000 at this adjustment level. When properly adjusted a digital code of 0000000000 will represent analog input 1LSB above zero volts, and a digital code of 11111111 will represent an analog input of 1LSB below zero volts.

#### Gain Adjustment

The gain is adjusted by varying potentiometer R3. This adjustment is made by applying +2.042V (FS -1 1/2LSB) to the analog input and while monitoring the digital output, adjust R3 for the output code varying between 0 1 1 1 1 1 1 1 1 0 and 0 1 1 1 1 1 1 1 1 1 (FS). If the user needs to offset the entire range of the A/D, this can be accomplished by readjusting R33 as required. However, in this procedure, the offset should always be adjusted first.



A/D Converter Assembly

# 

### **10-Bit Video** Analog-to-Digital Converter

#### FEATURES

10-Bits @ 20MHz Word Rates One 35 Sq. In. PC Board Built-In Track-and-Hold – 25ps Aperture 15MHz Large-Signal Input Bandwidth **ECL Compatible** Signal-to-Noise Ratio Greater Than 56dB Noise Power Ratio Greater Than 45dB

#### APPLICATIONS

**Television Digitizing** Radar Digitizing **Medical Instrumentation Digital Communications** Spectrum Analysis Sonar Digitizing

#### GENERAL DESCRIPTION

The Analog Devices' model MOD-1020 is an ultra-high-speed A/D converter capable of digitizing video input signals to 10bit accuracy at word rates through 20MHz. The MOD-1020 is another in the series of state-of-the-art A/D converters from Analog Devices that employs the unique digital correcting subranging (DCS) conversion technique to virtually eliminate errors normally associated with subranging type A/D converters. No other A/D converter commercially available offers the user the speed and accuracy attainable with the MOD-1020.

The MOD-1020 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 35 square inches. The A/D is complete with internal track-and-hold, encoder, timing circuitry, references, and latched output. It produces a true all-parallel digital output.

The encode command input, digital outputs, and data ready output are balanced ECL compatible. The A/D requires only an external encode command input pulse and external power supplies for operation. The analog input impedance is at least 500 $\Omega$ , so that the user can easily terminate the A/D with lower impedances in his system. Gain and offset potentiometers are provided on the card so that the A/D can be operated in either the unipolar or bipolar modes. The A/D is fully repairable.

The MOD-1020 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications (baseband digitizing), composite color television digitizing, spectrum analysis, medical instrumentation, and many others. Each MOD-1020 is backed by Analog Devices' limited one-year warranty.









11

and Vectorscope Back-to-Back No A/D Conversion







Differential Phase - Model MOD-1020 ADC and Model 4120E DAC Back-to-Back 14.4MHz Conversion (Word) Rate

Differential Gain - Model MOD-1020 and Model 4120E DAC Back-to-Back 14.4MHz Conversion (Word) Rate

The above waveforms were obtained utilizing a Tektronix Model 149A N.T.S.C. Test Signal Generator with a 20 IRE unit TV test signal output. The display (output) was obtained using a Tektronix Model 520A Vectorscope.

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### SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1020	
RESOLUTION (FS = FULL SCALE)	10 Bits (0.1% FS)	
LSB WEIGHT	1mV or 2mV Depending on Analog Input Range	
ACCURACY (INCLUDING LINEARITY) @ DC	±0.05% Fuli Scale ±1/2LSB	
Monotonicity	Guaranteed 0 to +70°C	
Nonlinearity vs. Temperature Gain vs. Temperature	0.0005% of FS/°C	
DYNAMIC CHARACTERISTICS		
AC Linezrity <sup>1</sup> (dc to 1MHz)	Spurious Signals >60dB below FS	
(1MHz to 5MHz)	Spurious Signals >55dB below FS	
(5MHz to 10MHz)	Spurious Signals >50dB below FS See Text and Timing Diagram	
Conversion Rate <sup>2</sup>	dc to 20MHz (See Note and Ordering Information)	
Aperture Uncertainty (Jitter)	±25ps max	
Signal to Noise Ratio <sup>3</sup>	56dB min	
Signal to Noise Ratio <sup>4</sup>	65dB min	
Noise Power Ratio <sup>5</sup>	45dB min, 47dB typ	
Overvoltage Recoverv <sup>7</sup>	50ns	
Input Bandwidth (small signal, 3dB) <sup>8</sup>	30MHz	
Input Bandwidth (large signal, 3dB) <sup>9</sup>	15MHz; Flat within 0.2dB, dc to 10MHz	
60kHz: 62kHz	In-Band Spurious Signals >60dB below FS	
4.998MHz; 5.000MHz	In-Band Spurious Signals >55dB below FS	
9.996MHz; 9.998MHz Differential Cain <sup>10</sup>	In-Band Spurious Signals >50dB below FS	
Differential Phase <sup>10</sup>	0.5° with 20 IRE Unit Reference	
ANALOG INPUT (See Notes on Input		
Range in Text)		
Voltage Range	1V p-p or 2V p-p, Depending on Hook-Up Fither Unipolar or Binolar	
	±4V Absolute max Input	
Impedance	1000Ω (2V Input Range)	
Offset	50037 (1V Input Range) Adjustable to Zero with On-Card Potentiometer (R4)	
Offset vs. Temperature	0.01%/°C	
ENCODE COMMAND INPUT	· · · · · · · · · · · · · · · · · · ·	
Logic Levels, ECL Compatible	"0" = -1.7V	
(Balanced Input)	$100\Omega$ Line-to-Line	
Rise and Fall Times	Sns max	
Duration (min/max)	10ns/70% of Duty Cycle	
Frequency	Specified by Customer, to 20MHz (See Ordering Information)	
DIGITAL OUTPUT DATA	10 Parallal Birr ND7	
Logic Levels, ECL Compatible	"0" = -1.7V	
(Balanced Outputs)	"1" = -0.9V	
Drive Time Skew	7512 to 10012, Line-to-Line	
Coding	Binary (BIN); 2's Complement (2SC)	
DATA READY OUTPUT		
Logic Level, ECL Compatible	"0" = -1.7V	
(Balanced Output) . Rise and Fall Times	n = −0.9V Sns max	
Duration	25ns ±3ns	
Conversion Time	Output data valid 185 ±20ns after the leading edge of second	
	of the trailing edge of the Data Ready pulses is required to	
	shift the data to the output. For example, with a 20MHz encode	
	rate, data is valid 285 ±20ns after the application of the first	
	of the trailing edge of the Data Ready pulse is recommended	
	for strobing output data into external registers.	
POWER REQUIREMENTS		
+15V ±5%	200mA	
-15V ±5%	200mA	
-5.2V ±5%	2.7A	
Power Consumption	21 Watts	
TEMPERATURE RANGE <sup>11</sup>		
Operating	U to +7U C -55°C to +85°C	
Cooling Requirements	500 Linear Feet per Minute (LFPM)	
PHYSICAL CHARACTERISTICS		
Construction	Single Printed Circuit Card	
NOTES	<sup>8</sup> With analog input signal 40dB below FS.	
<ul> <li>AC linearity expressed in terms of spurious in-band signals g encode rate at the analog frequencies ( ) shown.</li> </ul>	enerated at ZUMHZ * WITH PS analog input. 19 Applies to devices optimized for video applications. Differential gain and	
<sup>a</sup> To be specified by the customer, See text and ordering information, <sup>b</sup> BMS signal to mis noise ratio with SO(kH) analog input <sup>c</sup> and customer and ordering information.		
Peak-to-peak signal to rms noise ratio with 500kHz analog input. DC to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz and "±15V must be equal and opposite within 200mV and track		

over temperature.

<sup>1</sup>Oc. to 5.2MR2 white hole Dandwidth with sol frequency of 5.860MH2 and an encode rate of 20MH2.
 <sup>4</sup>Recovers to 10-bit accuracy after 2 X FS input overvoltage in time specified.
 <sup>7</sup>For full-scale step input, attains 10-bit accuracy in time specified.

Specifications subject to change without notice.

### **Physical Characteristics**



MOD-1020 Block Diagram

#### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MOD-1020 Timing Diagram



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THE OFFSET POTENTIOMETER (R4) HAS SUFFICIENT RANGE TO ALLOW THE USER TO OPERATE THE ADC IN EITHER THE UNIPOLAR OR BIPOLAR MODE. THE ADC'S ARE CALIBRATED IN THE BIPOLAR CONFIGURATION AT THE FACTORY.

MOD-1020 Analog Input Range Options

#### OFFSET AND GAIN ADJUSTMENT

The offset of the ADC is adjusted by varying potentiometer R4. Apply an input voltage to the analog input corresponding to positive full scale. Adjust R4 such that the digital output is changing between 1111111111 and 111111110.

The gain of the ADC is adjusted by varying potentiometer R25. Apply an input voltage to the analog input that corre-

sponds to negative full scale. Adjust R25 such that the digital output is changing between 000000000 and 000000001.

In the foregoing, the ADC is calibrated to have a unipolar positive transfer function. If bipolar input range is required, adjust R4 to offset the entire input by one-half of the full scale input.

In setting the gain, always adjust R4 first to obtain the correct setting for full scale positive input.



#### Location of Adjustment Potentiometers

#### **ORDERING INFORMATION**

IMPORTANT-THE ENCODE RATE OF THE MOD-1020 MUST BE SPECIFIED BY THE CUSTOMER AS SHOWN BELOW:

ORDER MODEL NUMBER: MOD-1020- "XXX", where "XXX" is to be specified by the customer. "XXX" represents the encode word rate in MHz with the decimal place assumed to be (but not shown) between the second and third places. Full 10-bit accuracy will be maintained within ±12% of this

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specified frequency, up to a maximum of 21MHz. For example, a device specified as MOD-1020-200 is for operation at 20,0MHz and will maintain accuracy from 17.6MHz to 21MHz.

For encode rates of 10MHz or less, the MOD-1020 will maintain fully accuracy to 10MHz. For encode frequencies of 10MHz or less, order MOD-1020-100.

Mating sockets for the MOD-1020 are model number MSB-2 (36 required per A/D).

## 

### 12-Bit Video Analog-to-Digital Converter

### MOD-1205

#### **FEATURES**

12 Bits @ 5MHz Word Rate One-27 Sq. In. PC Board Built-In Track-and-Hold – 25ps Aperture Uncertainty 15MHz Analog Input Bandwidth TTL Compatible Low (13-Watt) Power Dissipation Signal-to-Noise Ratio Greater Than 66dB Noise Power Ratio Greater Than 56dB Completely Repairable

#### APPLICATIONS Radar Digitizing Digital Communications Real Time Spectrum Analysis Signature Analysis

#### **GENERAL DESCRIPTION**

Analog Devices' model MOD-1205 is a very high-speed A/D converter capable of digitizing video input signals to 12-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1205 is truly a breakthrough in high-speed A/D technology. It utilizes the latest state-of-the-art conversion technique called digital correcting subranging (DCS) to effectively eliminate errors normally associated with subranging type ADCs. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

The MOD-1205 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 27 square inches. Within this A/D is the required sample/track-and-hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. <u>NO</u> external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1205 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1205 is backed by Analog Devices' limited one year warranty.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



## **SPECIFICATIONS** (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1205
RESOLUTION (FS = FULL SCALE)	12 Bits (0.024% FS)
LSB WEIGHT	1mV
ACCURACY (INCLUDING LINEARITY) @ DC Monotonicity	$\pm 0.0125\%$ Full Scale $\pm 1/2$ LSB Guaranteed (0 to $\pm 70^{\circ}$ C)
Nonlinearity vs. Temperature	0.005% of FS/°C, max 0.01% of FS/°C, type: 0.03% of FS/°C, max
DVNAMIC CHARACTERISTICS	
AC Linearity <sup>1</sup> (dc to 1MHz) (1MHz to 2.5MHz) Conversion Time	Spurious Signals >70dB below FS, max Spurious Signals >65dB below FS, max; >68dB, typ See Text and Timing Diagram
Conversion Rate (Word Rate)	5MHz
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time Signal to Noise Ratio <sup>2</sup>	30ns (±10ns from unit to unit) 66dB min; 68dB, typ
Noise Power Ratio <sup>3</sup>	56dB min, 58dB typ
Overvoltage Recovery Time <sup>5</sup>	12-Bit (0.0125%) Accuracy within 200ns
Input Bandwidth (small signal 3dB)	15MHz min
Input Bandwidth (large signal, 3dB)	10MHz min; flat within ±0.1dB, dc through 5MHz
ANALOG INPUT	
Voltage Range	±2.048V FS ±4V Absolute max
Impedance	400 $\Omega$ with pin 30 open, 50 $\Omega$ with pin 30 grounded
Offset vs. Temperature	Adjust to 0 with On Board Potentiometer 0.02% ES/°C super 0.05% of ES/°C may
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V "1" = +2.4V to +5V
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration min/max Frequency (Pandom or Periodic)	25ns/50% of Duty Cycle
	Jimil
Format	12 Desailel Rise ND7
Logic Levels, TTL Compatible	"0" = 0  to  +0.4V "1" = +2.4V  to  +5V
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or 2 Standard TTL Loads
Time Skew	10ns max
Coding Commission Time	Offset Binary (OBN) or 2's complement (2SC)
	See Text on the Next Page
POWER REQUIREMENTS <sup>®</sup>	<b>a</b> aa
+13V +3% -15V +5%	200mA 150m A
-6V ±4%	700mA
+5V ±5%	800mA
Power Consumption	13 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	500 Linear Feet Per Min (LFPM) @ +70°C
PHYSICAL CHARACTERISTICS Construction	Single Printed Circuit Card
NOTES <sup>1</sup> AC linearity expressed in terms of spurious in-band signa rates at analog input frequencies ( ). <sup>2</sup> rms signal to rms noise at 500kHz analog input. <sup>3</sup> de to 2.4MHz white noise bandwidth with slot frequency <sup>4</sup> For full-scale step input, attains 12-bit accuracy in times 8	ls generated at specified encode y of 512kHz. specified.

<sup>6</sup> Por full-scale step input, attains 12-01 accuracy in third specified.
 <sup>6</sup> Recovers to 12-bit accuracy after 2 × FS input overvoltage in time specified.
 <sup>6</sup> ±15V supplies must be equal and opposite within 200mV and track over temperature.

Specifications subject to change without notice.









NOTE: WITH PIN 30 OPEN, ANALOG INPUT IMPEDANCE IS 400Ω. WITH PIN 30 GROUNDED, ANALOG IMPEDANCE IS 50Ω.

#### MOD-1205 Block Diagram

#### ORDERING INFORMATION

Order model number MOD-1205 A/D converter. Mating pin sockets for the MOD-1205 are model number MSB-2 (32 required per A/D).

#### **CONVERSION TIME**

Output data is valid two encode command clock periods plus 275ns  $\pm 25$ ns after application of an initial encode command pulse. Due to the pipeline delay effect of the A/D, a total of

three encode command pulses are required to shift the data to the output of the A/D. For example, with a 5MHz encode rate, data is valid  $675ns \pm 25ns$  after the application of the first encode command pulse-assuming that two pulses occur after the first.

Use of the trailing edge of the encode command is recommended for strobing output data into external register (see Figure 1).



DATA T<sub>N</sub> (THE RESULT OF ENCODE COMMAND T<sub>N</sub>) OCCURS TWO CONVERSION PERIODS PLUS 275ns ±25ns AFTER ENCODE COMMAND T<sub>N</sub>. FOR A 5MHz WORD RATE AS SHOWN, DATA IS VALID 275ns ±25ns AFTER THE THIRD ENCODE COMMAND PULSE OR T<sub>N</sub> + 675ns ±25ns. IN ALL CASES, THREE ENCODE COMMAND PULSES ARE REQUIRED FOR TRANSFER OF DATA TO THE OUTPUT, DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D. NO DATA READY PULSE IS SUPPLIED.

#### Figure 1. MOD-1205 Timing Diagram

#### **GROUND CONNECTIONS**

It should be noted that the MOD-1205 PC board has 9 ground pins. These are all connected to the ground plane on the board. For best results it is recommended that ALL of these pins be connected to a massive system or "mother board" ground plane.

#### **CALIBRATION PROCEDURE (MOD-1205)**

The MOD-1205 A/D is precisely calibrated at the factory before shipments and should need no further calibration. However, if slight readjustments of the A/D are required in the system, the following procedure should be followed. This procedure refers to a binary output.

#### Offset Adjustment

The offset is adjusted by varying potentiometer R22 with 0 volts applied to the analog input. To obtain the proper output

code, observe that the digital output is changing between 10000000000 and 011111111111 at this adjustment level. When properly adjusted a digital code of 1000000000000 will represent analog input 1LSB above zero volts, and a digital code of 01111111111111 represent an analog input of 1LSB below zero volts.

#### Gain Adjustment

The gain is adjusted by varying potentiometer R2. This adjustment is made by applying +2.0465V (FS -1.1/2LSB) to the analog input and while monitoring the digital output, adjust R2 for the output code varying between 1.1111111110and 1.111111111(FS). If the user needs to offset the entire range of the A/D, this can be accomplished by a readjusting R22 as required. However, in this procedure, the offset should always be adjusted first.



R22 OFFSET ADJUST

Location of Adjustment Potentiometers

## Voltage-to-Frequency & Frequency-to-Voltage Converters

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### **Selection Guide** Voltage-to-Frequency Converters





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Low Cost A/D Conversion Versatile Input Amplifier Positive or Negative Voltage Modes Negative Current Mode High Input Impedance, Low Drift Single Supply, 5 to 36 Volts Linearity: ±0.05% FS Low Power: 1.2mA Quiescent Current Full Scale Frequency up to 100kHz 1.00 Volt Reference Thermometer Output (1mV/K) F/V Applications



#### AD650

V/F Conversion to 1MHz Reliable Monolithic Construction Very High Linearity 0.002% typ at 10kHz 0.005% typ at 10kHz 0.07% typ at 100kHz Input Offset Trimmable to Zero CMOS or TTL Compatible Unipolar, Bipolar, or Differential V/F V/F or F/V Conversion Vol. I 11-15

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#### VOL. II, 12-2 V/F & F/V CONVERTERS





#### ADVFC32

High Linearity	Vol. I
±0.01% max at 10kHz FS	11-27
±0.05% max at 100kHz FS	
±0.2% max at 0.5MHz FS	
Output DTL/TTL/CMOS Compatible	
V/F or F/V Conversion	
6 Decade Dynamic Range	
Voltage or Current Input	
Reliable Monolithic Construction	

### MODEL 458/MODEL 460

Model 458: Full Scale Output 100kHz Model 460: Full Scale Output 1MHz High Stability: 5ppm/°C max, Model 458L 15ppm/°C max, Model 460L High Linearity: ±0.01% max at 100kHz, Model 458 ±0.015% max at 1MHz, Model 460 Versatility: Differential Input Stage Voltage and Current Inputs Floating Inputs: ±10V CMV Wide Dynamic Range: 6 Decades, Model 460 TTL/DTL Compatible Output No External Components to Meet Rated Performance Vol. II 12-13

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### Selection Guide Frequency-to-Voltage Converters



### MODEL 451/MODEL 453

Model 451: Full Scale Input 10kHz

Model 453: Full Scale Input 100kHz

Versatility: Adjustable Threshold, Gain & Output Offset

Guaranteed Low Nonlinearity: 80ppm max, 451L and 453L

Accepts TTL, CMOS, HNIL, Sinewave, Pulse,

Squarewave and Triangle Wave Input Signals No External Components to Meet Rated

Performance + 20mA Output to Operate Relays and Meters

Low Profile Package, 0.4" Case Height

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# Orientation Voltage-to-Frequency & Frequency-to-Voltage Converters

#### **VOLTAGE-TO-FREQUENCY CONVERTERS**

Voltage-to-frequency converters (VFC's) convert analog voltage or current levels to pulse trains or square waves in a logiccompatible form (usually TTL) at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal, responding directly to changes in the input signal; external-clock synchronization is not required. V/F converters find applications in analog-to-digital converters with high resolution, long-term high precision integrators, two-wire high-noise-immunity digital transmission, and digital voltmeters.

#### FREQUENCY-TO-VOLTAGE CONVERTERS

Frequency-to-voltage converters (FVC's) perform the inverse operation; they accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. Combining adjustable threshold, gain, and output offset with low linearity-error, F/V converters offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage. Examples are motor-speed controllers, power-line frequency monitors, and VCO stabilization circuits. In analog-to-analog data transmission, they convert serially transmitted data in the form of pulse streams back to analog voltage.

Applications of both forms of conversion, as appropriate to specific device types, are illustrated with varying degrees of detail on the individual data sheets.

#### FACTORS IN CHOOSING VFC's AND FVC's

Voltage-to-frequency converters are available from Analog Devices in both module- and monolithic-IC- form. The output of modular types, ranging from 10kHz to 1MHz F.S., is a train of pulses of constant height and width, with very low duty cycle for small analog inputs. The technical data in this volume embrace exceptionally high performance (low-drift and high-resolution) V/F converters, in the form of encapsulated modules. As the Selection Guide indicates, there is also technical data, to be found in Volume I, on a range of monolithic V/F converters, including ADI's unique AD537, which has symmetrical square-wave output, and both voltage and temperature references. Apart from performance specifications, the tradeoffs between module and IC are as follows: modular VFCs have the advantages of completely specified performance; they do not rely on the specifications of critical external components, because the complete selfcontained functional package requires no external components; trims are optional. IC's, on the other hand, have the advantages of lower cost and smaller size, and—in the case of the AD537-versatility of output and input connections, lower offset drift, flexibility of frequency range, low power, singlesupply operation, low external-component count, plus builtin voltage—and temperature—references. Modules offer better linearity, lower gain drift, and higher full-scale frequencies.

The most-popular VFC designs (Figure 1) contain an integrator, which charges at a rate proportional to the value of the input signal. Each time the integrator's charge has been increased by a precisely metered increment, the threshold crossing produces a pulse of accurately known area. The pulse serves both as the output (via a buffer) and as a subtractive charge



Figure 1. Block Diagram – Models 458, 460 VFC's

increment to reduce the integrator's net charge. The next pulse is triggered when the net integral has again reached the threshold. The relationship between the pulse rate and the input level is linear.





Frequency-to-voltage-converter modules (Figure 2) average a train of equal-area pulses that are generated internally by a precision charge dispenser, in response to each crossing of an input threshold. The analog output voltage is proportional to the sum of the pulse areas over a given period.

#### SPECIFICATIONS

The salient specifications for VFC's are (non)linearity, as a percentage of full-scale frequency; frequency range, the greater the frequency range, the greater the resolution for a given counting period; full-scale-calibration error; gain-temperature coefficient, in ppm of signal per °C, where "gain" is the ratio of full-scale frequency to full-scale voltage, input-offset temperature coefficient; overrange capability, within rated specifications, and step response, the worst-case time interval required for the frequency to respond to a full-scale-step input change.

For FVC's, important specs, in addition to accuracy specs corresponding to the above, include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated, and for versatility in interfacing various types of sensors directly), *hysteresis*, to provide a degree of insensitivity to noise superimposed on a slowly-varying input waveform, and *dynamic response* (important in motor control).

Definitions of some critical specifications, and the conditions for adjusting or measuring them, are detailed on individual data sheets.



### Low-Cost, Versatile, 10/100kHz Frequency to Voltage Converters

# **MODELS 451, 453**

#### FEATURES

#### Low Cost

Versatility: Adjustable Threshold, Gain & Output Offset Guaranteed Low Nonlinearity: 80ppm Max, 451L and 453L Accepts TTL, CMOS, HNIL, Sinewave, Pulse, Squarewave and

Triangle Wave Input Signals No External Components to Meet Rated Performance +20mA Output to Operate Relays and Meters Low Profile Package, 0.4" Case Height Meet MIL-STD-202E Environmental Testing

#### APPLICATIONS

Motor Control and Speed Monitor Line Frequency Monitor and Alarm Indicator Fluid Flow Measurements and Control FM Demodulation and VCO Stabilization Frequency vs. Amplitude Response Measurements

#### GENERAL DESCRIPTION

Models 451 and 453 are low cost 10kHz and 100kHz frequency to voltage converters that feature excellent low nonlinearity to less than 80ppm, output current of +20mA and the capability of interfacing with TTL, HNIL, CMOS, sinewave, squarewave, pulse and triangular input signals. External components are not required to achieve rated performance, however, extreme versatility is maintained by allowing access to all critical points of the design. This versatility allows programmable input threshold, gain, and output offset voltage.

Both models 451 and 453 are available in three selections, each offering guaranteed maximum nonlinearity error as well as maximum gain drift error. Models 451J and 453J offer 0.03% max nonlinearity and 100ppm/°C max gain drift. Models 451K and 453K offer 0.015% max nonlinearity and 50ppm/°C max gain drift. Models 451L and 453L offer 0.008% max nonlinearity and 50ppm/°C max gain drift.

WHERE TO USE FREQUENCY TO VOLTAGE CONVERTERS Pin compatible with existing popular models, these versatile new designs offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage.

Process Control Systems: For motor speed controllers, power line frequency monitoring and fluid flow measurements where flow transducers, such as variable reluctance magnetic pickups, provide pulse train outputs as a linear function of flow rate.

Audio and Accoustic Systems: For wow and flutter measurements with tape recorders and turntables, FM demodulation and speaker response measurements.

Test Instrumentation: For VCO stabilization, analog readout frequency meter, vibrational analysis and frequency versus amplitude X-Y plots where the vertical axis presents the nor-



mal amplitude signal and the horizontal axis presents the output signal from the F/V converter.

**Data Acquisition Systems:** For converting serially transmitted data back to analog voltages.

#### **DESIGN FEATURES AND USER BENEFITS**

The combination of low cost and high performance provided by models 451 and 453 offers exceptional quality and value to the OEM designer. These compact modules have been designed to provide maximum versatility, thereby increasing their utility in a broad scope of applications.

Adjustable Input Threshold: Threshold level is externally resistor programmable from 0 to  $\pm 12V$ , permitting simple, direct interface with low level signals, e.g. 10mV p-p, as well as with high level inputs such as CMOS and HNIL logic levels, e.g. 0 to  $\pm 12V$ .

Adjustable Gain: Model 451 can be adjusted to provide full scale output voltage for any input frequency from 100Hz to 20kHz. Model 453 can be adjusted to provide full scale output voltage for any input frequency from 1kHz to 200kHz. This adjustable gain feature enables the user to easily match the maximum frequency output from a wide class of frequency transducers to the +10V full scale output from models 451 and 453. Increased signal conversion sensitivity with higher resolution results.

Adjustable Output Offset Voltage: The output offset is adjustable from -10V to +10V, enabling bipolar outputs or expanded scale measurements or setting the input frequency where zero output voltage occurs.

# **SPECIFICATIONS** (typical @ +25°C and $V_s = \pm 15V$ dc unless otherwise noted)

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		10kHz FULL SCAL	E		100kHz FULL SCAI	.e	
MODEL	J	451 K	L	J	453 К	L	
TRANSFER FUNCTION	,	$E_{O} = (10^{-3} V/Hz)(F_{IN})$	1)	$E_{O} = (10^{-4} V/Hz)(F_{IN})$			
FREQUENCY INPUT Frequency Range Overrange Waveforms Pulse Width (Pulse Train Input) Threshold With External Adjustment Hysteresis Levels (TTL Compatible) High	dc to 10kHz min 10% min Sine, Square, Triangle, Pulse Train 20µs min +1.4V 0V to ±12V ±50mV +1.45V to +12V			dc to 100kHz min 10% min Sine, Square, Triangle, Pulse Train 2µs min +1.4V 0V to ±12V ±100mV +1.5V to +12V			
Low Max Safe Input Voltage <sup>1</sup> Impedance		-12V to +1.35V $\pm V_{S}$ 10MQ  10nF			-12V to +1.3V $\pm V_{S}$		
ACCURACY Warm-Up Time Nonlinearity <sup>2</sup> F <sub>IN</sub> = 1Hz to 11kHz F <sub>IN</sub> = 1Hz to 110kHz Gain vs. Temperature <sup>3</sup> (0 to +70°C) vs. Supply Voltage vs. Time	±0.03% max ±100ppm/°C max	one minute ±0.015% max ±50ppm/°C max ±300ppm/%	±0.008% max — ±50ppm/°C max	±0.03% max ±100ppm/°C max	one minute ±0.015% max ±50ppm/°C max ±350ppm/%0 mth	±0.008% max ±50ppm/°C max	
$\begin{array}{l} \textbf{RESPONSE} \\ \textbf{Step Response to $\pm$0.5\% of Final Value} \\ \textbf{F}_{IN} = d \textbf{c to Full Scale} \\ \textbf{F}_{IN} = Full Scale to dc \\ \textbf{Internal Filter Time Constant} \\ \textbf{External Filter Time Constant} \end{array}$		4ms 30ms 200μs 20ms/μF			0.8ms 4ms 24µs 20ms/µF		
$\begin{array}{c} \text{OUTPUT}^4 \\ \text{Voltage} \left( F_{\text{IN}} = \text{Full Scale} \right)^5 \\ \text{Current } \left( E_0 = +10 V, -10 V \right) \\ \text{Offset Voltage}^6 @ +25^\circ \text{C} \\ \text{vs. Temperature } (0 \text{ to } +70^\circ \text{C}) \\ \text{vs. Supply Voltage} \\ \text{vs. Time} \\ \text{Ripple} \\ \text{F}_{\text{IN}} = 11 \text{Hz} \\ \text{F}_{\text{IN}} = 10 \text{kHz} \\ \text{F}_{\text{IN}} = 10 \text{kHz} \\ \text{F}_{\text{IN}} = 10 \text{kHz} \\ \text{Impedance} \\ \text{Offset Scale Factor}^7 \end{array}$		+9.85V min; +9.95V (+20, -2)mA min ±7.5mV max ±30μV/° C max ±100μV/% max ±100μV/month 3mV p-p 80mV rms  0.1Ω -56μA/V	max		+9.85V min; +9.95V (+20, -2)mA min ±7.5mV max ±30μV/ <sup>0</sup> C max ±50μV/ <sup>0</sup> K max ±100μV/month 55mV p-p 35mV rms 35mV rms 35mV rms -45μA/V	max	
POWER SUPPLY <sup>8</sup> Voltage, Rated Performance Voltage, Operating Current, Quiescent TEMPERATURE RANGE Rated Performance Operating Storage		±15V dc ±(12 to 18)V dc (+10, -8)mA 0 to +70°C -25°C to +85°C			±15V dc ±(12 to 18)V dc (+10, -8)mA 0 to +70°C -25°C to +85°C		
MECHANICAL Case Size Weight	L	1.5" x 1.5" x 0.4" 25 grams	· · ·	I	1.5" x 1.5" x 0.4" 25 grams		

NOTES <sup>1</sup>F<sub>IN</sub> and REF terminals can be shorted to ±V<sub>s</sub> indefinitely without damage. <sup>3</sup>Nonlinearity error is specified as a percentage of 10V full scale output level. <sup>3</sup>Gain temperature drift is specified in ppm of output signal level. <sup>4</sup>OUT terminal can be shorted indefinitely to ±V<sub>s</sub> and ground without damage. <sup>5</sup>Adjustable to +10.000V using FULL SCALE ADJUST trim pot.

<sup>6</sup> Adjustable to zero using 50kD OFFSET ADJUST trim pot. <sup>7</sup> Current into the SUM PT terminal to offset the output voltage positive. <sup>8</sup> Recommended power supply, ADI model 904, ±15V @ 50mA output. Specifications subject to change without notice.

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	_106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs
Temperature Cycling	102A_	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



MATING SOCKET: AC1050

### Applying the Frequency-to-Voltage Converter

#### FREQUENCY TO VOLTAGE OPERATION

Models 451 and 453 accept virtually any signal waveshape providing accurate conversion into an output voltage proportional to the input signal frequency. The only restriction is that the input signal must remain above the threshold level for  $20\mu$ s when using model 451, and  $2\mu$ s when using model 453. Linear, stable conversion over four decades of input range for model 451 and five decades of input range for model 453, is achieved using a precision charge-dispensing design approach. Figure 1 represents a functional block diagram for both models 451 and 453 frequency to voltage converters.



Figure 1. Block Diagram – Models 451 & 453 F/V Converters

#### THEORY OF OPERATION

Input signals are applied directly to a comparator, A1, which is internally set to provide a +1.4V threshold with ±50mV hysteresis for model 451 and ±100mV hysteresis for model 453. This threshold level offers excellent noise immunity for TTL input levels. Following the input comparator is a precision charge dispensing circuit and output amplifier where the comparator signal is converted to a dc voltage. When the input comparator changes state, C<sub>C</sub> is alternately charged from a precision voltage reference and discharged through the summing point of an output amplifier, A2. A fixed amount of charge, Q, is controlled during each charge/discharge cycle. The higher the input frequency, the higher the average current into the summing point of A2. A current to voltage conversion is then accomplished by R<sub>F</sub>. The current pulses from the charge dispensing circuit are integrated by CF to reduce ripple. Added filtering for low frequency input signals is provided by an adaptive filter at the output of the charge dispensing circuit.

#### **BASIC F/V HOOK-UP**

Models 451 and 453 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figure 2 illustrates the basic wiring connection for either F/V converter model. Using the basic hookup as shown, full scale output voltage accuracy is +10V, -1/2% to -1/2%. The output offset voltage is 0V to  $\pm 7.5$  mV. The Full Scale and Output Offset errors can be eliminated by using the FINE TRIM PROCEDURE.



Figure 2. Basic Wiring Interconnection

#### FINE TRIM PROCEDURE

Connect the F/V converter as shown in Figure 3 and allow a five minute warm-up after initial power turn-on. Adjust the OFFSET ADJUST pot,  $R_0$ , for an output of 0.000V. The input terminal,  $F_{IN}$ , can be left open or tied to COM without affecting OFFSET ADJUST. Using a precision, stable frequency source connected to  $F_{IN}$  terminal, set the input frequency to 10.000kHz for model 451 or 100.000kHz for model 453. Adjust the FULL SCALE ADJUST trim pot,  $R_S$ , for an output of +10.000V.



Figure 3. Wiring Interconnection Showing Fine Adjustment Trims for Offset and Full Scale Frequency

#### ADDITIONAL TRIM CAPABILITY

Adjusting Input Threshold: The input comparator of models 451 and 453 shown in Figure 1, conditions the input signals providing protection against noisy environments as well as preventing double triggering with slow rise-time signals. Input levels up to the supply voltages,  $\pm V_S$ , will not cause damage to the input comparator.

Threshold voltage level,  $V_T$ , is internally set for both models 451 and 453 at +1.4V. Hysteresis,  $V_H$ , for model 451 is ±50mV, and ±100mV for model 453. Signals of virtually any waveshape which exceed the combined threshold and hysteresis levels,  $V_T$  $\pm V_H$ , will trigger the F/V converter. The REF terminal permits the user to conveniently adjust the input threshold over the range from 0 to ±12V to achieve optimum noise rejection or increased triggering sensitivity.

Increasing Threshold for Greater Noise Immunity: Connecting an external resistor from the REF terminal to the positive supply voltage,  $+V_S$ , increases the input threshold level above +1.4V, offering increased input noise immunity. Optimum noise immunity is generally determined by adjusting the threshold level to a point mid-way between the high and low input signal levels. For example, for a 0 to +12V input swing – representative of CMOS and HNIL logic signals – a  $17.6k\Omega$ resistor from +15V to the REF terminal results in a +6Vthreshold.



Figure 4. Increasing Threshold Above +1.4V for Greater Noise Immunity

Changes in impedance at the REF terminal result in changes to the hysteresis. Hysteresis levels can be calculated by assuming the comparator output is switching between  $\pm 12V$ . This  $\pm 12V$ signal is attenuated by a resistor-divider network formed by 12

 $R_{\rm H}$  (see Figure 1) and the parallel combination of all resistors attached at the comparator positive input. For example, with a 17.6k $\Omega$  resistor connected to the REF terminal, hysteresis becomes  $\pm 35 \, {\rm mV}$  for model 451 and  $\pm 75 \, {\rm mV}$  for model 453. The F/V converter will, therefore, trigger at +6V  $\pm 35 \, {\rm mV}$  for model 451 and  $\pm 61 \pm 100 \, {\rm m}$  for model 453.

Decreasing Threshold for Signals Less Than +1.4V: A resistor connected from the REF terminal to the negative power supply, -V<sub>S</sub>, will increase the input triggering sensitivity for operation with signals below +1.4V<sub>PK</sub>. As shown in Figure 5, a minimum threshold of zero volts is obtained with a 100k $\Omega$  resistor. The triggering level, V<sub>T</sub> ± V<sub>H</sub>, will be established by the resulting hysteresis levels. With a 100k $\Omega$  to -15V, model 451 hysteresis will be ±50mV and model 453 hysteresis will be ±60mV.

To reduce the hysteresis for greater triggering sensitivity, a  $1k\Omega$  resistor can be connected from the REF terminal to COM. Signals exceeding  $\pm 5mV$  (10mV p-p) with model 451 and  $\pm 15mV$  (30mV p-p) for model 453, will operate the F/V converter. A  $1k\Omega$  resistor from REF to COM is the minimum value recommended to reduce hysteresis and achieve reliable operation.



Figure 5. Decreasing Threshold Below +1.4V to Increase Triggering Sensitivity for Low Level Input Signals



Figure 6. Selecting External Gain Resistor RF

Adjusting Gain: Connect the FULL SCALE ADJUST terminal to the OUTPUT terminal to set the gain of model 451 at  $10^{-3}$  V/ Hz for a 10kHz full scale input frequency and the gain of model 453 at  $10^{-4}$  V/Hz for a 100kHz full scale input frequency. Connecting an external resistor from the SUM PT terminal to the OUTPUT terminal and leaving the FULL SCALE AD-JUST terminal open, facilitates gain adjustment. Model 451 can be adjusted over the range from  $10^{-1}$  V/Hz to 5 x  $10^{-4}$  V/Hz resulting in a full scale input frequency from 100Hz to 20kHz respectively. The gain of model 453 can be adjusted over the range from  $10^{-2}$  V/Hz to 5 x  $10^{-5}$  V/Hz resulting in a full scale input frequency from 1kHz to 200kHz respectively. The gain adjustment procedure is capable of increasing full scale frequency beyond the rated ranges for each model, however, nonlinearity will increase above 300ppm.

When using large values of  $R_F$  to externally set gain of the F/V converter, the output amplifier gain increases resulting in an increase in sensitivity when using the OFFSET ADJUST trim pot. For improved resolution in high gain applications ( $R_F > 1M\Omega$ ), an alternate method of trimming offset is shown in Figure 6.

Offsetting the Output: The output of models 451 and 453 can be offset over the range from -10V to +10V, enabling scale expansion for increased signal sensitivity as well as bipolar output swings up to 20V p-p.

Current introduced at the SUM PT terminal results in shifts of the output voltage directly proportional to the Offset Scale Factor, K<sub>S</sub>. For model 451, K<sub>S</sub> =  $-56\mu$ A/V and for model 453, K<sub>S</sub> =  $-45\mu$ A/V. The offset current can be generated using an external resistor from a voltage reference to the SUM PT terminal. A stable, well regulated supply voltage, such as ADI's model 904 is recommended. To shift the output positive, 0 to +10V, connect the current resistor to the negative, -V<sub>S</sub> supply. To shift the output negative, 0 to -10V, connect the current resistor to the positive, +V<sub>S</sub>, supply.

The example using model 451 illustrated in Figure 7 provides a 0 to +5V output change in response to a 5kHz to 10kHz input change. With this input, a bipolar output from -2.5V to +2.5V can be obtained by increasing the output voltage shift from -5V, ( $R_C = 53.6k\Omega$ ) to -7.5V, ( $R_C = 35.7k\Omega$ ).



#### Figure 7. Selecting External Output Offset Resistor, R<sub>C</sub>

#### SCALE EXPANSION

By combining both gain and output offset voltage adjustments, signals which exhibit a center frequency with small frequency changes, can be converted with improved resolution. Representative signals benefiting from the Scale Expansion procedure outlined below, are tachometer and frequency modulated signals. In the case of tachometer outputs, the speed is often set at an idle point and changes in output frequency represent changes in motor loading conditions. In the case of FM signals, the F/V converter can be applied such that the carrier frequency produces zero output. The resulting output voltage from the F/V converter represents the modulating signal.

Procedure for Scale Expansion: The following procedure incorporates both gain and output offset adjustments to achieve scale expansion. An example is illustrated in Figure 8 for an FM signal with a 50kHz carrier frequency and  $\pm$ 5kHz modulating signal.

1) Determine the Gain:  $G = \Delta E_O / \Delta F_{IN}$  where  $\Delta E_O$  is the total output voltage change desired in volts, and  $\Delta F_{IN}$  is the total input frequency change in Hz.

- 2) Calculate the external gain resistor,  $R_F$ ;  $R_F(\Omega) = G(1.8 \times 10^7)$ , model 451
  - $R_F(\Omega) = G(2.2 \times 10^8)$ , model 453

#### VOL. II, 12-10 V/F & F/V CONVERTERS

### **Understanding the Frequency-to-Voltage Converter Performance**

3) Calculate the Output Offset Shift,  $\Delta E_S$ , required to achieve the desired maximum output voltage,  $E_O$  (max) with the max input frequency,  $F_{IN}$  (max), and the new gain;

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 $\Delta E_S$  (volts) = G F<sub>IN</sub> (max) - E<sub>O</sub> (max)

4) Calculate the offset current resistor, R<sub>C</sub>;

$$R_{C}(\Omega) = \frac{V_{S} G}{(\Delta E_{S})(k_{s})}$$

 $k_s = 56 \times 10^{-9}$ , model 451  $k_s = 45 \times 10^{-10}$ , model 453



Figure 8. Application of Model 453 in FM Demodulation

#### **INTERFACING SIGNALS WITH DC OFFSETS > 10V**

Signals with dc levels up to  $\pm 10V$  can be directly connected to the input terminal of models 451 and 453. Capacitive coupling, as shown in Figures 9 and 10, is used for inputs with dc offsets greater than  $\pm 10V$ . The  $1M\Omega$  resistor illustrated in Figure 9 provides a dc return path to power common for the input comparator bias current. Threshold adjustments can be made following the capacitor, to set the F/V input sensitivity to match the ac signal peak-to-peak amplitude. Signals as low as 10mVp-p with model 451 and 30mV p-p model 453 are acceptable. Refer to Figures 4 and 5.

AC signals greater than  $\pm V_S$  should be attenuated with a resistive divider network following the capacitor. When large input transients ( $\geq \pm V_S$ ) are possible due to either a noisy environment or power turn-on surges, protection is provided with the addition of two diodes as shown in Figure 10.



Figure 9. Interfacing Signals With DC Offsets Greater Than  $\pm 10V$ 



Figure 10. Input Diode Protection for High Voltage Transients

#### PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale output voltage and is guaranteed for each model over the specified input range. Model 451 is rated over 1Hz to 11kHz range and model 453 is rated over 1Hz to 110kHz range. Typical nonlinearity performance is shown for all models in Figure 11.



Figure 11. Nonlinearity Error Versus Input Frequency

Gain Temperature Stability: Gain Drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range. Models 451K, 451L, 453K and 453L offer  $\pm 50$ ppm/°C maximum gain drift. Models 451J and 453J offer  $\pm 100$ ppm/°C maximum gain drift. Gain drift is typically half the guaranteed limits.

#### **OUTPUT RIPPLE**

The output contains an ac ripple signal which increases in amplitude with input frequency. Adding external capacitance in parallel with the internal filter capacitor will reduce output ripple as shown in Figures 12 and 13.



Figure 12. Output Ripple Versus External Filter Capacitor (C<sub>F</sub>) - Model 451



Figure 13. Output Ripple Versus External Filter Capacitor (C<sub>F</sub>) - Model 453

#### SETTLING TIME

Increasing the external filter capacitor to reduce output ripple will increase the settling time to step changes in frequency occurring at the input. Figure 14 shows curves of settling time to  $\pm 0.5\%$  of final value for both increasing and decreasing full scale step changes. As C<sub>F</sub> increases in value, the total filter time constants for models 451 and 453 approach equal values, resulting in identical settling time.



Figure 14. Settling Time Versus External Filter Capacitor

#### APPLICATIONS IN PROCESS CONTROL SYSTEMS

#### MOTOR CONTROLLER

In making rpm measurements, transducers are often encountered that have pulse-train outputs from variable-reluctance magnetic pickups (in which the output frequency is a function of rpm). These low level signals are generally in the range of 0 to 200mV peak. The adjustable input threshold feature of models 451 and 453 enables direct connection to low level transducers, offering simple, reliable interfacing.

The motor speed control and monitoring application shown in Figure 15 illustrates the F/V converter applied in a closed loop control system. R1 sets the threshold to +60mV with  $\pm 50mV$  hysteresis for model 451.

The +20mA output current capability of both models 451 and 453, enables direct interface to low impedance loads, up to  $500\Omega$ , such as analog meters or relays.



Figure 15. Application of F/V Converter to Control and Monitor Motor Speed in Closed Loop System

#### SPEED SWITCH

With the addition of a low cost comparator and relay, the F/V converter provides a reliable approach to controlling heavy



Figure 16. Application of F/V Converter to Control Load Power

#### VOL. II, 12-12 V/F & F/V CONVERTERS

generator loads after the generator has reached a specified speed. As shown in Figure 16, the relay will remain open until the output from the F/V converter reaches a preset POWER ON trip level. The F/V output signal is linearly related to the speed of the motor, permitting precise control of the POWER ON set point.

#### APPLICATION IN INSTRUMENTATION SYSTEMS

#### **FREQUENCY MONITORING**

Small input frequency changes can be monitored more readily by using the programmable gain feature of models 451 and 453 to achieve greater signal sensitivity. In the application of model 451 illustrated in Figure 17, gain has been set to 0.1V/ Hz, resulting in a 100Hz full scale frequency range. The output resolution for small changes occurring in the 60Hz line frequency has been improved. An additional advantage of this approach is the reduced accuracy and stability requirements placed on the relay trip levels, set by the voltage levels at the comparators. A precision voltage reference supply is not required.

Since both models 451 and 453 tolerate input signals up to the supply levels,  $\pm V_S$ , costly input protection is eliminated in most applications.



Figure 17. Application of F/V Converter to Monitor 60Hz Line Frequency

#### APPLICATION IN DATA ACQUISITION SYSTEMS

#### HIGH NOISE IMMUNITY TRANSMISSION

F/V converters are excellent companion products to V/F converters for use in low cost, two wire data transmission systems. As shown in Figure 18, this V/F/V approach utilizes the continuous self-clocking feature of the V/F converter thereby eliminating the need for costly additional twisted pair cable for external synchronization. Model 610 instrumentation amplifier amplifies the low level differential transducer signal to the 10V full scale of models 450 and 456 10kHz V/F converters. A differential line driver is used to drive a twisted pair cable through a noisy environment. A differential line receiver is used to drive model 451 10kHz F/V converter. The low cost of the V/F and F/V converters in addition to the simple twisted pair cabling approach make it economical to use a V/F/V converter pair for each channel in a data acquisition system.



Figure 18. Application of F/V Converter in a Low Cost, High Noise Rejection Two-Wire Data Transmission System

### ANALOG High DEVICES V(

# High Accuracy, 100kHz and 1MHz Voltage to Frequency Converters

# **MODELS 458 and 460**

#### FEATURES

High Stability: 5ppm/°C max, Model 458L 15ppm/°C max, Model 460L High Linearity: ±0.01% max at 100kHz, Model 458 ±0.015% max at 100kHz, Model 450 Versatility: Differential Input Stage Voltage and Current Inputs Floating Inputs: ±10V CMV Wide Dynamic Range: 6 Decades, Model 460 TTL/DTL Compatible Output

#### APPLICATIONS

Fast Analog-to-Digital Converter High Resolution Optical Data Link Ratiometric Measurements 2-Wire High Noise Immunity Digital Transmission Long Term Precision Integrator

#### **GENERAL DESCRIPTION**

Models 458 and 460 are high performance, differential input, voltage to frequency modular converters designed for analog to digital applications requiring accuracy and fast data conversion. Model 458 offers a 100kHz full scale frequency, guaranteed nonlinearity of  $\pm 0.01\%$  maximum over five decades (1Hz to 100kHz) of operation and guaranteed low maximum gain drift in three model selections; model 458L: 5ppm/°C max; model 458K: 10ppm/°C max; and model 458J: 20ppm/°C max. Model 460 offers a 1MHz full scale frequency, guaranteed maximum nonlinearity of  $\pm 0.015\%$  over six decades (1Hz to 1MHz) of operation and guaranteed low maximum gain drift in three selections; model 460L: 15ppm/°C max; model 460K: 25ppm/°C max; and model 460J: 50ppm/°C max. Model 460L is the industry's first 1MHz V/F converter to offer 15ppm/°C maximum gain drift.

The differential input stage of models 458 and 460 provide the versatility of either direct interface to off-ground 0 to +11V input signals with common mode voltages (CMV) to  $\pm$ 10V, as well as ground referenced positive, 0 to +11V or negative, 0 to -11V signals. Both models also accept positive current signals: 0 to +0.5mA, model 458; 0 to +1mA, model 460 for current to frequency (I/F) applications.

The rated performance of both models 458 and 460 is achieved without the need for external components or adjustments. Optional adjustments are available for trimming full scale frequency and the input offset voltage.

#### WHERE TO USE MODELS 458 AND 460

The combination of low gain drift, low nonlinearity and the versatility of a differential input with both high speed (100kHz/1MHz) models, offer excellent solutions to a wide variety of demanding applications; in high speed remote data acquisition systems – two wire data transmission over long



wires; in 5½ digit DVM's – featuring high resolution A/D conversion, monotonic performance, no missing codes and high noise rejection; in strain gage bridge weighing applications – accurate ratiometric measurements over wide dynamic range.

#### **DESIGN APPROACH - PRECISION CHARGE BALANCE**

Models 458 and 460 incorporate a superior charge balance design that result in high linearity and temperature stabilitysee Figure 1. Both models accept unipolar, single-ended voltage or current input signals directly. By offsetting the input using the current terminal, models 458 and 460 will accept bipolar input voltages up to  $\pm 5V$ .



Figure 1. Block Diagram - Models 458, 460

# **SPECIFICATIONS** (typical @ +25°C and VS = ±15V dc unless otherwise noted)

	100kHz Full Scale 458	IMHz Full Scale 460			
MODEL	JKL	JIKIL			
TRANSFER FUNCTION					
Voltage Input	$f_{ours} = (10^4  \text{Hz/V})  f_{rs}$	$f_{our} = (10^5 \text{Hz/V}) \text{ cm}$			
Current Input	$f_{OUT} = (2 \times 10^5 \text{Hz/mA}) i_{IN}$	$f_{OUT} = (10^{6} \text{Hz/mA}) i_{TN}$			
ANALOG INPUT					
Configuration	Differential	Differential			
Voltage Signal Range		· · · · · · · · · · · · · · · · · · ·			
$e_{IN}$ Terminal ( $e_{REE} = 0$ )	0 to +10V dc min	0 to +10V dc min			
$e_{\rm REF}$ Terminal ( $e_{\rm IN} = 0$ )	0 to -10V dc min	0 to -10V dc min			
Differential (e <sub>IN</sub> - e <sub>REF</sub> )	0 to +10V dc min	0 to +10V dc min			
Overrange	+10% min	+10% min			
Current Signal Range (i <sub>IN</sub> )	0 to +0.5mA min	0 to +1mA min			
Common Mode Voltage					
Impedance e Terminel	400B	400B			
come Terminal	4040	10k32			
in, Terminal	00	00			
Max Safe Input	±Ve	±Ve			
ACCURACY	······································				
Warm Up Time	5 Seconds to 0.01%	2 Minutes to 0.02%			
Nonlinearity, $e_{IN} = +0.1 \text{mV}$ to $+11 \text{V}$	±0.01% of Full Scale, max	±0.015% of Full Scale, max			
$e_{IN} = -0.1 \text{mV}$ to $-11 \text{V}$	±0.01% of Full Scale	±0.015% of Full Scale			
Full Scale Error <sup>1</sup>	+0.1% to +2%, max	+0.1% to +2%, max			
Gain vs. Temperature (0 to +70°C)	±20ppm/°C max   ±10ppm/°C max   ±5ppm/°C max	±50ppm/°C max   ±25ppm/°C max   ±15ppm/°C max			
vs. Supply Voltage	±15ppm/%	±25ppm/%			
vs. Time	±5ppm/day, ±25ppm/month	±10ppm/day			
Input Offset Voltage <sup>2</sup>	±10mV max	±10mV max			
vs. Temperature (0 to +70°C)	$\pm 30 \mu V/C max$	$\pm 30\mu V/C max$			
vs. Supply Voltage	$\pm 10\mu V/\%$	$\pm 10\mu V/\%$			
vs. 1ime	$\pm 2\mu V/day, \pm 20\mu V/month$	±10ppm/day			
RESPONSE					
Settling Time, ±0.01% +10V Step	3 Output Puises Plus 2µs	2 Output Puises Plus 2µs			
	Toms	1ms			
FREQUENCY OUTPUT'					
Waveform	TTL/DTL Compatible Pulses	TIL/DIL Compatible Pulses			
Pulse width Bigs and Eall Time	5µs	Souns Sound Sound			
Pulse Polarity	Positive	Positive			
Logic "1" (High) Level	+2.4V min	+2.4V min			
Logic "0" (Low) Level	+0.4V max	+0.4V max			
Capacitive Loading	500pF max	200pF max			
Fan Out Loading	10 TTL Loads min	10 TTL Loads min			
Impedance	3kΩ (High State)	670Ω (High State)			
POWER SUPPLY <sup>4</sup>		,			
Voltage, Rated Performance	±15V dc	±15V dc			
Voltage, Operating	±(13 to 18)V dc	±(13 to 18)V dc			
Current, Quiescent	(+25, -8)mA	(+25, -8)mA			
TEMPERATURE RANGE					
Rated Performance	0 to +70°C	0 to +70°C			
Operating	-25°C to +85°C	-25°C to +85°C			
Storage	-55°C to +125°C	~55°C to +125°C			
MECHANICAL					
Case Size	2" x 2" x 0.4"	2" x 2" x 0.4"			
Weight	45 Grams	45 Grams			
Mating Socket	AC1010	AC1010			

NOTES <sup>1</sup>Adjustable to zero using 500Ω potentiometer. <sup>3</sup>Adjustable to zero using 50kΩ potentiometer. <sup>3</sup>Protected for continuous short-circuits to ground and momentary (less than 1 sec) shorts to the +V<sub>S</sub> supply. Output is not protected for shorts to the -V<sub>S</sub> supply. <sup>4</sup>Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

### **OUTLINE DIMENSIONS** Dimensions shown in inches and (mm).





**MATING SOCKET: AC1016** 

### Applying the Voltage to Frequency Converter

#### **VOLTAGE TO FREQUENCY OPERATION**

Models 458 and 460 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to digital processing circuits.

#### **BASIC V/F HOOK-UP AND OPTIONAL TRIMS**

Models 458 and 460 can be applied directly to achieve rated performance without external trim potentiometers or other. components. Figures 2, 3 and 4 below illustrate the basic wiring connections for either V/F converter model. Using the basic hookup without trims, full scale ( $e_{IN} = 10V$ ) accuracy is +0.1% to +2% and the input offset voltage is ±10mV max. The full scale and input offset voltage errors can be eliminated by using the FINE TRIM PROCEDURE.

#### FINE TRIM PROCEDURE

Connect the optional trims as shown in Figure 2, 3 or 4 and allow a five minute warm-up after initial power turn-on. Using a precision, stable voltage source, set the input voltage,  $e_S$ , to 10mV. Adjust the OFFSET trim,  $R_O$ , for an output pulse interval of 0.01 sec (model 458) or 0.001 sec (model 460).



Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse frequency of 100kHz (model 458), or 1MHz (model 460). The V/F converter may now be used without further adjustment.

#### DIFFERENTIAL INPUT

The  $e_{IN}$  and  $e_{REF}$  input terminals represent a true differential input capable of accepting a signal from a strain gage bridge, a balanced line, or a signal source sitting at a common mode voltage. The differential input eliminates the need for a differential amplifier to handle these signals.

To apply the 458 or 460 voltage inputs differentially, the  $e_{IN}$  pin must always be positive with respect to the  $e_{REF}$  pin as shown in Figure 4. The differential signal source may be completely floating with common mode voltages up to  $\pm 10V$  max. For differential inputs the output frequency is:

$$F_{OUT} = \left[\underbrace{(e_1 - e_2)}_{INPUT} + \left(\frac{e_1 + e_2}{2}\right) \times \left(\frac{1}{CMR}\right)\right] K_g$$
  
SIGNAL

 $K_g = 10^4 Hz/V$ ; model 458 10<sup>5</sup> Hz/V; model 460

#### OFFSETTING INPUT FOR BIPOLAR INPUTS

The input summing terminal,  $+i_{IN}$ , may be used to improve dynamic response as well as scale the output frequency to directly convert bipolar input voltages. An offset current is fed through an external resistor from a stable voltage reference. As shown in Figure 5, input voltages of  $\pm 5V$  min can be converted directly.



Figure 5. Offsetting Input to Accept ±5V Bipolar Inputs

The output may also be scaled up so that low amplitude signals, such as 1V will give full scale output frequency; 100kHz model 458 or 1MHz model 460. By scaling the output frequency for low level signals, the step response will significantly improve. As shown in Figure 6 for model 458, the step response for a 1 volt input decreases from 200 $\mu$ s before input scaling, to 20 $\mu$ s with scaling.



Figure 6. Offsetting Input to Achieve Improved Dynamic Response for Small Signal Inputs

#### PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale input and is guaranteed over the 0.1mV to 11V operating signal range; ±0.01% max, models 458J/K/L, ±0.015% max, models 460J/K/L. Typical nonlinearity performance is illustrated in Figure 7.



Figure 7. Nonlinearity Error Versus Input Voltage

Gain Temperature Stability: Gain drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range; 5ppm/°C (458L), 10ppm/°C (458K), 20ppm/°C (458J), 15ppm/°C (460L), 25ppm/°C (460K) and 50ppm/°C (460J) max.

#### LONG TERM PRECISION INTEGRATOR

In critical measurement applications, such as pollution monitoring where it is required to integrate for periods greater than 1 hour with overall accuracy of 0.05%, the V/F converter offers a superior low cost approach when compared to the traditional operational integrator circuit. As shown in Figure 8, the analog signal is applied to a precision input amplifier, model 52K and then to the V/F input. The V/F output is connected to a large capacity counter and display, operating as a totalizer. The total pulse count is equal to the time integral of the analog input signal. Since the output displayed is an accumulated pulse count, there is no integrator drift error. A feature of this approach is the infinite hold capability without errors due to time drift, since the counter may be held at any time without affecting the output reading.



Figure 8. Models 458/460 as Long Term Integrator with Arbitrary Display Calibration. Frequency Division Ratio can Otherwise be Chosen to Provide Direct Readout in any Desired Units.

#### **CMOS/HNIL COMPATIBLE OUTPUT**

The circuit shown in Figure 9 may be used to shift the output of the 458/460 from 0 to +5V to 0 to +12V, to provide a 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic.



Figure 9. Circuit for Shifting the Output of the 458/460 to Drive CMOS/HNIL Logic

#### PRECISION HIGH CMV ANALOG ISOLATOR

By combining the V/F converter with a floating power supply and optical isolator as shown in Figure 10, accurate low level measurements in the presence of high common mode voltages may be achieved. Only the CMV rating of the optical isolator and the breakdown rating of the power supply limit the CMV rating. Using this approach for isolating transducers, ground loop problems are eliminated. Cost and complexity are minimized since only a single optical isolator is required to couple the serial pulse output from the V/F to the digital réadout.



Figure 10. Optical Isolation Using LED Photo Isolator to Provide Up to 1500V dc CMV Isolation

#### APPLICATION IN DATA ACQUISITION SYSTEMS

High Noise Immunity Data Transmission: A method of accurately transmitting analog data through high noise environments is illustrated in Figure 11. This approach utilizes the self clocking output of models 458 and 460 and eliminates the need for costly additional twisted pair for external synchronization. Model 610 amplifies the low level differential transducer signal up to the 10V full scale V/F input level. A differential line driver is used to drive a twisted pair cable. The differential line driver and receiver offer high noise immunity to common mode noise signals.



Figure 11. Application of Model 458 V/F Converter in a High Performance, High Noise Rejection Two-Wire Data Transmission System

# Synchro & Resolver Converters

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Inductosyn is a registered trademark of Farrand Industries, Inc. MULTIBUS is a registered trademark of Intel Corporation.

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# **Selection Guide** Synchro & Resolver Converters

The products in this section are generally concerned with angular measurements. They include the following classes of device:

Digital Angle to Trigonometric (sine-cosine) Analog Voltage Digital-to-Resolver Converters Digital-to-Synchro Converters Inductosyn<sup>TM</sup>-to-Digital Converters Resolver-to-Analog Voltage Converters **Resolver-to-Digital Converters** Resolver-to-Digital Display (Angular-Position Indicators) Synchro-to-Analog Voltage Converters Synchro-to-Digital Converters Synchro-to-Digital Display (Angular-Position Indicators)

Complete descriptions, specifications, and applications information on the products in this section can be found in the data sheets. Brief general information can be found overleaf.

The Selection Guide is provided to ease the job of finding the right unit to do your job. Devices are listed in the Selection Guide vertically, by model number, in alphabetic, then numeric order, as well as by function and type of input. Salient characteristics are listed horizontally. A bullet is placed at each intersection that is appropriate for each device.

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RES	SYNCHRO	Angle Position Indicator	API1620 API1718	•	:			:				:				
libe	DIGITAL	Digital to Synchro Resolver	DSC1705 DSC1706 DRC1745 DRC1746	•	•			•				•	•	•		
		Digital to Trig. (Analog)	DRC1765 DRC1766 DTM1716 DTM1717		•••••••••••••••••••••••••••••••••••••••		••••••	••				•	•	•		
	INDUCTOSYN INPUT	Inductosyn/ Resolver to Digital	IRDC1730 IRDC1731 IRDC1732 IRDC1733 1S20 1S40 1S60 1S61		•	•••••		•	402 7997 9666 9209		-1130 7753 7753 7753			•••		
RES	OLVER INPUT	Resolver to Digital Converters	RDC1740 RDC1741 RDC1742		•			•					•	•		
		Sync/Resolver Analog Synchro or Resolver to BCD Converters	SBCD1752 <sup>1</sup> SBCD1752 <sup>1</sup> SBCD1753 <sup>2</sup> SBCD1756 <sup>1</sup> SBCD1757 <sup>2</sup>	•			•		•	•			•1 •2 •1 •2			
		Synchro or Resolver to Binary	SDC1700 SDC1702 SDC1704 SDC1721 SDC1725 SDC1726	•	•		-	•				•	, <b>•</b>	•	•	
sy	NCHRO INPUT	Synchro to Digital	SDC1740 SDC1741 SDC1742	•				•					•	:		

13-Bit BCD plus sign

214-Bits BCD

s DD. syn is a registered trademark of Farrand Industries Inc. ; indicates new products since publication of 1982-1983 Databook Update.

Here's an example of its use: if you were looking for a 14-bit digital-to-resolver converter with the highest accuracy in the smallest package, you might start at the 14-bit column; you would see that there are two resolver families that have 14-bit resolution and error less than 5 arc-minutes: DRC1745 and DRC1705; the DRC1745 is a hybrid, and the DRC1705 is in a >0.4'' module. Thus, you would be quickly led to look at the DRC1745 data sheet and be guided to its location by the page number at the right.

In addition to the devices listed in the chart, data sheets for the following accessory products are also to be found in this section:

Resolver and Synchro 5VA Output Transformers, models RTM/STM1686/1696/1736/1687/1697/1737

Synchro/Resolver 5VA-Output Power Amplifier, model SPA1695

Two-Speed Processor for Coarse/Fine Synchro/Resolver Systems, model TSL1612

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# **Orientation** Synchro & Resolver Converters

These products constitute a complete line of devices for the digital measurement and control of angular and linear displacements by means of synchros, resolvers, and Inductosyns. In addition to modules and hybrid circuits that perform the appropriate conversions, the line also includes modules that perform purely algebraic or logical functions; in some cases, solid-state circuitry emulates the functions of electromechanical devices.

The range of synchro processing modules now available covers a wide area of application. They are widely used in military and radar applications, but there are additional fields in which they could be used to advantage because of the proven ruggedness and high precision of the electromechanical hardware, their standardized specifications, and their low cost. They have a number of advantages over potentiometers and optical systems.

In this introductory section, there will be provided a brief set of device definitions. Detailed data and applications information is given in the data sheets. For a complete introduction to synchro/digital conversion, Analog Devices has available a 208page book, *Synchro and Resolver Conversion*, edited by G. Boyes (1980), \$11.50.

In this section, and in much of the text, the word "Synchro" appears frequently. In many cases, the word "Resolver" could be used in its place. The modules make use of angular data in resolver form, if the input data is in three-wire synchro form, transformers in "Scott T" configuration convert it to resolver form; analog outputs are available in both forms. There are a number of voltage and frequency options.

#### REPRESENTATION OF ANGLES IN DIGITAL FORM

#### Binary

The most commonly used method of representing angles in digital form is simple natural binary weighting, where the mostsignificant bit (MSB) represents 180°, the next represents 90°, etc. The table shows the bit weights in degrees, degrees-andminutes, and radians for this coding method.

#### BCD

When angular measures have to be displayed in visual form, BCD coding is used, through the use of binary-to-BCD converters, such as the BDM1615, which provides the necessary scaling and conversion, e.g., from 1010000000000 ( $180^{\circ}$ + 45°) to 10 0010 0101.0000 000 (or 225.00°).

#### **TYPICAL S/D/S DEVICES**

Binary-to-Binary-Coded-Digital Converter (BDM1615/16/17) A device that accepts angular data in binary form and converts it to BCD form, with fractional degrees in decimal fractions of  $1^{\circ}$  (1615, 1617) or minutes and seconds (1616). The BCD output is modulo 360°.

Bit No.	Degrees	Degrees,	minutes	Radians
1	180	180	0	3.141593
2	90	90	0	1.570796
3	45	45	0	0.785398
4	22.5	22	30	0.392699
5	11.25	11	15	0.196349
6	5.625	5	37.5	0.098175
7	2.8125	2	48.75	0.049087
8	1.40625	1	24.38	0.024544
9	0.70312	0	42.19	0.012272
10	0.35156	0	21.09	0.006136
11	0.17578	0	10.55	0.003068
12	0.08789	0	5.27	0.001534
13	0.04395	0	2.64	0.000767
14	0.02197	0	1.32	0.000383
15	0.01099	0	0.66	0.000192
16	0.00549	0	0.33	0.000096

#### Digital-to-Synchro Converters (DSC1705/06)

Devices that accept parallel binary digital inputs (14 or 12 bits) and an ac reference signal, and provide outputs in 3-wire synchro form.

#### Inductosyn/Resolver-to-Digital Converter (IRDC1730)

A device that produces a digital output capable of resolving (to 12 bits) intermediate distances within a single track-pitch of a Farrand linear-Inductosyn stator in displacement- and angle-measuring Inductosyn systems. The moving element is used as though it were a resolver input; hence the device will also convert resolver information to digital.

#### Synchro-to-Digital Converter

A device that accepts either 3-wire synchro- or 4-wire resolver inputs, together with a 2-wire ac reference, and outputs angular binary data in a continuously tracking mode, employing a Type 2 servo loop. The inputs may be from either remote synchros or from electrically simulated synchros (e.g., DSC's).

### Digital Converter and Processor for Two-Speed Synchros (TSL1612)

A two-speed processor takes as inputs two sets of digital information, representing the angles from coarse and fine synchros, and combines them to produce a single 19-bit word representing the actual angle of the "coarse" shaft. The TSL consists of the processing logic alone—it can be used with a pair of SDC's, which provide the two sets of digital information.



# Synchro/Resolver Angle Position Indicators and Digital Converter

### API1620 and API1718

#### FEATURES

Five Digit Display Accuracy 0.02° (API1620) or 2 arc-minutes (API1718) Two Channel Input Accepts High or Low Level Synchros, Resolvers or Magslips 47Hz to 600Hz Carrier Frequency 16-Bit BCD or Natural Binary Output Storage Compartment for Leads/Connectors

#### **API1620 FEATURES**

Degrees and Decimal Parts of a Degree Display Display Test Facility Full Scale 359.99°

#### API1718 FEATURES

Nato Codified Degrees and Minutes Display Display Latch Facility Full Scale 359° 59'

#### DESCRIPTION

The Angle Position Indicators API1620 and API1718 are instruments for displaying in visual digital form the angle represented by synchro, magslip or resolver signals. In addition to displaying the angle in visual form the APIs also convert the input angular signals into natural binary or BCD angular data at TTL levels for use externally. Facility is provided for the connection of two sets of input signals which may be alternately switched into the converter. The APIs have been designed to accommodate input signals from all the usually encountered angular data transmission systems i.e., Synchros, Magslips and Resolvers at both high and low voltage levels and at frequencies from 47Hz to 600Hz. The two sets of inputs to the APIs can be different e.g., a 60Hz synchro on one input together with a 400Hz resolver on the other. The facility of switching from one set of inputs to the other enables the angular position of separate devices to be directly compared. The meters have been designed to work with any reference voltage from 6V rms to 115V rms.

#### STORAGE COMPARTMENT

A storage compartment for storing the input leads and connectors is provided on the underside of the instrument, access to this is by an easily operated slotted screw fastener. The API is delivered with part of the Application Kit stored in this compartment.

#### SELF TESTING

Both Angle Position Indicators have a self checking facility. This is provided by internally simulated input angles of  $45^{\circ}$  and  $225^{\circ}$  selected by the front panel mode switch. The simulated angles have an accuracy an order of magnitude greater than the Instrument.



#### NATO CODE NUMBER

The API1718 BCD option has been issued with a Nato Stock Number, 6625-99-539-8389, which eases acceptance of the Angle Position Indicator in military applications.

#### MODELS AVAILABLE

The two Angle Position Indicators described in this data sheet differ primarily in the format of the display and the presence of a Display Check or Display Latch facility.

<u>Model API1620</u> has a display format of degrees and decimal parts of a degree with a full scale range of  $359.99^{\circ}$  and an accuracy of  $0.02^{\circ}$ . It has a display check facility on the front panel and is available in two options, viz.

<u>BINARY option</u> has 16-bit representation at TTL levels of the input angular signal in natural binary form on the rear connector.

<u>BCD option</u> has a 5 decade BCD representation at TTL levels of the input angular signal on the rear connector.

<u>Model API1718</u> has a display format of degrees and minutes with a full scale range of 359° 59 minutes and an accuracy of 2 arc minutes. It has a display latch facility on the front panel and is available in two options, viz.

<u>BINARY option</u> has a 16-bit representation at TTL levels of the input angular signal in natural binary form on the rear connector.

<u>BCD option</u> has a 5 decade BCD representation at TTL levels of the input angular signal on the rear connector.

# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Models	API1620	API1718
ACCURACY <sup>1</sup>	±0.02° at 400Hz ±0.03° at 60Hz	2 arc minutes at 400Hz 3 arc minutes at 60Hz
ANGULAR RANGE	000.00° to 359.99° continuous rotation	000.00° to 359° 59 minutes continuous rotation
TEMPERATURE RANGE	Operational 0 to +50°C Storage -5°C to +55°C	•
INPUT SIGNAL VOLTAGE	11.8V rms 200Hz to 600Hz 26.0V rms 200Hz to 600Hz 90.0V rms 47Hz to 600Hz	•
REFERENCE VOLTAGE	6V rms to 115V rms with no adjustments required	*
REFERENCE FREQUENCY	47Hz to 600Hz	•
INPUT IMPEDANCE	Signal 2M $\Omega$ Reference 200k $\Omega$	*
TOLERANCE ON SIGNAL TO REFERENCE PHASE	±20°	•
DISPLAY	5 digit, dot matrix LED	*
DATA OUTPUT (TTL) ON REAR CONNECTOR (BCD 2TTL Loads, Binary 3TTL Loads)	Either 5 decade BCD or 16-bit natural binary. Degrees and decimal parts of a degree format.	•
INHIBIT INPUT (TTL) (1TTL LOAD)	Logic "0" = Hold Logic "1" = Track	*
BUSY OUTPUT (TTL) (10TTL LOADS)	Logic "0" = Data Stable Logic "1" = Busy	•
POWER SUPPLY	23VA (typ), 28VA (max) at either 115V rms or 220V rms ±15% 47Hz to 400Hz	•
WEIGHT	10 lbs 4.53Kgm	*
SIZE (EXCLUDING HANDLE)	$11.75'' \times 8'' \times 4''$ (300mm × 204mm × 102mm)	•
NATO STOCK NO.	_	6625-99-539-8389 (BCD version only)

#### NOTES

\*Specifications same as API1620.

applied (all lines varying together). The input amplifier limits are set at +15% of the nominal voltage levels, no damage will occur if 90 volts is applied on the 11.8 volts or 26.0 volt settings and up to 150 volts can be applied on the 90 volts setting without damage. For voltages considerably lower than the normal voltages the API will continue to function at a reduced accuracy; the inaccuracy will manifest itself mainly as an hysteresis error.

Specifications subject to change without notice.



Front Panel of the API1620



Front Panel of the API1718

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#### DATA READOUT

The digital angle readout is displayed on a five digit display by Light Emitting Diode (LED) dot matrix indicators on the front panel.

The API1620 model displays this angle as degrees and hundredths of a degree.

The API1718 model displays this angle as degrees and minutes.

The displayed angle is also available at TTL levels in either Binary or BCD format on the rear connector. In both APIs this angle is produced in degrees and hundredths of a degree.

#### **DISPLAY CHECK (API1620)**

The API1620 has a display check press button on the front panel which when pressed causes all the dots in all LED matrices to be illuminated.

#### POWER CONNECTIONS

The Angle Position Indicators can be powered from 115V ac or 220V ac  $\pm 15\%$ , the changeover switch being on the front panel. The supply frequency can be 47Hz to 400Hz.

#### **DISPLAY LATCH (API1718)**

The API1718 has a Display Latch button on the front panel which when pressed will hold the display at its existing reading —but does not effect the digital output data.

Both APIs have a latch facility available on Pin 36 on the rear connector. This "INHIBIT" input will "Freeze" both the display and the digital output data if a Logic "0" is applied.

#### **OUTPUTTING VALID DATA**

A "Converter Busy" pulse is available on Pin 37 of the rear connector, which indicates the state of the converter. When this line is at Logic 1 the converter is busy and the data is changing. A Logic 0 indicates that the data is valid.

Data can be transmitted without error under the following timing sequence.



Data Transfer Waveforms

#### DATA OUTPUT CONNECTIONS AND BIT WEIGHTS

The APIs are available in two forms one giving the output in BCD form and the other giving the output in natural binary form. In both cases the resolution corresponds to 16-bits binary. The pin connections for the 37 way DCM 37S Souriau rear connector are given in the following table.

#### **OPERATING NOTES**

The line voltage selector switch must be set in the correct

PIN	NATURAI	. BINARY VERSION	BCD VERSION
NUMBER	BIT NO.	BIT WEIGHT	CODING
1	GR	OUND	GROUND
2	16	0.0055	0•01°
3	15	0.0110	0.02°
4	14	0.0220	0•04°
5	13	0.0439	0•08°
6	12	0.0879	0•10°
7	11	0.1758	0•20°
8	10	0.3516	0•40°
9	9	0.7031	0.80°
10	N/C		1.0°
11	N/C		2•0°
12	8	1•4063	4•0°
13	7	2.8125	8.0°
14	6	5.6250	10·0°
15	5	11.2500	20•0°
16	4	22.5000	40·0°
17	3	45.0000	80•0°
18	2	90:0000	100•0°
19	1	180.0000	200•0°
20	N/C		N/C
TO	••		TO↓
35	N/C		N/C
36	INHI	JIT I	NHIBIT
37	BUS	Y	BUSY

#### Connections on Output Connector at rear of API

position before the power is applied. To the left of the voltage selector switch is the instrument "on/off" press button and to the left of that is the power indicator neon.

#### SIGNAL VOLTAGE SELECTOR SWITCH

The three position selector switch alters the transformers to suit the synchro or resolver voltages being applied to the API. THIS SWITCH SHOULD BE SET IN THE 90 VOLT POSI-TION DURING 45° OR 225° CHECKING, no damage will be done if this or any of the switches are in wrong positions but errors in checking could occur.

#### MODE SELECTOR SWITCH

This mode selector switch marked M, S, R,  $45^{\circ}$ ,  $225^{\circ}$  meaning Magslip, Synchro, Resolver,  $45^{\circ}$  check and  $225^{\circ}$  check is for making appropriate changes according to whether a magslip synchro or resolver is being used. If two differing systems are being applied to the inputs e.g. Channel 1 resolver at 26V and Channel 2 synchro 90V, then the mode switch will have to be changed from R to S and the voltage switch from 26V to 90V when changing from Channel 1 to Channel 2. No damage will be done to the API by any order of switching but some change of loading on the inputs may occur. To avoid this problem the channel switch marked CH1, OFF, CH2 should be set in the OFF position when changing the mode and voltage switches.

#### DIRECTION OF DATA ROTATION

The convention of zero angle on Magslips differs from Synchros by  $150^{\circ}$ . Correction for this has been made inside the APIs, so that zero degrees will be indicated on the API for both Synchro and Magslips set to zero. The direction of rotation convention is different for Synchros and Magslips this has not been changed so that a clockwise rotation (from zero) of the synchro will give the same reading as an anticlockwise rotation (from zero) of a Magslip.



Schematic Arrangement of the API1620 and API1718

#### **REFERENCE INPUT**

Both the Angle Position Indicators require a reference voltage to be supplied via the input connectors. This must be the same reference as supplied to the devices under test and can be any voltage from 6V rms 115V rms.

#### POWER AND SIGNAL INPUT CONNECTIONS

The power and input connectors have lettered pins (see table on previous page). Connections are:

#### Power

Fixed Connector: Amphenol 62GB-57A-8-3.3P Free Connector: Amphenol 62GB-16F-8-3.3S

3 Way:	Pin A	Ground
	Pin B	Live
	Pin C	Neutral

#### Inputs

Fixed Connector: Amphenol 62GB-57A-10-6P Free Connector: Amphenol 62GB-16F-10-6S

6 Way:	Pin A to S1	Pin D to S4
	Pin B to S3	Pin E to Ref High
	Pin C to S2	Pin F to Ref Low

For resolver inputs the sine voltage is applied to S1 and S3 and the cosine to S2 and S4. The phase of the resolver connections should be such that if S3 and S4 and Ref Low are regarded as common then in the first angular quadrant 0 to 90° the voltages on S2 and Ref High will be in time phase, i.e., positive together and negative together and the voltages on S1 and Ref High will be 180° out of time phase. For synchro or magslip operation the connections should be made to S1, S2 and S3 in rotation.



Pin Connections as Viewed Looking at the Front of the API1620 and API1718

APPLICATIONS OF THE ANGLE POSITION INDICATOR The API finds many applications in both civil and military systems where it is common place to use synchro or resolver angular data transmission. In many areas of mechanical engineering where angular settings have to be made to high accuracies, the APIs can be used with a precision synchro to display the shaft angle—or by using both inputs to compare shaft angle settings.

Other examples of the API's applications are checking constant velocity, coupling (universal joints) and measuring nonuniformity in the gearing velocity of gear boxes. By converting the digital output data to printers, permanent records can be obtained.

#### FUSES

The API1620 is protected by a 300mA anti-surge fuse in the fuse holder in the rear panel. The API1718 has two 160mA anti-surge fuses located on the rear panel for 240V operation. When used at 115V the 300mA fuses supplied should be fitted.

#### **ORDERING INFORMATION**

The APIs should be ordered according to the following:

API1620/BCD	degrees and hundredths display. BCD digital data output on rear connector.
API1620/BIN	degrees and hundredths display. Binary digital data output on rear connector.
API1718/BCD	degrees and minutes display. BCD digital data output on rear connector. Nato Code: 6625–99–539–8389.
API1718/BIN	degrees and minutes display. Binary digital data output on rear connector.

The API1620 is supplied with the following applications kit: 2 input connectors Amphenol sockets type 62GB-16F10-6S, 1 mains lead with Amphenol socket type 62GB-16F8-3.3S attached, one 37 way DCM37S Souriau connector with cover and spring clip. 1 Users Handbook. Calibration Result Sheet.

The API1718 is supplied with the following applications kit: 2 input leads with Amphenol socket type 62GB-16F10-6S attached. (Nato stock number 6625-99-541-3454). 1 mains lead with Amphenol socket type 62GB-16F8-3.3S attached. (Nato stock number 6625-99-541-3453). One 37 way connector DCM37S/Souriau connector with cover and spring clip. 1 Users Handbook. 3 Spare fuses (one 160mA anti-surge, two 300mA anti-surge). Calibration result sheet.

# **ANALOG** DEVICES

# Digital-to-Synchro Converters

# DSC1705/1706

#### FEATURES

Very Low Radius Vector Variation (Transformation Ratio) (±0.1%) High Accuracy (±2 arc-mins at +25°C) 12- or 14-Bit Resolution No 5 Volt Power Supply Required MIL Spec/Hi Rel Versions Available Internal 1.3VA Amplifiers Internal Transformers (400Hz Option) No Trims or Adjustments Necessary

#### APPLICATIONS

Driving Control Transformers Driving Torque Receivers (with External Amplifiers) Servo Mechanisms Retransmission Systems Positional Control

#### GENERAL DESCRIPTION

The DSC1705 and DSC1706 are Digital-to-Synchro and Digitalto-Resolver converters capable of driving electromechanical loads of up to 1.3VA.

They accept a 14- or 12-bit digital input representing angle and a reference voltage of either 60Hz or 400Hz, and produce a 3 wire or 4 wire output suitable for driving Synchros or Resolvers.

The 400Hz converters contain internal 1.3VA amplifiers as well as output and reference transformers.

The 60Hz versions contain internal 1.3VA amplifiers but require external output and reference transformers.

If it is necessary to drive a load requiring more than 1.3VA, options for both the 400Hz and 60Hz converters are available allowing the use of external amplifiers and transformers.

#### **RADIUS VECTOR**

One of the outstanding features of these converters is the almost negligible Radius Vector variation (Transformation Ratio).

On many Digital-to-Synchro converters presently available, the individual sine and cosine outputs produced do not follow the exact sine and cosine laws, and depending upon angle can vary up to  $\pm 7\%$ . This is not always important as the ratio of the sine to the cosine, i.e., the tangent, is always correct to the specified accuracy of the converter. There are cases however, when driving torque receivers and certain servo control loops when this variation is unacceptable.

The design of the DSC1705 and DSC1706 has reduced this variation to less than  $\pm 0.1\%$ . This means that when the converters are used in closed loop servo systems, the gain of the closed loop is independent of the digital input angle, thus making reference correction unnecessary.



#### MODELS AVAILABLE

The two Digital to Synchro/Resolver converters described in this data sheet differ primarily in the areas of resolution and accuracy as follows:

Model <u>DSC1705XYZ</u> is a 14-bit converter with an overall accuracy of ±4 arc-minutes.

Model <u>DSC1706XYZ</u> is a 12-bit converter with an overall accuracy of ±8 arc-minutes.

The XYZ option code defines the option thus: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the output and the reference voltages, whether the output is in Synchro or Resolver format and whether external transformers are required.



Principle of Operation

**FUNCTIONAL DIAGRAM, DSC1705 and DSC1706** The principle of operation of the converters described in this data sheet is shown in the diagram above.

# **SPECIFICATIONS** (typical @ +25°C unless otherwise noted)

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Model	DSC1705	DSC1706
ACCURACY <sup>1</sup>	±4 arc-minutes	±8 arc-minutes
RESOLUTION	14 Bits (1LSB = 1.3 arc-minutes)	12 Bits (1LSB = 5.3 arc-minutes)
INPUT CODE	14-Bits Natural Parallel Binary with MSB = 180°	12-Bits Natural Parallel Binary with MSB = 180°
REFERENCE VOLTAGE INPUT		
With Internal Transformers		
Low Level	26V rms	
High Level External Transformer Options <sup>2</sup>	115V rms	*
External Transformer Options	4 V mis	*
REFERENCE FREQUENCY	00Hz 0F 400Hz	
With Internal Transformers		
Low Level	2012	*
High Level	200kQ	*
External Transformer Options <sup>2</sup>	10kΩ	*
DIGITAL INPUT (TTL COMPATIBLE)	1TTL Load	*
OUTPUT VOLTAGE AND FORMAT		
With Internal Transformers		
Low Level	11.8V rms Line-to-Line Synchro	
	or Resolver	*
High Level	90V rms Line-to-Line Synchro	,
	or Resolver	*
External Transformer Options	7V rms Sine and Cosine	
LOAD CAPABILITY	1.3VA	*
SHORT CIRCUIT PROTECTION	Continuous for 5 minutes	*
OUTPUT SETTLING TIME <sup>4</sup>	50µs for 180° Step	*
RADIUS VECTOR VARIATION (Transformation Ratio)	±0.1% max Sine and Cosine	*
INTERNAL TRANSFORMER ISOLATION	500V dc	*
POWER SUPPLIES		
Voltage	±15V dc ±5%	*
Current		
(a) No Load	95mA per Line	*.
(b) Full Load Mean	225mA per Line	*
WARM-UP TIME	1sec to Full Accuracy	*
OPERATING TEMPERATURE RANGE	$0 \text{ to } +70^{\circ}\text{C}$ Standard	*
	-55°C to +105°C Extended	*
STORAGE TEMPERATURE RANGE	-55°C to +125°C	*
SIZE	3 125" x 2 625" x 0 8"	*
	(79.4mm x 66.7mm x 20.3mm)	*
WEIGHT	8 ounces (224 grams) max	*
MEAN TIME BETWEEN FAILURES		
(MTBF) CALCULATED	150,000 Hours	*
NOTES *Specifications same as DSC1705. <sup>1</sup> Accuracy applies over the full operating temperatu of the option and for: (a) ±10% reference frequency and amplitude var	<sup>2</sup> Refers to input to convert re range <sup>3</sup> Refers to output from inte external transformers. iation. <sup>4</sup> Dependent upon option a	er and not to external transformers. rnal converter amplifiers and not from nd load conditions.

(a) 10% reference requery and amplitude variable (b) 10% harmonic distortion on the reference.
(c) ±5% power supply variation.
(d) Any balanced load from no load to full load.

Specifications subject to change without notice.

#### CONNECTING THE CONVERTER

400Hz options. All these converters contain internal output and reference transformers.

The digital input should be connected to pins "1" through "12" on the DSC1706 and pins "1" through "14" on the DSC1705, noting that pin "1" is the Most Significant Bit (MSB).

"S1", "S2" and "S3" should be connected to the appropriate inputs on the synchro being driven. ("S4" is used also when connection is made to a resolver).

The reference should be connected to "R<sub>Hi</sub>" and "R<sub>Lo</sub>" ensuring that the phase is correct.

"GND" is the common for both power supplies and digital inputs.

60Hz Options. For 60Hz operation, an external transformer, STM1679 is required.

The power supplies and digital input should be connected as for the 400Hz version.

The STM1679 transformer should have its pins "SIN", "COS" and "V" connected to the equivalent pins on the converter. The "GND(SIG)" and "GND(REF)" should both be connected to "GND" on the converter.

The outputs to the load should be taken from "S1", "S2" and "S3" on the STM1679 transformer ("S4" also in the case of a resolver).

The reference input should be made to "R<sub>Hi</sub>" and "R<sub>Lo</sub>" on the STM1679.



60Hz Connection to a Control Transformer (Diagram Shows Bottom View of Modules)

#### **OPERATION WITH EXTERNAL AMPLIFIERS OR TRANSFORMER OTHER THAN STM1679**

For certain applications, the power output required by the load will be greater than the 1.3VA supplied by the internal amplifiers. Thus external amplifiers and transformers will be needed. Products offered to fulfull this requirement are:

#### SPA1695 – Dual 5VA Amplifier

STM1696 - 5VA output and reference transformers (400Hz) STM1697 - 5VA output and reference transformers (60Hz)

If you have a requirement for such products please request the data sheet.

#### CONVERTER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



MATING SOCKET: CAMBION 450-3388-01-03

TRANSFORMER (STM1679) OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM



#### **BIT WEIGHT TABLE**

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90,0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1,4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB for DSC1706)	0.0879
13	0.0439
14 (LSB for DSC1705)	0.0220

#### LOADING THE DSC's WITH CONTROL TRANSFORMERS (CT's)

The most common device to be driven by Digital to Synchro converters is the control transformer (CT)

The minimum power required to drive a CT can be expressed as:

$$(VA) = \frac{V^2}{|Z_{so}|} \cdot \frac{3}{4}$$

where V is the line to line voltage and  $Z_{so}$  is the impedance between one input terminal and the other two shorted together with the rotor open circuit. ( $Z_{so} = R_{so} + j X_{so}$ )

For example, if a CT has a  $Z_{so}$  of 700 + j 4900 and a line to line voltage of 90 volts, then:

$$|Z_{so}| = \sqrt{700^2 + 4900^2} = 4950$$
 Ohms  
and (VA) =  $\frac{90^2}{4950} \cdot \frac{3}{4} = 1.23$ VA

#### TUNING CT LOADS

The load can be reduced by tuning the output with 3 capacitors as shown below.



Capacitor Connection for Tuning CT's

C should be equal to:

$$\frac{X_{so}}{2\omega (R_{so}^2 + X_{so}^2)}$$

The power required after tuning will be:

(VA) untuned 
$$x \frac{R_{so}}{Z_{so}}$$

Therefore in the above example the capacitor value should be:

$$\frac{4900}{2 \times 2\pi \times 400 (245 \times 10^5)} = 40 \text{nF}$$

and the power required after tuning will be:

1.23 x 
$$\frac{700}{4950}$$
 = 0.17VA

Note allowance should always be made for tolerances in the CT windings, capacitors and frequency.

#### PRACTICAL CONSIDERATIONS OF TUNING CT LOADS

- 1. The capacitors used need not be of high tolerance, 20% is sufficient.
- 2. Three capacitors must be used, one across S1 and S2, one across S1 and S3 and one across S2 and S3.
- 3. Voltage working and type of capacitors should be as follows:

#### 11.8V Line-to-Line options:

15 Volt ac working or greater, non-polarized tantalum type.

90V Line-to-Line options:

100 Volt ac working or greater, for example, low K ceramic types.

4. For tuning Resolver loads, two capacitors only are required, one connected between S1 and S3 and the other connected between S2 and S4.

#### CONTROL DIFFERENTIAL TRANSMITTERS (CDX's)

The loading on a DSC of these devices can be considered in a similar way to that of CT's. However becasue a CT normally follows a CDX, the effective Z will need to be calculated. This value will normally be between 66% and 80% of the  $Z_{so}$  quoted for the CDX.

#### TORQUE RECEIVERS (TR's)

Torque receivers are more difficult devices to drive than CT's and CDX's, and in general external amplifiers and transformers will be necessary. However, because of the lack of radius vector variation, the DSC1705 and DSC1706 are far more suited to driving TR's than converters with a variation of  $\pm 7\%$ .

For a deviation of an angle  $\theta$ , the drive current required will be:

$$\frac{2 \cdot V \cdot \sin \frac{\theta}{2}}{|Z_{ss}|}$$

Points to be observed are:

- (a) The TR should not be allowed to lock up.
- (b) A phase lead equal to that specified for the TR should be introduced into the reference input to the DSC.
- (c) The reference should always be present on the TR and the converter.
- (d) The DSC output voltage should be matched exactly to the voltage requirements of the TR.

#### CAUTIONS

- (a) Do not connect a 115V reference to a 26V converter.
- (b) Do not reverse the power supplies.
- (c) Do not connect the reference to any other pins except " $R_{Hi}$ " and " $R_{Lo}$ ".

#### ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define the item. All standard options and their appropriate option codes are listed below.

Part Number <sup>1</sup>	Resolution	Operating Temp. Range	Line-to-Line Output Voltage and Format	Reference Voltage	Reference Frequency
DSC1705511	14 Bits	0 to +70°C	11.8V Synchro	26 V	400Hz
DSC1705512	14 Bits	0 to +70°C	90.0V Synchro	115V	400Hz
DSC1705611	14 Bits	-55°C to +105°C	11.8V Synchro	26V	400Hz
DSC1705612	14 Bits	-55°C to +105°C	90.0V Synchro	115V	400Hz
DRC1705518	14 Bits	0 to +70°C	11.8V Resolver	26V	400Hz
DRC1705618	14 Bits	-55°C to +105°C	11.8V Resolver	26V	400Hz
DSC1705507 and STM1679522	14 Bits	0 to +70°C	90.0V Synchro	115V	60Hz
DSC1705607 and STM1679622	14 Bits	-55°C to +105°C	90.0V Synchro	115V	60Hz

Note: 1. For 12-bit resolution, substitute DSC1706 in place of DSC1705 in the above.

2. For options not shown above, consult the factory.

#### VOL. II, 13–12 SYNCHRO & RESOLVER CONVERTERS



#### **FEATURES**

Accurate Sine, Cosine Multiplication 14-Bit Resolution 3 Arc-Minutes Accuracy 0.1% Radius Accuracy Low Profile (0.4") Maximum Frequency to Full Accuracy 2.5kHz Low Feedthrough

#### APPLICATIONS

Digital to Synchro Conversion Displays Axis Rotation Simulators Numerical Control Prediction Vector Resolution Spectrum Analysis Ultra Low Frequency Oscillators

#### **GENERAL DESCRIPTION**

The DTM1716 and DTM1717 are computing converters which have a digital angle input in natural binary form and a bipolar analog input  $V_i(t)$ . There are two analog outputs  $V_{01}(t)$  and  $V_{02}(t)$ , the outputs are related to the inputs by;

 $V_{01}(t) = V_i(t) \sin \phi(t)$   $V_{02}(t) = V_i(t) \cos \phi(t)$ 

where  $\phi$  is the digital angular input.  $\phi$  ranges from 0 to 360°. The analog input has a range of ±10V; the analog output has a range of ±10V.

The digital input has a resolution of 14 bits for the DTM1716 and 12 bits for the DTM1717. The modules are powered from  $\pm 15V$  supply lines.

If the output voltages are regarded as the components of a vector, the radius accuracy is better than 0.1% and the angular inaccuracy is less than 3 arc minutes for the DTM1716.

A block diagram of the DTM1716 is shown in Figure 1.

Particular attention has been paid in the design to achieve high accuracy in the sine and cosine generation so that they may be used separately as accurate functions.



Figure 1. Diagram of DTM1716

# Digital Vector Generator DTM1716/1717 SERIES



Two models are available each with two options as shown below.

<u>DTM1716500</u> has 14-bit digital input resolution and a 0 to  $+70^{\circ}$ C operating temperature range.

<u>DTM1716600</u> has 14-bit digital input resolution and  $a - 55^{\circ}C$  to +105°C operating temperature range.

<u>DTM1717500</u> has a 12-bit digital input resolution and a 0 to  $+70^{\circ}$ C operating temperature range.

<u>DTM1717600</u> has a 12-bit digital input resolution and  $-55^{\circ}$ C to +105°C operating temperature range.

#### **OPERATION**

The operation of the DTM1716 is straightforward, being powered from  $\pm 15V$  lines relative to the common pin. No damage is caused by either the  $\pm 15V$  or  $\pm 15V$  being disconnected but they must not be reversed. The analog input is protected against a short circuit to either power line. The output is short circuit proof and can be connected to either power line without damage. The digital inputs are standard TTL levels. The module dimensions and pin out are shown in Figure 2.



# **SPECIFICATIONS** (typical @ +25°C unless otherwise noted)

MODELS	DTM1716	DTM1717
DIGITAL ANGULAR RESOLUTION	14 bits (1 LSB = 1.3 arc-mins)	12 bits (1 LSB = 5.3 arc-mins)
FULL SCALE OUTPUT	±10V	*
SCALING ACCURACY	0.1% FSR	•
FULL SCALE INPUT	±10V	*
SCALE TEMPCO	25ppm/°C of FSR	•
ZERO OFFSET	5.0mV max	*
OFFSET DRIFT	50μV/°C	•
AC ACCURACY Analog Step Response (10V Step)	40μs (to 0.1%)	•
MAX SLEW RATE	0.5V/µs	*
FULL POWER OUTPUT	8kHz	*
FEEDTHROUGH	<1mV at 400Hz	. •
ANALOG INPUT IMPEDANCE	20kΩ	*
ANALOG OUTPUT IMPEDANCE	100mΩ	*
OUTPUT LOAD	2kΩ	*
OUTPUT PROTECTION	Short circuit proof	*
DIGITAL INPUT	14-bit natural parallel binary, 1TTL Load	12-bit natural parallel binary, 1TTL Load
RESPONSE TO DIGITAL STEP (90°) (FS Analog Input)	40µs to 0.1% of final value	*
VECTOR ACCURACY <sup>1</sup> Radius Error Angular Error	0.1% FSR ±3 arc-mins	•
POWER SUPPLY REJECTION	80dB	*
POWER SUPPLIES	+15V @ 60mA max -15V @ 50mA max	*
TEMPERATURE RANGE Operating Storage	0 to +70°C Standard or -55°C to +105°C extended -55°C to +125°C	•
DIMENSIONS	3.125 x 2.625 x 0.4" 79.4 x 66.7 x 10.2mm	*
WEIGHT	3 oz (85 grams)	*

#### NOTES

\*Specification same as DTM1716.

<sup>1</sup>See Figure 4.

Specifications subject to change without notice.

#### ABSOLUTE MAXIMUM INPUTS

V <sub>i</sub> to GND	• •	 •	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•	•	±	v	S	նսյ	opl	y
+15V Supply	Pin				•			•	•	•					•								+	17	V
-15V Supply	Pin .							•											•				-	17	V
Logic Inputs.																	-	0	.4	v	te	0	+5	.5	V

#### APPLICATIONS OF THE DTM1716

Figure 3 shows how the DTM1716 can be used in radars and radar simulators for modulating display sawtooth generators using signals derived from a synchro transmitter on the antenna and a Synchro to Digital converter. The synchro signal representing the antenna angle is converted to a 14-bit natural binary representation by the Synchro to Digital converter SDC1704. The digital angle is applied to the digital input of the DTM1716. A dc voltage is applied to the DTM1716 analog input which controls the radius of the displayed raster. The output voltages are used to provide the X and Y time base currents. The switches across the capacitors are opened on the leading edge of the transmission pulse and closed after a time interval determined by the range.



Figure 3. PPI Waveform Generation Using the DTM1716

#### AXIS ROTATION

Figure 4 shows how two DTM1716's may be used to compute the new two dimensional coordinates of a point relative to a rotated set of axes. The input voltage  $X_1$  and  $Y_1$  are proportional to the coordinates of a point in the XY plane. If a digital angle  $\phi$  is applied to the DTM1716's, the output voltages  $X_2$  and  $Y_2$  correspond to the X and Y coordinates of the point relative to a set of axes rotated through the angle  $\phi$ . The systems can be extended to three dimensions.

The arrangement as shown in Figure 4 may also be used to obtain the new coordinates of a point which is rotated through the angle in the same coordinate set. This scheme provides a low cost, accurate and compact solution to transformation problems.



Figure 4. Axis Rotation in Two Dimensions Using the DTM1716

### Applying the DTM1716/1717 Series

#### SYNCHRO TO INVARIANT SINE/COSINE

In many engineering applications it is required to obtain voltages proportional to the sine and cosine of an angular movement and to be able to scale the voltages electrically. Figure 5 shows how a Synchro to Digital converter and the DTM1716 may be used for this purpose. The advantage of this scheme is that the coefficients of sine and cosine are electrically scalable by means of the bipolar voltage  $V_i$ , saving memory space, multipliers, power and space.



Figure 5. Synchro to Invariant Sine/Cosine Using the SDC1704 and DTM1716

#### POWER SPECTRUM ANALYSIS

Figure 6 shows a less usual application of the DTM1716 in the spectrum analysis of low frequency signals. This has the advantage of providing almost infinite resolution at extremely low relative cost.

A simple method of obtaining the power in the frequency interval  $f \pm \Delta f$  is shown in Figure 6.

The input waveform from which the power spectrum is required is g(t). Multiplication of this waveform by Sin  $2\pi$ ft causes the energy in the waveform between  $f - \Delta f$  and  $f + \Delta f$  to be shifted to lie between  $-\Delta f$  and  $f + \Delta f$ . The low pass filter passes this voltage waveform to the square law devices to produce an output proportional to the power. Two channels, sine and cosine, are used for the case where g(t) may contain a periodic component. If for example there is a line in the power spectrum, without the use of the two channels the output at that frequency would depend upon its phase. The use of both sine and cosine multiplication avoids this problem.



Figure 6. The Use of the DTM1716 to Obtain the Power Frequency Spectrum of g(t)

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#### PHASE MODULATION

The DTM1717 can be used for low frequency phase modulation of subcarriers. Figure 7 shows the method which uses two DTM1717's and an ADC. Frequency modulation can be obtained if the amplitude of the signal is made to be inversely proportional to its frequency. This can be accomplished by inserting an integrator in series with the modulation input. Similar techniques can be used for very low frequency synthesis.





#### ORDERING INFORMATION

There are only two options for each of the DTM1716 and DTM1717. They are the commercial or extended temperature ranges. The appropriate designations are as follows:

DTM1716500 (14 bits) 0 to +70°C DTM1716600 (14 bits) -55°C to +105°C DTM1717500 (12 bits) 0 to +70°C DTM1717600 (12 bits) -55°C to +105°C

#### **OTHER PRODUCTS**

Many modular and hybrid devices concerned with the conversion of synchro data are manufactured by us, some of these are listed below.

#### DIGITAL VECTOR GENERATORS

The DRC1765 and 1766 are hybrid digital-to-resolver converters that perform a similar function to the DTM1716 but operate over the extended temperature range of  $-55^{\circ}$ C to  $+125^{\circ}$ C.

#### SYNCHRO-TO-DIGITAL CONVERTERS

SDC1700 series of low profile modular converters with 10-, 12- and 14-bit natural binary output. These all have internal transformers for all frequency options.

SDC1740 series of hybrid converters with 10-, 12- and 14bit natural binary output. These hybrid converters offer transformer isolation of both the signal and reference inputs. The operating temperature range is the extended range of  $-55^{\circ}$ C to  $+125^{\circ}$ C.

#### DIGITAL-TO-SYNCHRO CONVERTERS

DSC1705 and 1706 are modular 14- and 12-bit digital-tosynchro converters with a 1.3VA output and internal transformers for signal and reference isolation.

DRC1745 and 1746 are hybrid 14- and 16-bit signal to resolver converters with a 2VA output working over the extended temperature range of  $-55^{\circ}$ C to  $+125^{\circ}$ C.

# 

# Inductosyn<sup>™</sup> Preamplifier and Power Oscillator

# IPA1751, 0SC1754

FEATURES IPA1751 Encapsulated for Protection Phase Shift <5° Phase Match >1° Load Capacity 10,000pF

OSC1754 Isolated Output Multi-Tapped Quadrature Reference Output

#### APPLICATIONS

The IPA1751 and OSC1754 when used with one of the IRDC1730 series Inductosyn/resolver-to-digital converters offers the user all the electronic modules necessary for the Inductosyn to controller interface.

### GENERAL DESCRIPTION IPA1751

The output signals from an Inductosyn slider are at a low level of the order millivolts and requires amplification and buffering before transmission to an Inductosyn to digital converter. The IPA1751 provides the necessary gain and output impedance for this purpose.

Any gain mismatch in the two channels amplifying the sine and cosine outputs of the Inductosyn slider contributes to the system error. The IPA1751 with a 0.15% gain match over the temperature range only contributes an error of 0.23 micron using a 2mm pitch Inductosyn. By carefully controlling phase mismatch to less than 1° the error contribution is only 0.2 micron in a 2mm pitch Inductosyn.

The IPA1751 with an output resistance of less than 3 ohms and a capability of driving a cable capacity of 10,000pF is totally suited to machine tool application where the Inductosyn to digital converter is remote from the measuring Inductosyn.



#### **OSC175**4

The OSC1754 provides the drive for energization of the Inductosyn track. Transformer isolated outputs are available at four voltages that allows a wide range of track resistance to be accommodated. In addition to the power output, a two low power outputs are provided one in phase and one  $90^\circ$  in advance of the power output. The necessity for a quadrature output is for the reference input of the IRDC, since Inductosyn track impedance is predominantly resistive, the slider sine and cosine output voltages are in phase quadrature with the voltage.

The demands on the absolute accuracy of the phase, frequency and amplitude are not exacting owing to the method of conversion used in the IRDC that is tolerant to all these parameters (see IRDC1730/31/33 Data Sheets).

#### MODELS AVAILABLE

Model IPA1751/560 is a two channel preamplifier 1 kHz to 10 kHz operating 0 to  $+70^{\circ}\text{C}$ .

Model OSC1754/500 is a power oscillator at 10kHz operating 0 to  $+70^{\circ}$ C.

Inductosyn is a registered trademark of Farrand Industries, Inc.

### SPECIFICATIONS

**J** (typical @ +25°C over full range of power supply inputs unless otherwise noted)

Model	IPA1751/560
GAIN	$1300 \pm 10\%$
GAIN MISMATCH Channel to Channel	· · ·
Over Temperature Range	$\pm 0.15\%$ (equivalent to 2.5 arc mins)
PHASE SHIFT	<5°
PHASE MISMATCH Channel to Channel	<1°
CROSSTALK	<0.1%
<b>OPERATING FREQUENCY</b>	10kHz
INPUT RESISTANCE	$5k\Omega \pm 10\%$
OUTPUT RESISTANCE	<5Ω
MAX LOAD CAPACITY	10,000pF
MAXIMUM SIGNAL OUTPUT LEVEL	3V rms
POWER SUPPLIES	
Voltage Current	$\pm 12$ V to $\pm 15$ V 30mA max
TEMPERATURE RANGE	
Operating Storage	0 to + 70°C - 55°C to + 125°C
SIZE	2.0" × 2.0" × 0.4" (50.8mm × 50.8mm × 10.2mm)

NOTE

Specifications subject to change without notice.

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



### HYBRID INDUCTOSYN PREAMPLIFIER AND POWER OSCILLATOR

The IPA1764 and OSC1758 are extended temperature devices  $(-55^{\circ}C \text{ to } + 125^{\circ}C)$  with performance similar to the IPA1751 and OSC1754 described in this data sheet. U.S. MIL-STD-883B processing is available on these products.

These products are housed in a hermetically sealed 18-pin double DIP metal case -0.775'' (19.7mm)  $\times 0.975''$  (24.8mm)  $\times 0.2''$  (5.1mm).

#### **OTHER PRODUCTS**

We manufacture a range of Inductosyn/resolver-to-digital converters specifically designed for the numerical controlled machine tool and robot applications.

**IRDC1730** – 12-bit parallel binary output with analog velocity output, direction and ripple carry logic outputs. Tracking rate up to 170 revolutions per second.

**IRDC1731** – A serial output converter with 4,000 counts per revolution, direction and ripple carry output. Tracking rate up to 100 revolutions/pitches per second.

**IRDC1732** – A low cost hybrid. Twelve-bit parallel tri-state latched binary output.

**IRDC1733** – With the features of the IRDC1730 without analog velocity and at a reduced cost.

In addition to this above range, we manufacture a complete range of modular and hybrid synchro/resolver-to-digital and digital-to-synchro/resolver converters.

#### **ABSOLUTE MAXIMUM VALUES**

Sin & Cos I/P							•	 			. ±\	1
+ V Pin								 			+17V	1
-V Pin	<sup>.</sup>							 			- 17V	7
Sin & Cos O/P	1k Load						.`				±10\	1
Indefinite Shor	t Circuit P	ro	of									

# $SPECIFICATIONS (typical @ +25^{\circ}C with \pm 15V supplies unless otherwise noted)$

Model		OSC1754/500	<b>Comments and Conditions</b>
FREQUENCY	r	10kHz ±5%	Over Temperature Range
OUTPUTS	ISOLATED POWER O/P	20V rms 15V rms 5 Watts 10V rms Maximum 5V rms	With $+V = \pm 15V$ All Output Meet $\pm 5\%$ Tolerance Over Temperature Range Fully Loaded.
REFERENCE	81	2.5V rms@4mA max in Phase with Power Outputs	Additional 7% max Change No Load to Full Load.
REFERENCE	22	2.5V rms @ 4mA max 90° Phase Advanced WRT Power Outputs	N.B. All Outputs Vary Proportional to + V Supply
POWER SUPI	PLY	+ 12V to + 15V 100mA max 500mA max	No Load Full Load
<u>-v</u>	· · · ·	- 12 to - 15 20mA max	Independent of Load
TEMPERATU Operating Storage	JRE RANGE	0 to + 70°C − 55°C to + 125°C	
SIZE	· · · · · · · · · · · · · · · · · · ·	3.125" × 2.625" × 1" (79.4mm × 66.7mm × 25.4mm)	
WEIGHT		8 oz 224g	

#### NOTE

Specifications subject to change without notice.

**OUTLINE DIMENSIONS** 

Dimensions shown in inches and (mm).



#### **ABSOLUTE MAXIMUM VALUES**

+V Pin								•									+ 18V
– V Pin		•,	•	•		÷	•		•	•		•		•	•		- 18V

#### **APPLICATION OF OSC1754 AND IPA1751**

The diagram below shows a "hookup" with the preamplifier power oscillator and an IRDC1733 with an Inductosyn. Precise application information is not possible as the Inductosyn in its application has many variables.

#### **Current Set Resistor**

This resistor is used to match the voltage output of the oscillator to the Inductosyn track resistance and provide the manufacturer's recommended current. By variation of the voltage outputs and current resistance, track by this up to approximately 30 feet (9.1 meters) can be accommodated.

#### Decoupling

The preamplifier and oscillator have internal high frequency decoupling capacitors on the supply lines, however, it is recommended that electrolytic decoupling capacitors are connected close to the module pins.

#### **Channel Gains**

There are several ways to achieve a signal value of 2.5V rms at the converter input. When setting gains it is important that the 2.5V rms signal is the maximum in either channel.

Within the limits set by noise, slider exactation can be varied. A useful feature of the tracking converter is its ability to reject incoherent and common mode noise.

As the input impedance of the IRDC is resistive, the gain can be scaled by the addition of series resistors. The required value is  $2.22k\Omega$  per excess volt, the mismatch being more important than the absolute value. A mismatch of 0.1% in the values gives rise to an error of 0.0000787 of the Inductosyn pitch.



Use of IRDC1733 with Inductosyn Preamplifier IPA1751 and Power Oscillator OSC1754

#### **ORDERING INFORMATION**

IPA1751/560 Preamplifier 0 to +70°C OSC1754/500 Oscillator 10kHz, 0 to +70°C



# 12-Bit, Tracking Inductosyn<sup>™</sup>/ Resolver-to-Digital Converters

# IRDC1730/1733

#### **FEATURES**

**Uses Ratiometric Amplitude Measurement Principle** Can Be Used with Inductosyns or Resolvers 12-Bit Parallel Word Representing Resolver Shaft Angle or **Distance Moved Through Inductosyn Pitch** Tracking Rates at Up to 170 revs/sec (10,200 rpm) or 170 Pitches Per Second **Transformer Isolated Inputs Resistive Scaling Facility Accommodates Most Resolver** Signal Levels **Direction Output** Ripple Clock Output (Revolution or Pitch Count) DC Velocity Output Representing Input Rate No External Trims or Adjustments Four Frequency Options (400Hz, 2.6kHz, 5kHz or 10kHz) Low Profile Module (0.4", 10.2mm) **Designed to Meet Intrinsic Safety Requirements** 

#### APPLICATIONS

Industrial Control Machine Tool and Robot Control

#### GENERAL DESCRIPTION

The IRDC1730/33 convert resolver format (sine and cosine) signals into a 12-bit parallel word. The units accept inputs from either a resolver, in which case the 12-bit word represents the angle of the resolver shaft or from an Inductosyn slider via external pre-amps in which case the 12-bit word represents the distance moved through an Inductosyn pitch.

The converters are of the continuous tracking type working on a type 2 servo loop principle and operate for input rates of up to 170 revs per second (in the case of the 5kHz and 10kHz versions). In the case of an Inductosyn input used at these frequencies, they will track at a maximum rate of 170 pitches per second.

The converters are available in 4 different frequency options, 400Hz, 2.6kHz, 5kHz and 10kHz; and the signal and reference inputs, which are transformer isolated, are accepted as 2.5 volts rms max. An outstanding feature of the converters is that even though the signal and reference inputs are transformer isolated, they can still be externally resistively scaled to accommodate the user's particular voltage levels.

A further advantage of the IRDC1730/33 is that they work on a ratiometric, amplitude comparison principle and therefore any voltage drop between the resolver or the Inductosyn and the converter does not substantially affect the accuracy. The amplitude measurement technique also ensures a high degree of noise immunity which might exist on the signal input lines.

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In addition to the digital output, the IRDC1730 also provides a dc velocity signal which is proportional to the rate at which the input is changing.

A direction signal is also provided as well as a ripple clock output which gives a pulse every time the resolver input passes through the zero position or the Inductosyn slider moves to an adjacent pitch (see timing diagram).

The IRDC1730/33 are housed in a 0.4'' (10.2mm) low profile module and weighs only 3.5 ozs (100G).

#### MODELS AVAILABLE

The IRDC1730/33 are available in two operating temperature versions, each one of which is available in four frequency options. For details of how to specify an exact part number see "Ordering Information".

#### **OPERATION OF THE CONVERTER**

The IRDC1730/33 are tracking converters. This means that the output always automatically follows the input for speeds up to the maximum specified tracking rate of the particular option. There is no requirement for "Convert Command" signals. One full revolution of the resolver or the movement of the slider through a distance equivalent to one pitch of the Inductosyn will cause the output of the converter to change from an output of all "zeroes" through to an output of all "ones" or vice versa. As the output of the converter passes through electrical zero of the resolver or the Inductosyn, a pulse will be output on the Ripple Clock (RC) pin. The direction of rotation is indicated by the DIR signal.

### SPFCIFICATIONS (Autorian Data State

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	ai w +20 6 uniess otherwise stated)	······
Model	IRDC1730	IRDC1733
ACCURACY <sup>1</sup>	±8 arc-minutes Static Input (see tracking rate specification)	*
RESOLUTION	· 12 Bits (LSB = 5.27 arc-minutes or 1/4096 of a pitch)	•
DIGITAL OUTPUT	Parallel, 2TTL Loads, MSB = 180° or half pitch posn.	*
SIGNAL AND REFERENCE FREQUENCY <sup>1</sup>	400Hz, 2.6kHz, 5kHz or 10kHz	*
SIGNAL VOLTAGE <sup>1</sup>	2.5 volts max (Sine and Cosine) rms	*
SIGNAL IMPEDANCE	5.6kΩ	*
REFERENCE VOLTAGE <sup>1</sup>	2.5 volts rms	* ·
REFERENCE IMPEDANCE	5.6kΩ	* .
ALLOWABLE PHASE SHIFT <sup>2</sup> (Signal to		
reference)	±20° will give no additional error with a static input	<b>*</b>
TRANSFORMER ISOLATION	500 volts dc	*
TRACKING RATE (min, i.e., at least)	For ±14 arc-minutes Accuracy:	•
	68 rps (400Hz) 87 ms (2 6kHz)	*
	170 rps (5kHz, 10kHz)	•
	For ±10.5 arc-minutes Accuracy:	•
	34 rps (400Hz)	•
	43 rps (2.6kHz)	*
SETTLING TIME (For 170° Stop)	85 lps (5k112, 10k112)	· · · · · · · · · · · · · · · · · · ·
400Hz Options	38ms	•
2.6kHz Options	33ms	*
5/10kHz Options	12ms	*
ACCELERATION CONSTANT (KA)	99 425 /0002	•
2 6kHz Options	88,455/sec 469.000/sec <sup>2</sup>	•
5/10kHz Options	1,015,000/sec <sup>2</sup>	*
"BUSY" OUTPUT	Logic "HI" when busy. 350ns max width. 1TTL load.	*
DIRECTION OUTPUT (DIR)	Logic "LO" when counting up. Logic "HI" when	*
	counting down. 2 STTL load (Mil) 4STTL loads	
	(comm). Valid for min of 300ns before and min of	
RIPPLE CLOCK QUITPUT (RC)	Low going pulse indicating when internal counters will	·
RIFFLE CLOCK OUTFUT (RC)	change from all "1s" to all "0s" or vice versa. Duration	• •
	equals BUSY period, between contiguous positive	
	going edges.	· · · · · · · · · · · · · · · · · · ·
INHIBIT INPUT	Logic "LO" to inhibit. 1LS TTL Load.	*
VELOCITY OUTPUT CHARACTERISTICS:	+FTV +FO( d. f., may shad by shing rate of option	NA
Scaling Polarity	ESV ES% de for max stated tracking rate of option Positive going voltage for increasing angle	NA
Zero Offset	5mV max at +25°C max	
	10mV max at max specified operating temperature	
Gain Temperature Coefficient	0.07%/ C typical, 0.2%/ C max	
Output Noise	Less than 5mV in 0 to 20Hz bandwidth	
POWER SUPPLIES	±15 volts @ 25mA	*
	+5 volts @ 185mA	*
POWER DISSIPATION	1.33 Watts	*
TEMPERATURE RANGE	0 to +70°C Standard	*
	-55°C to +105°C Extended	*
DIMENSIONS	2.625 × 3.125 × 0.4 (66.6mm × 79.3mm × 10.2mm)	*
WEIGHT	3.5 ozs.	*

NOTES <sup>1</sup> Accuracy applies over the operating temperature range and over: (a) ±10% signal and reference voltage and frequency variation (b) ±10% signal and reference harmonic distortion (c) ±5% power supply variation. <sup>2</sup>See "Dynamic Accuracy vs. Resolver Phase Shift" on next page.

\*Specifications same as IRDC1730. Specifications subject to change without notice.

### CONNECTING THE CONVERTER AND RESISTIVELY SCALING THE INPUTS

The sine and cosine signal inputs from the resolver or the Inductosyn slider are required to be 2.5V rms at the converter pins (see note 1, on previous page).

The resistive voltage scaling facility enables higher voltages to be interfaced by the simple addition of external scaling series resistors.

In the case of the signal voltages, the resistor value should be  $2.22k\Omega$  per extra volt required. The matching of the resistors is more important than the absolute calculated value. A matching of 0.1% between the two resistors will give rise to an additional error of 1.7 arc-minutes or 0.0000787 times the Inductosyn pitch.

The reference input can also be scaled using a resistance of  $2.2k\Omega$  per extra volt in the R<sub>HI</sub> line. The absolute value of this resistor is not critical as long as the voltage appearing on the converter pins is within ±10% of 2.5 volts rms.

An example of resistive scaling is shown below where a resolver with a signal voltage of 11.8 volts rms and a reference voltage of 26 volts rms is being used with the IRDC1730.



Resistive Scaling of a Resolver to the IRDC1733

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are  $\pm 15V$  and  $\pm 5V$ . They must be connected to the " $\pm 15V$ " and " $\pm 5V$ " pins with the common connection to GND. It is suggested that 0.1 $\mu$ F and 6.8 $\mu$ F capacitors be placed in parallel from  $\pm 15V$  to GND, from  $\pm 15V$  to GND and from  $\pm 5V$  to GND.

DYNAMIC ACCURACY VS RESOLVER PHASE SHIFT Most resolvers, particularly those of the brushless variety, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

#### Shaft speed (RPS) X Phase Shift (Degs) Reference Frequency

For example, for a phase shift of  $20^{\circ}$ , a shaft rotation of 22 RPS and a reference frequency of 5kHz, the IRDC1730/33 will exhibit an additional error of:

$$\frac{20 X 22}{5000} = 0.088^{\circ}$$

This effect can be eliminated by putting a phase lead in the reference to the converter equivalent to the phase shift in the resolver.

#### THEORY OF OPERATION

The sine and cosine signals are applied to the signal trans-

formers to produce on the secondary windings the following voltages:

$$V_1 = K E_0 Sin \omega t Sin \theta$$
$$V_2 = K E_0 Sin \omega t Cos \theta$$

Where  $\theta$  is the angle of the resolver shaft or the distance moved through a particular pitch of the Inductosyn.

To understand the conversion process, then assume that the current word state of the up-down counter is  $\phi$ .

The  $V_1$  is multiplied by  $\cos \phi$  and  $V_2$  is multiplied by  $\sin \phi$  to give:

 $\begin{array}{c} K E_O \sin \omega t \sin \theta \cos \phi \\ \text{and} \quad K E_O \sin \omega t \cos \theta \sin \phi \end{array}$ 

These signals are subtracted by the error amplifier to give:

K E<sub>O</sub> Sin ωt (Sin  $\theta$  Cos  $\phi$  – Cos  $\theta$  Sin  $\phi$ )

K E<sub>O</sub> Sin  $\omega$ t Sin ( $\theta - \phi$ )

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin  $(\theta - \phi)$ .

When this is accomplished, the word state of the up-down counter ( $\phi$ ), equals within the rated accuracy of the converter, the resolver shaft angle  $\theta$ .

The Ripple Clock output (RC) is provided from the most significant end of the counter while the direction output (DIR) is taken from the steering logic input to the counter. The BUSY output is derived from the clock used to drive the counter and this can be disabled using the INHIBIT.



#### DATA TRANSFER

The readiness of the converter for data transfer is indicated by the state of the BUSY pin, (see diagram).

The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, when the input to the converter is changing. The converter is busy when the BUSY pin is at a TTL "Hi" level. These pulses correspond to those delivered by the VCO to increment or decrement the up-down counter (see



Data Transfer Diagram (See Also Timing Diagram) SYNCHRO & RESOLVER CONVERTERS VOL. II, 13–23 schematic diagram). Thus the pulses will occur for increasing and decreasing counts.

The most suitable time for transferring data is at or following the negative going transition of BUSY.

Taking the INHIBIT to a logic "Lo" state prevents the VCO (BUSY) pulses from updating the up-down counter. However, if applied during a BUSY pulse, the INHIBIT will not become effective until the end of the BUSY pulse.

An alternative method of transferring the data is by applying the  $\overline{\text{INHIBIT}}$  (taking it to a logic "Lo" state), waiting for at least the width of a BUSY pulse, transferring the data and releasing the  $\overline{\text{INHIBIT}}$ .

Note that sustained application of the INHIBIT opens the internal control loop and the converter may take an appreciable time to recover to full accuracy when the loop is restored.

### USE OF THE IRDC1730 IN A RESOLVER MACHINE TOOL APPLICATION

In many machine tool applications, a resolver is fitted to the axis lead screw in order to provide a method of measuring linear displacement. The IRDC being a tracking converter with no drift or stale data problems and having a very high maximum tracking rate (over 10,000 rpm in the case of the 5 and 10kHz versions) forms an ideal method of converting the output of the resolver into digital format for use by the controller. The diagram below shows how the resolver may be used in this type of application as well as a method of using external counters to count the number of revolutions of the lead screw and so give an absolute digital representation of the machine axis position.

Note that unlike the phase measuring resolver to digital conversion techniques which require the resolver to be supplied with a very accurate sine and cosine waveform, this method requires that the resolver rotor is energized and the sine and cosine outputs from the stator taken to the converter. The advantage of this method is that the converter's ratiometric operation does not require a particularly stable voltage or frequency reference to be applied to the resolver rotor. In addition, any small drops in voltage between the resolver and the



Using the IRDC1730 with a Resolver on a Machine Tool Axis

converter or any noise induced in the signal lead, will not substantially affect the accuracy.

The "Set Datum" microswitch shown on the end of the lead screw and the associated circuitry is used to zero the counters when the axis movement is at the end of the lead screw. As long as the microswitch operates within a pitch, the datum can then be set electronically.

#### USE OF THE IRDC1730 WITH AN INDUCTOSYN FOR MEASURING LINEAR OR ROTARY DISPLACEMENT

The IRDC1730 can be used very effectively with an Inductosyn to provide a very accurate linear or rotary measurement system. Inductosyns are normally of 2mm pitch and therefore the resolution obtainable will be in excess 0.5 microns. The use of the IRDC1730 in, for example, a machine axis control system is shown in the diagram below.

The Inductosyn gives signals similar to a resolver but with two important differences. The output signals from the slider are very small and need preamplification before being applied to the converter.

These signals are also advanced in electrical phase by  $90^{\circ}$  with respect to the current flowing in the Inductosyn track. The simplest way of correcting this is to drive a reference input to the converter which is also shifted in phase by  $90^{\circ}$ . This is performed internally in the OSC 1754 drive oscillator.

The amplifiers which are necessary between slider and converter need to have equal gains in order to amplify the signals to the 2.5 volts rms required by the converter. (A gain ratio of 1.002 will give rise to an inaccuracy of 1/6000 of a pitch). A typical voltage which might be available at the input to the amplifier is 2mV. The amplifiers should be connected as close to the slider as possible with the longer connecting leads being at the high voltage level. The low output impedance of the amplifiers will then drive the cable.

The "Set Datum" circuitry shown in the diagram is identical to that used for the resolver application, the only provision being that the microswitch always operates within the same pitch of the Inductosyn.



Use of IRDC1733 with Inductosyn Pre-Amplifier IPA1751 and Power Oscillator OSC1754


Individual Mating Sockets: Cambion 450-3388-03-01

BIT WEIGHT TABLE					
Bit Number	Weight in Degrees				
1 (MSB)	180.0000				
2	90.0000				
3	45.0000				
4	22,5000				
5	11,2500				

5.6250

2.8125

1.4063

0.7031

0.3516

0.1758

0.0879

**VELOCITY OUTPUT FILTER** 

12 (LSB)

6

7

8

9

10

11

The velocity output of the IRDC1730 is internally filtered as shown below.



### TIMING DIAGRAM



SYNCHRO & RESOLVER CONVERTERS VOL. II, 13-25

### **USE OF THE IRDC1730 VELOCITY OUTPUT VOLTAGE**

The diagram below shows the use of the velocity output voltage of the IRDC1730 in a servo system.



Practical control using the IRDC1730 as a virtual tachometer

### **TRANSFER FUNCTIONS**

The transfer functions of the various options of the IRDC1730 is as shown below.

### **400Hz Options**

 $\theta_0$  4.815 × 10<sup>5</sup>s + 9.331 × 10<sup>7</sup>

 $\overline{\theta_1} = \frac{1}{s^3 + 1.055 \times 10^3 s^2 + 4.815 \times 10^5 s + 9.331 \times 10^7}$ 

2.6kHz Options

 $\theta_0$  2.745 × 10<sup>6</sup>s + 1.935 × 10<sup>9</sup>

 $\overline{\theta_1} = \frac{1}{s^3 + 4.125 \times 10^3 s^2 + 2.745 \times 10^6 s + 1.935 \times 10^9}$ 

### 5kHz and 10kHz Options

 $\frac{\theta_0}{\theta_1} = \frac{5.909 \times 10^6 \text{s} + 3.908 \times 10^9}{\text{s}^3 + 3.85 \times 10^3 \text{s}^2 + 5.909 \times 10^6 \text{s} + 3.908 \times 10^9}$ 

### **OTHER PRODUCTS**

In addition to the IRDC1730/33, we also manufacture a very comprehensive range of products which are concerned with the conversion of synchro and resolver information into digital format.

Of particular note is the IRDC1731 which accepts similar inputs to the IRDC1730 but provides a 4000 count serial output. Also we manufacture:

IPA1751 Inductosyn pre-amplifier

OSC1754 Inductosyn/resolver power oscillator

SDC1740/41/42 14- and 12-bit hybrid synchro/resolverto-digital converters with *internal transformers*. SDC1702, 1700 and 1704 10-, 12- and 14-bit synchro/ resolver-to-digital converters.

SDC1725 and 1726 12- and 10-bit synchro/resolver-todigital converters with latched three-state outputs. SDC1721 16-bit synchro/resolver-to-digital converter. DTM1716 and 1717 digital vector generators. DSC1705 and 1706 14- and 12-bit digital-to-synchro/ resolver converters with low radius vector variation. API1620 angle position indicator.

### **ORDERING INFORMATION**

The IRDC1730 part number is suffixed with an X and a Y code to denote operating temperature range and reference frequency as follows. (Note that the Z code used in our other products to denote voltage is left as a zero in this product).

### IRDC1730/XY0 IRDC1733/XY0

Y = 1	400Hz
Y = 4	2.6kHz
Y = 5	5kHz
Y= 6	10kHz

X = 5	0°C to +70°C
K = 6	-55°C to +105°C

### ABSOLUTE MAXIMUM INPUTS

R <sub>HI</sub> to R <sub>L</sub>	0																			-	± S	5V	rn	15
Sin/Cos to	Si	gn	al	C	lo	m	m	or	1		•									2	± 5	γ	rn	15
+15V Pin	•					•											÷			•	•	+	17	V
– 15V Pin						•															•	-	17	V
+5V Pin		•		•		•										•			1	0.4	ŧ٧	ťto	o 7	V
Any Logic	Ir	ıp	ut	s	•	•				•		•	•	`.			- 1	0.	4V	' te	0	+ 5	5.5	V

All dc voltages are with respect to GND pin.

### Note:

No damage will result by allowing the signal and reference voltages to be applied without the dc power supplies present.

# 

# 4000 Count, Tracking Inductosyn<sup>™</sup>/ Resolver-to-Digital Converter

# IRDC1731

### FEATURES

Works on Amplitude Measurement Technique Can Be Used with Inductosyns or Resolvers 4000 Count Serial Output per Revolution or Pitch Transformer Isolated Inputs 100 revs/sec (pitches/sec) Tracking Rate Resistive Scaling Facility Accommodates Most Signal Levels Direction Output Zero Crossing Output (Pitch or Revolution Counter) No External Trims or Adjustments Low Profile 0.4" (10.2mm)

### APPLICATIONS

Digital Display of Inductosyn or Resolver Information in Robotics or Machine Tool Axis Measurement

### GENERAL DESCRIPTION

The IRDC1731 converts resolver format (sine and cosine) signals into a 4000 count serial output. The unit accepts inputs from either a resolver, in which case the 4000 counts represent 1 revolution of the shaft or from an Inductosyn slider via external pre-amps in which case the 4000 counts represent a distance corresponding to 1 pitch of the Inductosyn track.

The converter is of the continuous tracking type working on a type 2 servo loop principle and operates for input rates of up to 100 revolutions per second in the case of the resolver and 100 pitches per second in the case of the Inductosyn. The continuous tracking principle gives the advantages of zero drift and instantly available, nonstale data.

The converter operates on a 5kHz reference frequency and the inputs, which are transformer isolated, are accepted as 2.5 volts rms max.

An outstanding feature of the converter is that even though the signal and reference inputs are transformer isolated, they can be externally resistively scaled to accommodate the user's particular voltage levels.

A further advantage of the IRDC1731 is that it works on a ratiometric, amplitude comparison principle and therefore any voltage drops between the resolver or the Inductosyn and the converter does not substantially affect the accuracy. The amplitude measurement technique also ensures a high degree of immunity to noise which may exist on the signal input lines.

Inductosyn is a registered trademark of Farrand Industries, Inc.



In addition to the serial output, a direction signal is provided as well as a Zero Crossing signal which gives a pulse every time the resolver input passes through the zero position or the Inductosyn slider moves to an adjacent pitch.

The IRDC1731 is housed in a 0.4'' (10.2mm) low profile module and weights only 3.5 ozs. (100 G).

MODELS AVAILABLE

Two models of the IRDC1731 are available, viz:

<u>Model IRDC1731550</u> which operates over a 0 to  $+70^{\circ}$ C temperature range. (Commercial temperature option).

<u>Model IRDC1731650</u> which operates over a  $-55^{\circ}$ C to  $+105^{\circ}$ C temperature range. (Extended temperature option).

# SPECIFICATIONS (typical @ +25°C unless otherwise stated)

----

Model	IRDC1731
ACCURACY <sup>1</sup>	±2 counts (static input)
	±3 counts (50 pitches or revs/sec input)
	±4 counts (100 pitches or revs/sec input)
RESOLUTION	4000 counts equals one revolution of resolver or
	one pitch of the Inductosyn
DIGITAL OUTPUT	Serial, negative going pulses, width 1.0 $\pm 0.5 \mu s$
	4 TTL loads – commercial temperature options
SIGNAL AND REFERENCE ERECHENCY	
SIGNAL INPUT VOLTAGE <sup>1</sup>	2.5 volte me
SIGNAL INDUT IMDEDANCE	5.6LQ
BEEEDENCE INDUT VOLTACE <sup>1</sup>	2.5 volt
REFERENCE INPUT HOREDANCE	
REFERENCE INPUT IMPEDANCE	5.0K12
'Dynamic Accuracy vs. Resolver Phase	$\pm 20$ will give no additional error with a static
Shift')	mput
TRANSFORMER ISOLATION	500 volts dc
TRACKING RATE (Minimum)	100revs/sec (Resolver input)
	100 pitches/sec (Inductosyn input)
STEP RESPONSE (179° Step)	80ms max for ±1 count additional error
ACCELERATION	
Constant K <sub>a</sub>	650,000/sec <sup>2</sup>
DIRECTION OUTPUT (DIR)	Logic "Lo" when counting up. Logic "Hi" when
	counting down. Direction output level changes at
	4  TTL loads = commercial temperature ontions
	2 TTL loads – extended temperature options
ZERO CROSSING OUTPUT (Z.C. O/P)	Positive going pulse, 1.0 $\pm 0.5\mu$ s in width produced
	when resolver input passes through zero position or
	Inductosyn slider moves to adjacent pitch.
	4 TTL loads – commercial temperature options
Down down and	2 11L loads – extended temperature options
POWER SUPPLIES	+15V dc @ 35mA max
	+5V dc @ 170mA max
POWER DISSIPATION	1.90 watts max
OPERATING TEMPERATURE RANGE	
Commercial	0 to +70°C
Extended	-55°C to +105°C
STORAGE TEMPERATURE RANGE	-55°C to +125°C
DIMENSIONS	$2.625'' \times 3.125'' \times 0.4''$
	(66.7mm X 79.4mm X 10.2mm)
WEIGHT	3.5 ozs. (100 G)
NOTES <sup>1</sup> Accuracy applies over the appropriate operating temperatur (a) ±10% signal and reference voltage amplitude variation. (b) ±10% signal and reference harmonic distortion.	e range and:
(c) ±10% variation in reference frequency.	
Specifications subject to change without notice.	

### **OPERATION OF THE CONVERTER**

The IRDC1731 is a tracking converter meaning that the output automatically follows the input up to a rate of 100 revs. or pitches per second without the need for any convert command signal. 4000 negative going pulses are output for each full revolution or pitch and a TTL direction output (DIR) indicates the direction of motion.

# CONNECTING THE CONVERTER AND RESISTIVELY SCALING THE INPUTS

The sine and cosine signal inputs from the resolver or Inductosyn and the reference input are required to be 2.5 volts rms. The voltage scaling facility enables higher voltages to be interfaced by the simple addition of external series scaling resistors.

In the case of the signal voltages, the resistors should be  $2.22k\Omega$  per extra volt required. The matching of the resistors is more important than the absolute calculated value. A matching of 0.1% between the two resistors will give rise to an additional error of  $\pm 0.31$  counts.

The reference input can be scaled resistively also using a resistance of  $2.2k\Omega$  per extra volt in the  $R_{HI}$  line. The absolute accuracy of this resistor value is not critical as long as the voltage appearing on the converter pins is within the tolerance specified for the 2.5 volt rms reference input.

An example of resistive scaling is shown below where a resolver with a signal voltage of 11.8 volts rms and a reference voltage of 26 volts rms is being used with the IRDC1731.



The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are  $\pm 15V$ and  $\pm 5V$ . They must be connected to the " $\pm 15V$ " and " $\pm 5V$ " pins with the common connection to the ground pin GND.

It is suggested that  $0.1\mu$ F and  $6.8\mu$ F capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

# USE OF THE IRDC1731 IN A RESOLVER MACHINE TOOL \_ APPLICATION

In many machine tool applications, a resolver is fitted to the axis lead screw in order to provide a method of measuring linear displacement. The IRDC1731, being a tracking converter and having no drift or stale data problems, forms an ideal method of converting the output of the resolver into digital format, either for use by a processor or for a visual digital readout of axis position. The diagram shows how a resolver may be used in this type of application with the



Figure 1. Diagram Showing IRDC1731 Used with a Resolver in a Machine Tool Axis Measurement System

IRDC1731 and external counters to provide a BCD (Binary Coded Decimal) indication of axis position.

In the diagram shown, the number of counters will be sufficient to register the 4000 counts produced by one revolution of the resolver. This means that the counter output will represent a distance equivalent to one pitch of the lead screw (normally 2, 5 or 10 millimeters). In order to provide a readout of the absolute position on the lead screw, more counters can be added as indicated in the diagram.

The "Set Datum" microswitch shown on the end of the lead screw and the associated circuitry is used to zero the counters when the axis movement is at the end of the lead screw. Once the microswitch has been activated, the counters will be reset to zero by the next zero crossing pulse (Z.C. O/P) and the counting will commence. This method gives the advantage that the lead screw zero datum can be accurately set to within one count while the microswitch is only required to operate within one revolution of the lead screw.

### DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Most resolvers, particularly those of the brushless variety, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

### Shaft Speed (R.P.S.) X Phase Shift (Deg)

### **Reference Frequency**

For example, for a phase shift of 20°, a shaft rotation of 22 revs. per second and a reference frequency of 5kHz, the IRDC1731 will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088^{\circ} = 0.98 \text{ counts}$$

This effect can be eliminated by putting a phase lead in the reference to the converter equivalent to the phase shift in the resolver.

# USE OF THE IRDC1731 WITH AN INDUCTOSYN FOR MEASURING LINEAR DISPLACEMENT

The IRDC1731 can be used very effectively with an Inductosyn to provide a very accurate linear displacement measurement system. Inductosyns are normally of 2mm pitch and, therefore, the resolution obtainable will be 0.0005mm or 0.5 microns.

The diagram indicates the method of converting the Inductosyn output into digital format.



### Figure 2. An Inductosyn Used with the IRDC1731 and External Counters

The Inductosyn in this case is made to behave like a resolver. The fixed track is driven from an ac current generator at a frequency of 5kHz, and the resolver format sine and cosine signals are available from the slider. The reason for using a current source is that the track is mainly resistive and it is better to determine the phase by deliberately driving the track from a current source and inserting a 90 degree phase advance into the reference rather than having a less accurately defined phase shift due to the track's X to R ratio.

The amplifiers which are necessary between slider and converter need to have equal gains in order to amplify the signals to the 2.5 volts rms required by the converter. (A gain ratio of 1.002 will give rise to an inaccuracy of 1/6000 of a pitch.) A typical voltage which might be available at the input to the input to the amplifiers is 3mV. The amplifiers should be connected as close to the slider as possible with the longer connecting leads being at the high voltage level. The low output impedance of the amplifiers will then drive the cable.

Further information on interfacing the IRDC1731 to Inductosyns is available from the factory.

The "Set Datum" circuitry shown in the diagram is identical to that used for the resolver application, the only provision being that the microswitch always operates within the same pitch of the Inductosyn.



### ORDERING INFORMATION

Order IRDC1731550 for operation over temperature range of 0 to  $+70^{\circ}$ C. (Commercial)

Order IRDC1731650 for operation over temperature range of -55°C to +105°C. (Extended)

### **OTHER PRODUCTS**

In addition to the IRDC1731, we also manufacture a very comprehensive range of products which are concerned with the conversion of synchro and resolver information into digital format.

Of particular note is the IRDC1730 which accepts similar inputs to the IRDC1731 but provides a parallel 12-bit digital representation of the input as well as a direction and Zero crossing output. In addition a dc voltage is provided which represents input velocity.

# **ANALOG** DEVICES

# MULTIBUS<sup>™</sup>Compatible Multi-Channel Interface

# MCI 1794

### **FEATURES**

Complete Three-Channel Tracking Inductosyn<sup>TM</sup>/ Resolver-to-Digital Converter 12-Bit Angular Resolution 12-Bit Pitch Counter I/O or Memory Mapped Compatible with Both 8- and 16-Bit MULTIBUS Processors Three Independent Channels Tracking Rates up to 170rpm (10,200rpm) Powered from the Standard MULTIBUS Supplies

### **GENERAL DESCRIPTION**

The MCI1794 is a complete three-channel tracking Inductosyn or resolver-to-digital converter. Each channel converts an input angle into a 12-bit binary data and also contains an independent 12-bit pitch counter for multiturn applications.

The MCI1794 compliance is: Slave D16, I16.

The MCI1794 greatly simplifies the task of interfacing Inductosyns or resolvers with Intel 8080/85/86 based microprocessors and is particularly useful in numerically and computer controlled machines.

The MCI1794 is provided with wire-wrap links which preset the port address (Table I).

The user can change the links to suit both the required addresses and the master data bus requirements.

### 8- AND 16-BIT MULTIBUS COMPATIBILITY

The resolver board is capable of operating on both 8-bit and 16bit buses. Read and write operations to and from the resolver board are accomplished through seven on-board I/O ports. Ports 0 to 5 are concerned with reading the shaft angle and pitch. Port 6 is used to reset the read signal logic.

The shaft angle and its pitch are represented by two 12-bit words. Each of the 3 axis resolvers has one 16-bit and one 8-bit port. The word structure of each of the six resolver ports is given in Table I. The shaft pitch is obtained from a 12-bit counter which is clocked each time the shaft rotates through 360°. The pitch counters of each axis can be cleared independently by performing an I/O write to either of the two port addresses for the axis concerned.

Inductosyn is a registered trademark of Farrand Industries, Inc. MULTIBUS is a registered trademark of Intel Corporation.



### DATA ACQUISITION

To allow maximum flexibility the resolver board has been designed to work in both 8-bit and 16-bit bus systems.

Each resolver has a unique I/O board address which is set by connecting the BOARD SELECT pin (T57) to one of the outputs of the board select decoders, BSO-BS15 (Table II). A total of 16 boards can be connected to the same computer bus. The position of the board select address in the I/O address field is set by connecting 104 (LSB), 105, 106 and 107 (MSB) to the appropriate address pins Z58-Z44 (ADRI-ADRF). A further three address lines are decoded to select which on-board port is to be accessed. The position of the on-board port select lines in the I/O field is determined by connecting 100, 101 and 102 to the appropriate address pins. It is usual to have the on-board port address below the board select address.

The board is normally fitted with three IRDC1730/33 converters. For complete information regarding these parts ask for the separate data sheet. The remaining address line, i.e., those which have not been decoded, should be connected to connector pins T16 through T26, with any spare connector pins between T16 and T26 being connected to T6 (Logical 1).

### ANALOG INPUT SIGNALS

The analog inputs are connected via a 50-pin connector, J. The pin designation of this connector is given in Table III and should be read in conjunction with the IRDC1730 data sheet.

Port Address (Hex)	Channel No.	Data M.S. 4 Bits	Data L.S. 4 Bits	Port No.
48	Channel 1	Pitch M.S	. 8 Bits	0
4B`	Channel 1	Pitch L.S.P.	Angle M.S.P.	).
4A	Channel 1	Angle L.S.	. 8 Bits	) ) 1 )
44	Channel 2	Pitch M.S	. 8 Bits	2
47	Channel 2	Pitch L.S.P.	Angle M, S.P.	)
46	Channel 2	Angle L.S.	. 8 Bits	)3 )
40	Channel 3	Pitch M.S	. 8 Bits	4
43	Channel 3	Pitch L.S.P.	Angle M.S.P.	)
42	Channel 3	Angle M.S	. 8 Bits	)5 )
4C	Clear	Not A	pplicable	6

Table I. MCI1794 Port Designation (as Supplied): 8-Bit Data Bus

MSB Port Address (Hex)	BS No. Connected to T57
0	0
1.	4
2	2
3	6
4*	1*
5	5
6	3
7	7
8	8
9	9
Α	10
. В	11
С	12
D	13
Е	14
F	15

J2–J50		All GND
J1	Channel 1	Velocity Output
J3	Channel 1	Signal Common
J5	Channel 1	Cosine Input
J7	Channel 1	Sine Input
J9	Channel 1	GND
J13	Channel 1	R <sub>LO</sub> Input
J15	Channel 1	R <sub>HI</sub> Input
J17	Channel 2	Velocity Output
J19	Channel 2	Signal Common
J21	Channel 2	Cosine Input
J23	Channel 2	Sine Input
J29	Channel 2	R <sub>LO</sub> Input
J31	Channel 2	R <sub>HI</sub> Input
J33	Channel 3	Velocity Output
J35	Channel 3	Signal Common
J37	Channel 3	Cosine Input
J39	Channel 3	Sine Input
J45	Channel 3	R <sub>LO</sub> Input
J47	Channel 3	R <sub>HI</sub> Input

\*N.B. This address is pre-wired.

Table II. Post Address Significance When T57 (Board Select) is Connected to a BS Terminal

Table III. J Connector Pin Designation

### **ORDERING INFORMATION**

MCI1794/5Y0

The Y of the suffix specifies the frequency option of the IRDC1730 converters.

VOL. II, 13-32 SYNCHRO & RESOLVER CONVERTERS



# **5VA Output Transformers**

# RTM/STM 1686/1696/1736/1687/1697/1737



# **RTM/STM 1686**

**SPECIFICATIONS** (typical @ +25°C unless otherwise noted)

ACCURACY <sup>1</sup> (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	400Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	21 ounces (580G)

### NOTES

<sup>1</sup>Accuracy applies over the full operating temperature range of the option and for:

(a) ±10% reference frequency and amplitude variation.

(b) 10% harmonic distortion on the reference.

(c) Any balanced load from no load to full load.

Specifications subject to change without notice.

### **APPLICATION OF THE RTM/STM1686**

The RTM/STM1686 should be used in conjunction with the DTM1716 or the DTM1717 Digital Vector Generator and the SPA1695 Power Amplifier.

### **ORDERING INFORMATION**

Part Number	Operating Temp. Range	Line-to-Line Output Voltage and Format	Reference Voltage	Reference Frequency
STM1686611	-55°C to +105°C	11.8V Synchro	26 V	400Hz
STM1686612	-55°C to +105°C	90.0V Synchro	115V	400Hz
RTM1686618	-55°C to +105°C	11.8V Resolver	26 V	400Hz

Note: For options not shown above, consult the factory.



Figure 1. Diagram Showing Connection of the STM1686 to a DTM1716 or DTM1717 and SPA1695 (See Notes)

### RTM/STM1686 OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



# **RTM/STM 1696**

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY <sup>1</sup> (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	400Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	22 ounces (620G)

NOTE:

<sup>1</sup> See STM1686 note 1. Specifications subject to change without notice.

### **APPLICATION OF THE RTM/STM1696**

The RTM/STM1696 should be used in conjunction with the DSC1705 or DSC1706 Digital-to-Synchro (or Resolver) Converter and the SPA1695 Power Amplifier.

### ORDERING INFORMATION

		Line-to-Line			
	Operating	Output Voltage	Reference	Reference	
Part Number	Temp. Range	and Format	Voltage	Frequenc	
STM1696611	-55°C to +105°C	11.8V Synchro	26V	400Hz	
STM1696612	-55°C to +105°C	90.0V Synchro	115V	400Hz	
RTM 1696618	-55°C to +105°C	11.8V Resolver	26 V	400Hz	
Note: For option	s not shown above, con	sult the factory.			

# **RTM/STM 1736**

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY <sup>1</sup> (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	400Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT Note:	19 ounces (540G)

<sup>1</sup>See STM1686 note 1.

Specifications subject to change without notice.

### **APPLICATIONS OF THE RTM/STM1736**

The RTM/STM1736 should be used in conjunction with the DSC1605 or the DSC1606 Digital-to-Synchro Converter and the SPA1695 Power Amplifier.

### **ORDERING INFORMATION**

Part Number	Operating Temp. Range	Line-to-Line Output Voltage and Format	Reference Voltage	Reference Frequency
STM1736611	-55°C to +105°C	11.8V Synchro	26 V	400Hz
STM1736612	-55°C to +105°C	90.0V Synchro	115V	400Hz
RTM1736613	-55°C to +105°C	11.8V Resolver	11.8V	400Hz
RTM1736614	-55°C to +105°C	26V Resolver	26 V	400Hz
RTM1736618	-55°C to +105°C	11.8V Resolver	26 V	400Hz
Note: For option	r not chown shows son	sult the factory		

### NOTES FOR FIGURES 1, 2, AND 3:

1. The "Sin F/B" and the "Cos F/B" pins of the SPA1695 should be connected directly of the "Sin" and "Cos" terminals on the output transformer at the transformer.



Figure 2. Diagram Showing Connection of the STM1696 to a DSC1705 or DSC1706 and SPA1695 (See Notes)

### RTM/STM1686 OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM





Figure 3. Diagram Showing Connection of the STM1736 to a DSC1605 or DSC1606 and SPA1695 (See Notes) RTM/STM1736 OUTLINE DIMENSIONS

AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



This is to compensate for any drop in voltage along the connections between the "Sin O/P" and "Cos O/P" pins of the amplifier and the transformer.

2. The "+15V" and "-15V" pins of the SPA1695 should be connected to a regulated power supply in order to drive the internal operational amplifiers. The "+15V(P)" and "-15V(P)" are used for the output stage and these supplies need not be a precision source, the range of voltage when considering all tolerances including ripple, should be be-

# STM 1687

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY <sup>1</sup> (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	60Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	3 lbs (1.34kg)

Note:

<sup>1</sup>See STM1686 note 1.

Specifications subject to change without notice.

### APPLICATION OF THE STM1687

The STM1687 should be used in conjunction with the DTM1716 or the DTM1717 Digital Vector Generator and the SPA1695 Power Amplifier.

### DIMENSIONS AND CONNECTIONS

The STM1687 consists of a kit of two D3953 transformers and one A10163 transformer. These should be connected as shown in Figure 4.

The dimensions are given in Figures 7 and 8.

# STM 1697

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY <sup>1</sup> (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	60Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	3 lbs (1.34kg)

Note: <sup>1</sup> See STM1686 note 1.

Specifications subject to change without notice.

### **APPLICATION OF THE STM1697**

The STM1697 should be used in conjunction with the DSC1705 or the DSC1706 Digital to Synchro Converter and the SPA1695 Power Amplifier.

### DIMENSIONS AND CONNECTIONS

The STM1697 consists of a kit of two D3953 transformers and one A10033 transformer. These should be connected as shown in Figure 5.

The dimensions are given in Figures 7 and 8.

tween 14.75 and 20 volts.

3. The part of the 0 volt system local to the amplifier and converter should be tapped from the "GND(SIG)" pin on the transformer and should not interconnect with any other part of the 0 volt system by any other method (see above diagram).



Figure 4. Diagram Showing the Connection of a STM1687 to a DTM1716 or DTM1717 and a SPA1695

### ORDERING INFORMATION

The transformer should be ordered as:

STM1687622 50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

Note: For options not shown above, consult the factory.



Figure 5. Diagram Showing the Connection of a STM1697 to a DSC1706 or DSC1705 and a SPA1695

### ORDERING INFORMATION

This transformer should be ordered as:

STM1697622 50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

Note: For options not shown above, consult the factory.

# STM 1737

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY <sup>1</sup> (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	60Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	~55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	3 lbs (1.34kg)

Note: <sup>1</sup> See STM1686 note 1.

Specifications subject to change without notice.

### **APPLICATION OF THE STM1737**

The STM1737 should be used in conjunction with the DSC1605 or the DSC1606 Digital-to-Synchro Converter and the SPA1695 Power Amplifier.

### DIMENSIONS AND CONNECTIONS

The STM1737 consists of a kit of two D3953 transformers and one A10033 transformer. These should be connected as shown in Figure 6.

The dimensions are given in Figures 7 and 8.



Figure 6. Diagram Showing the Connection of a STM1737 to a DSC1606 or DSC1605 and a SPA1695

### **ORDERING INFORMATION**

This transformer should be ordered as:

STM1737622 50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

Note: For options not shown above, consult the factory.

### OUTLINE DIMENSIONS





Figure 7. Outline Drawing and Dimensions of the D3953 Transformer

BALANCING SCOTT-T TRANSFORMERS (APPLIES ONLY TO TRANSFORMERS IN KIT FORM).



Figure 9. Diagram Showing Balancing Circuit

The Scott T transformers (two D3953 transformers) can be balanced by the following method:

Connect the primary windings of the transformers to give a known angle input of 45°. This can be done by connecting the two coils in parallel to a 7V rms supply, thus giving an equal



Figure 8. Outline Drawing and Dimensions of the A10163 and A10033 Transformers

sine and cosine contribution.

The 3 wire output signal is then monitored on an Angle Position Indicator (e.g. API1620 or API1718) with no load attached. A resistor R1 should be connected across S1 and S3 until the API reads 45.00°.

A balanced load is then connected across S1, S2 and S3 the change in angle is monitored by the API and minimized by adding resistors (R2 and R3) in series with S1 and S3. R2 and R3 will have equal values. Increasing R2 and R3 will decrease the angle monitored by the API.

Suggested initial values for R1 is  $27k\Omega$  and for R2 and R3 is  $30\Omega$ .

The transformer modules STM1686, 1696 and 1736 are balanced before leaving the factory.



# Synchro/Resolverto-Linear DC Converter

# SAC1763

### FEATURES

High Dynamic Performance (27,000°/sec) High Accuracy (±11 Arc-Minutes) Internal Converter Tracking Loop Provides High Noise Immunity Low Output Ripple (Less than 5mV p-p) DC Output Proportional to Input Rate 50Hz to 2.6kHz Reference Frequency Operation Self Contained—No External Transformers or Adjustments Needed

### APPLICATIONS

Measurement and Recording of Synchro or Resolver Information on Chart Recorders, X-Y Plotters, FM Recorders, Etc. Servo Control and Positioning

### **GENERAL DESCRIPTION**

The SAC1763 is a Synchro/Resolver-to-Linear dc Converter. It takes input angular information in synchro or resolver form voltages and gives an output voltage which is linearly proportional to the input angle. The output voltage of  $\pm 10V$  at  $\pm 5mA$ represents an input angular change of  $\pm 180$  degrees of the synchro or resolver format signals applied to the converter input.

Options are available for all the standard line to line voltages and frequencies for either synchro or resolver inputs. Theses options together with commercial or extended temperature ranges are determined by a code following the type number (see ordering information).

An important feature of the SAC1763 series converters is that no external transformer modules are required. The transformer isolation is carried out by micro transformers which are inside the converter module *even for the 60Hz versions*.

When converters are used in control loops, it is often useful to have a voltage which is proportional to angular velocity. This voltage is available and has been brought out on all SAC1763 converters. The availability of the velocity voltage eliminates the need for a tachometer for stabilization.



### MODELS AVAILABLE

Options of the SAC1763 are available to cover all the standard synchro and resolver voltages and frequencies. In addition, options exist for standard operating temperature (0 to  $+70^{\circ}$ C) and extended operating temperature ( $-55^{\circ}$ C to  $+105^{\circ}$ C) (see ordering information).

### THEORY OF OPERATION

The SAC1763 is based upon the well proven 12-bit tracking Synchro/Resolver Converter type SDC1700. This is followed by a 12-bit precision DAC (Digital-to-Analog Converter).



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# SPECIFICATIONS (max at 25°C unless otherwise stated)<sup>1</sup>

• • • • • • • • • • • • • • • • • • •	
Model	SAC1763
ACCURACY <sup>2</sup>	±11 arc-minutes
RESOLUTION	1 part in 4096
ANALOG OUTPUT	±10V Representing ±180° 5mA is Available
OUTPUT DRIFT	0.175 arc-minutes per °C
OUTPUT RIPPLE AND NOISE	<5mV p-p
SIGNAL AND REFERENCE FREQUENCY <sup>1</sup>	60Hz, 400Hz and 2.6kHz
SIGNAL INPUT VOLTAGE (LINE TO LINE)	90V, 26V or 11.8V rms
SIGNAL IMPEDANCE	
90V Signal	$200k\Omega$ Resistive
26V Signal	58k $\Omega$ Resistive
11.8V Signal	27kΩ Resistive
REFERENCE VOLTAGE	115V, 26V or 11.8V rms
REFERENCE IMPEDANCE	
115V Reference	270kΩ
26V Reference	56kΩ
11.8V Reference	27k\$2
TRANSFORMER ISOLATION ON SIGNAL	
AND REFERENCE INPUTS	500V dc
MAX INPUT RATES FOR FULL ACCURACY	
60Hz Options	5revs/sec
400Hz Options	36revs/sec
2.6kHz Options	75revs/sec
MAX ACCELERATION ON INPUT FOR	
ADDITIONAL ERROR LESS THAN	
6 ARC-MINUTES	
60Hz Options	166°/sec <sup>2</sup>
400Hz Options	9668°/sec <sup>2</sup>
2.6kHz Options	45,528°/sec <sup>2</sup>
STEP RESPONSE (179° Step)	
(For less than 6 arc-minutes error)	
60Hz	1.5sec
400Hz	125ms
2.6kHz	50ms
VELOCITY VOLTAGE OUTPUT	
(See also Specifications on the next page)	$\pm 10V$ nominal for $\mp$ max input rate of the option
POWER SUPPLY REQUIREMENTS	+15V at 150mA
	-15V at 45mA
POWER DISSIPATION	2.93 watts
OPERATING TEMPERATURE RANGE	
Standard	0 to +70°C
Extended	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
DIMENSIONS	3.12" × 2.625" × 0.8"
	(79.4mm X 66.7mm X 20.3mm)
WEIGHT	7 ozs. (200 grams)

### NOTES

<sup>1</sup> The converters can be used over the following reference frequency ranges with no loss of accuracy. They will, however, retain the dynamic characteristics (input rate and acceleration) quoted for the particular option.

60Hz options can be used over 50Hz to 800Hz 400Hz options can be used over 400Hz to 2000Hz 2.6kHz options can be used over 2kHz to 3.5kHz <sup>2</sup> Accuracy is specfied for the following conditions:

(a) ±10% signal and reference amplitude variation.
(b) ±10% signal and reference harmonic distortion.

(c) ±5% power supply variation.

Specifications subject to change without notice.

### CONNECTING THE CONVERTER

The electrical connections to the converter are straighforward. The power lines, which must not be reversed, are  $\pm 15V$ . They must be connected to the "+15V" and "-15V" pins with the common connection to the ground pin "GND".

It is suggested that  $0.1\mu$ F and  $6.8\mu$ F capacitors be placed in parallel from +15V to GND, from -15V to GND.

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

 $\begin{array}{l} E_{S1} - S_3 = E_{RLO} - R_{HI} \sin \omega t \sin \theta \\ E_{S3} - S_2 = E_{RLO} - R_{HI} \sin \omega t \sin (\theta + 120^\circ) \\ E_{S2} - S_1 = E_{RLO} - R_{HI} \sin \omega t \sin (\theta + 240^\circ) \end{array}$ 

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

 $E_{S1} - S_3 = E_{RLO} - RHI Sin \omega t Sin \theta$  $E_{S2} - S_4 = E_{RHI} - RLO Sin \omega t Cos \theta$ 

The system reference voltage is connected to pins " $R_{HI}$ " and " $R_{LO}$ " in accordance with the above convention.

The analog output voltage representing the digital angle is between the pin "OUT" and "GND",  $\pm 10V$  corresponding to  $\pm 180$  degrees. Up to 5mA may be taken from the "OUT" pin. The relationship between the output voltage and the input angle is shown in the diagram below.



Diagram Showing Relationship Between Input and Output

Sometimes, it is required that the input/output relationship of the converter is the other way round. This can be achieved in the case of synchro options by interchanging connections "S1" and "S3". This is shown in the diagram below.



Diagram Showing Relationship Between Input and Output When "S1" and "S3" are Interchanged

### VELOCITY PIN

The analog voltage proportional to the rate of change of angle is provided between the pins VEL and GND. The variation is  $\pm 10.0V$  nominal for the maximum velocity of the option.

This pin provides a dc voltage output which is proportional to the angular velocity of the input. The voltage goes negative for an increasing digital angle and goes positive for a decreasing digital angle.

The characteristics of the velocity pin output are given in the following table.

Scaling of Output Voltage for One Fifth max Velocity	2 Volts (Nominal)
Output Voltage Temp. Coeff.	0.05%/°C of Output
Output Voltage Drift (All Models)	0 to +70°C ±50µV°C -55°C to +105°C ±100µV/°C
Linearity	0 to 100 <sup>°</sup> /sec 60Hz Options 1.5% 0 to 800 <sup>°</sup> /sec 400Hz Options 2% 0 to 1600 <sup>°</sup> /sec 2.6KHz Options 2%
Noise (0 to 2011z)	60Hz Options: 0 to 200°/sec 2mV rms 400Hz Options: 0 to 1600°/sec 2mV rms 2.6kHz Options: 0 to 3300°/sec 2mV rms
Impedance (Output)	ıΩ
max Current Available	lmA

The velocity voltage can be used in closed loop servo systems for stabilization instead of a tachometer.

The SAC1763 velocity outputs do not have the disadvantages of being inefficient at low speeds and do not need gearing required by tachometers. In addition, the output is available at no extra cost.

For other velocity output scaling and linearity consult the factory.

### **RESISTIVE SCALING OF INPUTS**

A feature of this converter is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11k $\Omega$  per extra volt of signal in series with "S1", "S2" and "S3", and 2.2k $\Omega$  per extra volt of reference in series with "R<sub>HI</sub>".

In the case of a Resolver-to-Digital Converter, add  $2.22k\Omega$  in series with "S1" and "S2" per extra volt of signal and  $2.2k\Omega$  per extra volt of reference in series with "R<sub>HI</sub>".

For example, assume that we have an 11.8V line to line, 26V reference Synchro Converter, and we wish to use it with a 60V line to line signal with a 115V reference.

In each signal input line, the extra voltage capability required is:

60-11.8=48.2V

Therefore each one of the three resistors needs to have a value of:

 $48.2 \times 1.11 = 53.5 \mathrm{k}\Omega$ 

Similarly the single resistor needed in series with " $R_{HI}$ " can be calculated as being 195.8k $\Omega$ .

The inputs of the converter can therefore be scaled as in the diagram below.



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# USING THE CONVERTERS WITH OTHER THAN THE SPECIFIED REFERENCE FREQUENCY

The converters can be used with different reference frequencies, other than those for which they are basically specified, with no resulting loss of accuracy (see below). However, they will retain the dynamic characteristics given in the specification.

Basic Option	Frequency	Range for no	Loss in Accuracy
--------------	-----------	--------------	------------------

60Hz	50Hz	→	800Hz
400Hz	400Hz	→	2000Hz
2.6kHz	2kHz	→	3.5kHz

### TRANSFER FUNCTION

The transfer functions for the three reference frequency options of the converters are shown below.

### **60Hz Options**

 $\frac{\theta_0}{\theta_1} = \frac{1.9 \times 10^5 (1 + 5.6 \times 10^{-2} \text{ s})}{\text{s}^3 + 1.03 \times 10^2 \text{ s}^2 + 1.08 \times 10^4 \text{ s} + 1.9 \times 10^5}$ 400Hz Options  $\theta_0 \qquad 8.8 \times 10^7 (1 + 6.8 \times 10^{-3} \text{ s})$ 

$$\frac{\theta_1}{\theta_1} = \frac{1}{s^3 + 8.04 \times 10^2 s^2 + 6.1 \times 10^5 s + 8.8 \times 10^7}$$

2.6kHz Options

 $\frac{\theta_0}{\theta_1} = \frac{10^9 (1 + 3.3 \times 10^{-3} \text{s})}{\text{s}^3 + 1.7 \times 10^3 \text{s}^2 + 3.303 \times 10^6 \text{s} + 10^9}$ 

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM Dimensions shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



### **APPLICATIONS OF THE SAC1763**

The SAC1763 may be used to record synchro or resolver information, from for example gyrocompasses or other navigational aids, on to equipment such as X-Y recorders, chart recorders or FM tape recorders, see below.



Diagram Showing Gyrocompass Information Being Recorded Using SAC1763

The applications of the SAC1763 are not only in measurement of synchro or resolver information but also in controlling angular movement. The diagram below shows the SAC1763 being used inside an angular control loop where the input is a dc voltage. The availability of the velocity voltage eliminates the need for an electromechanical tachometer for stabilization purposes.



Diagram Showing the SAC1763 Used in a Servo System Where the Input is a dc Voltage

### **ORDERING INFORMATION**

The full part number for all the standard converter options defining reference and signal voltage and frequency, operating temperature range and whether Synchro or Resolver format is given below. It should also be remembered that the signal and reference inputs can be resistively scaled (see section "Resistive Scaling of Inputs") and that in certain cases reference frequencies other than those specified can be used. (See section "Using the Converters with other than the Specified Reference Frequency".)

Part Number	Operating Temp. Range	L to L Voltage/Format	Ref. Voltage	Ref. Freq.
SAC1763511	0 to +70°C	11.8V Synchro	26 Volts	400Hz
SAC1763611	-55°C to +105°C	11.8V Synchro	26 Volts	400Hz
SAC1763512	0 to +70°C	90.0V Synchro	115 Volts	400Hz
SAC1763612	-55°C to +105°C	90.0V Synchro	115 Volts	400Hz
SAC1763522	0 to +70°C	90.0V Synchro	115 Volts	60Hz
SAC1763622	-55°C to +105°C	90.0V Synchro	115 Volts	60Hz
SAC1763513	0 to +70°C	11.8V Resolver	11.8 Volts	400Hz
SAC1763613	-55°C to +105°C	11.8V Resolver	11.8 Volts	400Hz
SAC1763514	0 to +70°C	26.0V Resolver	26 Volts	400Hz
SAC1763614	-55°C to +105°C	26.0V Resolver	26 Volts	400Hz
SAC1763518	0 to +70°C	11.8V Resolver	26 Volts	400Hz
SAC1763618	-55°C to +105°C	11.8V Resolver	26 Volts	400Hz
SAC1763543	0 to +70°C	11.8V Resolver	11.8 Volts	2.6kHz
SAC1763643	-55°C to +105°C	11.8V Resolver	11.8 Volts	2.6kHz
SAC1763544	0 to +70°C	26.0V Resolver	26 Volts	2.6kHz
SAC1763644	-55°C to +105°C	26.0V Resolver	26 Volts	2.6kHz
SAC1763548	0 to +70°C	11.8V Resolver	26 Volts	2.6kHz
SAC1763648	-55°C to +105°C	11.8V Resolver	26 Volts	2.6kHz

### VOL. II, 13-40 SYNCHRO & RESOLVER CONVERTERS



# BCD Output Synchro-to-Digital Converters

# SBCD1752/1753/1756/1757

### FEATURES

- BCD (Binary Coded Decimal) Output Representing 0 to 359.9° or 0 to ±179.9°
- -15V Power Supply Requirement Optional High Tracking Rate (75 revs/sec)
- Internal Microtransformers for 60Hz, 400Hz and 2.6kHz Options

Voltage Scaling with External Resistors (Unique Feature) Transformer Isolated Outputs Low Cost

MIL Spec/Hi Rel Options Available

### APPLICATIONS

Visual Display of Angular Information Valve Position Indication Antenna Monitoring Industrial Controls

### **GENERAL DESCRIPTION**

The SBCD1752, SBCD1753, SBCD1756 and the SBCD1757 are modular, continuous tracking Synchro/Resolver-to-Digital converters which employ a type 2 servo loop.

They are intended for use in both Industrial and Military applications either for displaying angular data directly, or for inputting BCD information directly into a data processing system.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in parallel Binary Coded Decimal (BCD).

Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

One of the outstanding features of these converters is the use made of precision Scott T and reference microtransformers. This has made it possible to include the transformers within the module, even for the 60Hz version as well as providing facilities for external voltage scaling.

### MODELS AVAILABLE

The four Synchro-to-Digital converters described in this data sheet, differ primarily in the areas of output format and power supply requirements.

Model <u>SBCD1752XYZ</u> is a 13-bit plus sign, BCD output converter, giving  $-180.0^{\circ}$  to  $-0.1^{\circ}$  and +0.0 to  $+179.9^{\circ}$  requiring ±15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.



Model <u>SBCD1753XYZ</u> is a 14-bit, BCD output converter, giving 0 to  $359.9^{\circ}$ , requiring  $\pm 15V$  and  $\pm 5V$  power supplies, and having an overall accuracy of  $\pm 0.2$  Degrees.

Model <u>SBCD1756XYZ</u> is a 13-bit plus sign, BCD output converter, giving  $-180.0^{\circ}$  to  $-0.1^{\circ}$  and +0.0 to  $+179.9^{\circ}$  requiring +15V and +5V power supplies, and having an overall accuracy of  $\pm 0.2$  Degrees.

Model <u>SBCD1757XYZ</u> is a 14-bit, BCD output converter, giving 0 to  $359.9^{\circ}$ , requiring +15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

The XYZ code defines the option thus:

- X signifies the operating temperature range.
- Y signifies the reference frequency.
- Z signifies the input voltage and range and whether it will accept Synchro or Resolver information.

More information about the option code is given under the heading "Ordering Information".

### **DATA TRANSFER (ALL MODELS)**

The readiness of the converters for data transfer is indicated by the state of the BUSY pin. The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the option (see Specifications table). The converter is busy when the BUSY pin is at TTL "High" level. The pulses occur for increasing and decreasing counts.

The most suitable time for transferring data is 400ns after the trailing edge of the BUSY pulse, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.

# **SPECIFICATIONS** (typical at 25°C unless otherwise stated)

-

MODELS	DELS SBCD1752		SBCD1756	SBCD1757
ACCURACY <sup>1</sup> (max Error) All Frequency Options	±0.2 Degrees	•	*	•
OUTPUT	Parallel BCD, 8TTL Loads	•	•	•
RESOLUTION	13-Bit + Sign Representing -180.0° to -0.1° and +0.0° to +179.9°	14 Bit Representing 0 to 359.9°	•	••
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz and 2.6kHz	•	• .	*
SIGNAL VOLTAGE (Line to L	.ine)			
Low Level	11.8V rms	•	•	•
High Level	90.0V rms	•	*	•
SIGNAL IMPEDANCES Low Level High Level	26kΩ (Resistive) 200kΩ (Resistive)	•	•	•
REFERENCE VOLTAGE				
Low Level	26V (11.8V Signal)	•	•	• .
High Level	115V (90V Signal)	•	•	•
REFERENCE IMPEDANCE				
Low Level	56kΩ (Resistive)		•	•
High Level	270KS2 (Resistive)	·····	•	
ISOLATION	500V dc		•	•
TRACKING RATE (min)				
60Hz	5 Revolutions Per Second	• 1	•	•
400Hz	36 Revolutions Per Second	•	•	
2.6kHz	75 Revolutions Per Second	•	•	•
Accel. Constant Ka	anna / <sup>2</sup>	• · · ·		•
60HZ 400Hz	120 000/sec <sup>2</sup>	•	•	•
2.6kHz	600,000/sec <sup>2</sup>	•	•	•
STEP RESPONSE (179° Step) (For 0.1° Error)				
60Hz	1.5sec	•	•	•
400Hz	125ms	•	•	
2.6kHz	50ms	•		•
POWER LINES	+15V @ 25mA	•	+15V @ 80mA	***
·	-15V @ 25mA	• •	+5V @ 500mA	•••
	+5V @ 500mA	•		
POWER DISSIPATION	3.25 Watts	*	3.7 Watts	***
BUSY LOGIC OUTPUT, POSI	TIVE PULSE (1 TTL Load)	•		
60Hz	3.5 to 4.5µs	•	•	
400Hz 2.6kHz	0.5 to 1.25µs 0.5 to 1.25µs	•	•	•
MAX DATA TRANSFER TIME (From 400ns After	······			
Trailing Edge of BUSY at max Velocity)				
60Hz	40µs	•	•	•
400Hz	5.0µs	· •	•	•
INHIBIT INPUT (To Inhibit)	Logic "0" 1TTL Logd	*	•	•.
TEMPERATUPE PANCE	Sope o HILLOAD			
Operating	0 to +70°C Standard	<b>*</b> .	•	*
	-55°C to +105°C Extended	•	• •	•
Storage	-55°C to +125°C	•	*	•
DIMENSIONS	3.125" x 2.625" x 0.8"	•	•	•
	(79.4 x 66.7 x 20.4mm)	•		-
WEIGHT	6.4 ozs. (180 grams)	•	6.5 ozs. (185 grams)	***

NOTES <sup>1</sup>Specified over the appropriate operating temperature range and for (a) ±10% signal and reference amplitude variation (b) 10% signal and reference harmonic distortion (c) ±5% power supply variation (d) ±10% variation in reference frequency.

•Specifications same as SBCD1752 ••Specifications same as SBCD1753 •••Specifications same as SBCD1756

Specifications subject to change without notice.

# Applying the SBCD1752/1753/1756/1757



### Data Transfer Diagram

The function of the INHIBIT pin is to enable the user to inhibit the update of the converter's output counter. This is achieved by taking the INHIBIT pin to a TTL Logic zero. If used, the INHIBIT should be applied 400ns after the trailing edge of the BUSY pulse. This will ensure that the data on the output pins is valid. The data should then be transferred and the INHIBIT released before the next BUSY pulse occurs. The worst case times allowable for data transfer in this case are shown in the Specifications under the heading of "MAX DATA TRANSFER TIME (from 400ns After Trailing Edge of BUSY at Max Velocity)". It should be noted that the application of the INHIBIT will not prevent the BUSY pulses appearing on the BUSY pin, and thus if the INHIBIT is not released by the time that the next BUSY pulse occurs, the BUSY pulse will still appear, although the internal converter loop will have been opened. Under this condition, a worst case recovery time, equivalent to that of a step of 179 degrees may be encountered (see Spec.). To avoid this and to ensure valid data transfer, the system shown in the diagram is recommended.



Suggested External Interface Circuitry

In cases where the converter is connected to a data bus or used as a peripheral, the method outlined in the above diagram is recommended. The INHIBIT is not necessary in this case, and the external "Enable" has control of the converter output.

The AC1755 mounting card described later in this data sheet contains the external components shown in the diagram.

### CONNECTING THE CONVERTER

The power lines, which should not be reversed, should be connected to "+15V", "-15V" and "+5V" in the case of the SBCD1752 and SBCD1753, and to "+15V" and "+5V" in the case of the SBCD1756 and SBCD1757, with the common connection to "GND" in all cases.

It is suggested that  $0.1\mu$ F and  $6.8\mu$ F capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

The digital output connections in the case of the SBCD1753 and SBCD1757 should be taken from the pins marked "0.1" through to "200"; these values being represented in degrees.

In the case of the SBCD1752 and SBCD1756, the data should be taken from the pins marked "0.1" through to "100", these values also being represented in degrees. In the case of these latter units the "SIGN" pin will indicate the polarity of the output, Logic "0" representing positive angles and Logic "1" representing negative angles.

In the case of a synchro, the signals are connected to  $S_1$ ,  $S_2$  and  $S_3$  according to the following convention:

### Synchro connection

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

**Resolver Connection** 

The BUSY and INHIBIT pin (if used), should be connected as described under the heading "DATA TRANSFER".

The reference connections are made to pins R<sub>HI</sub> and R<sub>LO</sub>.



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### **RESISTIVE SCALING OF INPUTS**

A unique feature of the SBCD1752/1753/1756/1757 converters is that the inputs can be resistively scaled to accommodate any value of input signal and reference voltage.

In order to calculate the values of the external scaling resistors necessary, add  $1.11k\Omega$  in series with the input per extra volt in the case of the signal, and  $2.2k\Omega$  per extra volt in the case of the reference.

For example, assume that it is required to use a standard 11.8V line to line signal, 26V reference converter with 60V line to line signal and a 115V reference. The resistors should be arranged as in the diagram.

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Note: In the case of  $R_1$ ,  $R_2$ , and  $R_3$ , the ratio error between the resistances is more critical than the absolute value. In general a 1% ratio error will give rise to an extra inaccuracy of 0.28 Degrees, while a ratio accuracy of 0.1% will give rise to an extra inaccuracy of 0.028 Degrees. The absolute value of  $R_F$  is not critical.

### **CARD MOUNTING**

All the converters can be mounted on an AC1755 mounting card. This card contains the latches and monostable, described under the "DATA TRANSFER" heading, which are necessary to transfer the data on to a computer bus system, as well as sockets for the converter. The latches have a tri-state output to facilitate ease of use. The AC1755 also contains facilities for the inclusion of input signal scaling and reference resistors as described under the heading "RESISTIVE SCALING OF INPUTS". The card uses a 22/22 0.156" pitch edge connector. The pin-out is shown below. If it is not required to use the external latches, they can be jumpered on the board.



AC1755 Mounting Card (First Angle Projection). Dimensions Shown in Inches and (mm).

Edge Pin Number	Function	Edge-Pin Letter	Function
1	R (Lo)	A	Tri-State Enable
2	R (Hi)	F	+15 Volts
3	S <sub>3</sub>	Ĥ	+15 Volts
4	S <sub>2</sub>	J	-15 Volts (3)
5	S <sub>1</sub>	K	-15 Volts (3)
6	S <sub>4</sub>	L	GND
		M	GND
13	BUSY	N	+5 Volts
15	INHIBIT	Р	+5 Volts
16	0.1	Т	8
17	0.2	U	10
18	0.4	v	20
19	0.8	W	40
20	1	x	80
21	2 ·	Y	100
22	4	Z	200 (1) SIGN (2)

NOTES

(1) SBCD1753 and SBCD1757 only

(2) SBCD1752 and SBCD1756 only

(3) SBCD1752 and SBCD1753 only

AC1755 Mounting Card Edge Connections

### **ORDERING INFORMATION**

Converters should be ordered by the appropriate part number (i.e., SBCD1752, SBCD1753, SBCD1756 or SBCD1757) followed by the appropriate option code.

If the unit is to be a Resolver-to-Digital converter, the SBCD should be replaced by RBCD in the part number.

The XYZ options are as follows:

X signifies the operating temperature range thus;

$$X = 5$$
 0 to +70°C (Commercial Temp.)

X = 6 -55°C to +105°C (Extended Temp.)

Y signifies the reference frequency thus;

- $\bar{Y} = 1$  signifies 400Hz
- Y = 2 signifies 60Hz\*
- Y = 4 signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is a Synchro-to-Digital or a Resolver-to-Digital converter. The options for Z are:

Z = 1 signifies Synchro,	signal 11.8 Volts
	reference 26 Volts
Z = 2 signifies Synchro,	signal 90 Volts
	reference 115 Volts
Z = 8 signifies Resolver,	signal 11.8 Volts
	reference 26 Volts

Thus an SBCD1753 with a commercial (0 to  $+70^{\circ}$ C) operating range, using a 400Hz, 26 volt reference with an 11.8 volt signal would be ordered as an SBCD1753511.

•For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.

In addition a 400Hz unit will work with a 2.6kHz reference and a 60Hz unit will work with a 400Hz reference; however they will have the velocity and acceleration characteristics of the lower frequency rated unit.

### **OTHER PRODUCTS**

The SBCD series of Synchro-to-Digital converters are just a few of the modules and instruments concerned with Synchro conversion manufactured by us. Some of our other products are listed below and technical data is available. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

### SYNCHRO-TO-DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4'') converter with a 12-bit natural binary output. Its overall accuracy is ±8.5 arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz. The SDC1702 is similar to the SDC1700 but has a 10-bit natural binary output and an overall accuracy of ±22 arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14-bit natural binary output and an overall accuracy of  $\pm 2.0$  arc-minutes  $\pm 11$ SB.

### TWO SPEED PROCESSORS

The TSL1612 and the TSL1729 both produce one digital output word up to 20 bits in length from the outputs of 2 Synchroto-Digital converters in a coarse/fine system. The TSL1612 is used for ratios of 9:1, 18:1 and 36:1, while the TSL1729 is programmable for all ratios from 1:1 to 63:1.



# Solid State Control Differential Transmitter

### FEATURES

Accuracy is ±4 Arc Minutes 14 Bit Resolution Small Size – 3.125" x 2.6" x 0.8" Low Power Dissipation – 1.5 Watts Mil. Spec. Versions Available

# SCDX/RCDX1623



DESCRIPTION

The SCDX/RCDX Series are solid state control differential transmitters. Their function is analogous to an electromechanical CDX except that the mechanical input of the CDX has been replaced by a binary input angle. The solid state differential transmitter accepts a digital angle input together with either a 3 wire synchro (SCDX) (or 4 wire resolver; RCDX) angle input and gives as output synchro or resolver signals representing the difference between the two input angles. Thus the outputs can be described by A sin  $\omega t \cos(\theta - \phi)$  where  $\theta$  represents the synchro or resolver input angle,  $\phi$  represents the binary input angle (14 bits) and  $\omega$  is the synchro excitation frequency.

The outputs from the SCDX resemble in their function the outputs from a conventional resolver but they are not transformer isolated. The outputs are from a pair of operational amplifiers (5.0 volts rms at maximum) which can be fed into a power amplifier and Scott transformer to provide either 3 wire synchro or 4 wire resolver outputs at appropriate voltage levels.

Both 60Hz and 400Hz versions of the SCDX series are available. The 400Hz modules have the input transformers contained inside the module for either synchro or resolver inputs. The SCDX modules for use on 60Hz do not contain the input transformers; suitable external transformers are available for either synchro or resolver inputs.

These transformers are designated STM 1671/XYZ or RTM 1671/XYZ where the X, Y and Z signify the temperature and voltage conditions.

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Figure 1.

# SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

Accuracy*	±4 arc minutes
Resolution	14 bits (1 LSB = 1.3 arc minutes)
Digital Inputs	14 bits natural binary
Digital Input Levels	TTL, DTL
Digital Input Loading	3 TTL loads
Response Time to 180° digital or synchro input step	300 micro seconds
Signal Inputs	Resolver 5.0 volts 400Hz Synchro 11.8 volts rms 400Hz Resolver 11.8 volts rms 400Hz Resolver 26.0 volts rms 400Hz Synchro 90 volts rms 60Hz or 400Hz Resolver 90 volts rms 60Hz or 400Hz Resolver 115 volts rms 60Hz or 400Hz
Signal Impedance	Low level 20K ohms L-L High level 200K ohms L-L
Transformer Isolation	500 volts DC
Output Voltage	5 volts rms into 2K ohms (min)
Carrier Phase Shift	Less than 1 degree
Power Supplies	+15 volts at 45mA -15 volts at 45mA +5 volts at 20mA
Operating Temperature Range	-55°C to +105°C or 0°C to +70°C
Storage Temperature Range	-55°C to +125°C
Warm up	Full accuracy upon switch on
Dimensions	3.125'' x 2.625'' x 0.8'' 79.4mm x 66.6mm x 20.5mm
Weight	7 oz. (200 grams)
A	

•Note: Accuracy applies over operating temperature range and for —

a) ±10% signal amplitude variations

b) 10% signal harmonic distortion

c) ±10% signal frequency variation

d) ±5% power supply variation

Specifications subject to change without notice.



# PRINTED CIRCUIT CARDS FOR SCDX/RCDX 400Hz AND 60Hz MODULES

Printed circuit cards are available for both the 400Hz and the 60Hz SCDX or RCDX modules. In the case of the 400Hz versions of the SCDX or RCDX the input transformers are contained inside the modules which are mounted on the smaller printed circuit card. For 60Hz use the input transformer module is mounted on the printed circuit card. The edge connections are shown in table 1 the connections are 22/22 way - 0.156° pitch. (Pin 3, i.e. S<sub>4</sub> is only used on AC 1656 in which case it is connected to W.)

The card type numbers are AC 1637 for mounting the 400Hz module and AC 1656 for mounting the 60Hz module and its transformer unit.



Figure 2. 400Hz SCDX Module



### Figure 3. STM 1671 and 60Hz SCDX Modules

## Applying the SCDX/RCDX1623

### USE OF THE SCDX AND RCDX

The inputs to the SCDX are two angles one as either resolver or synchro wires and the other in digital form. The output from the SCDX or RCDX is from operational amplifiers giving 5 volts RMS capable of driving into loads of 2K ohms or more and it is in resolver form. The output can in some cases be used directly or via a directly connected Scott transformer to convert to synchro three wire data. The output magnitudes represent the sine and cosine of the difference between the input angle and the digital angle.

### CONNECTIONS

The SCDX modules can be used for either synchro or resolver use and in each case they can be used at 400Hz or 60Hz.

**400Hz operation.** In the case of 400Hz operation the input transformers are contained inside the SCDX module or RCDX module. The internal connections are different for the resolver and synchro use but in both cases the input pins marked  $S_1$ ,  $S_2$  and  $S_3$  are used for the signal voltages. For resolver use  $S_1$  is the sin input,  $S_2$  is the cosine input and  $S_3$  is the common connection. For synchro use the signals are applied to the pins  $S_1$ ,  $S_2$  and  $S_3$  in rotation. The distinction between the modules is in the marking RCDX or SCDX. Different signal voltage levels are accommodated by different transformer windings and are determined by the number representing Z in the ordering code; see the back page for details. A diagram showing the pin arrangement for the 400Hz version of the SCDX and RCDX is shown in Fig. 2.

60Hz operation. In this case the signal input uses four pins to the SCDX or RCDX modules which will be marked QRST, these pins take in resolver format signals (2 volts rms max.) Pin T is common, S is plus cosine, R is plus sine, and Q is minus cosine. The pins QRST on the RCDX or SCDX module must be connected to the pins QRST on the transformer module, i.e.  $Q \rightarrow Q$  etc. In the case of 60Hz synchro use the inputs must be applied to the pins marked  $S_1$ ,  $S_2$  and  $S_3$  on the transformer module. In the case of 60Hz resolver use the sine input must be applied between  $S_1$  and  $S_3$  and the cosine input between S<sub>2</sub> and W. (The sense of the connections is such that if W and S<sub>3</sub> are regarded as common then S<sub>1</sub> and S<sub>2</sub> will be in time phase with each other in the first quadrant.) No reference input is used in this module. A diagram showing the SCDX module and the STM 1671 transformer module pin arrangement and marking is shown in Fig. 3.

Warning In no circumstances should the synchro or resolver voltages be connected directly to the pins marked QRST. The outputs are directly available from the module on the pins marked sine and cos.

Pins 1 to 14 are the TTL digital angle input pins, pin 1 is the MSB  $(180^{\circ})$ .

The power supplies and ground are as shown in Fig. 2. *The power supply lines should not be reversed.* 

PIN Nº	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
FUNCTION	Sin	Cos	<b>S4</b>	S 3	S 2	NC	NC	NC	NC	NC	NC	NC	S1	NC	+15	Bit 14	Bit 13	Bi 12	Bit 11	Bit 10	Bit 9	Bit
PIN LETTER	A	В	C	D	E	F	н	J	ĸ	ι	м	N	Ρ	R	S	T	U	۷	w	x	Y	Z
FUNCTION	NC	NC	NC	NC	NC	GD	GD	-15	-15	NC	NC	+ 5	+5	NC	NC	Bit 7	Bit	Bit 5	Bit 4	Bit 3	8;1 2	Bit 1

 TABLE 1. Edge Connections for Cards AC1637 and AC1656

 When Used to Hold SCDX or RCDX Modules

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14	0.0220

BIT WEIGHT TABLE

### APPLICATIONS

The SCDX so far described has an input angle  $\theta$  from Synchro lines and a digital input angle  $\phi$ , the output is either resolver or synchro signals representing the angle  $(\theta - \phi)$ . Alternative types of SCDX are available in which the output due to the input angles  $\theta$  and  $\phi$  is synchro or resolver signals representing  $(\theta + \phi)$ . With the availability of SCDX units which can either add or subtract the input angles a greater flexibility of application is available. A common and obvious application for the SCDX is to add computer provided angular information to synchro wires. The example of application shown here has been chosen to show how apart from coupling in and out of computer systems, the advent of angle to digital conversion and visa versa has generated applications which do not have simple electromechanical equivalents.



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Figure 4. "Gear-Box" Using SCDX Modules

Fig. 4 Shows three interconnected modules i.e. two SCDX's and one synchro to digital converter. The inputs and outputs are either three wire synchro or four wire resolver signals. Modules interconnected in this way are used to give the electrical equivalent of gear changing. K represents the angular rotation of the input signals, L represents the angular rotation of the signals coupling the output of SCDX (1) to the input of SCDX (2) and M represents the angular rotation of the coupling between the 16 bit synchro to digital converter and the SCDX (1) has been offset by "n" bits from the M.S.B. As a result of this the rotation L will be given by:-

$$L = K \pm 2^{n} K$$
-----(1)

In (1) the plus or minus sign will depend upon whether the SCDX (1) is of the type that gives out  $\theta + \phi$  or  $\theta - \phi$ .

The interconnections between the synchro to digital converter and the SCDX (2) have also been staggered by m digits from

### SYNCHRO & RESOLVER CONVERTERS VOL. II, 13-47

the M.S.B. and this means that M will be given by:-

 $M = L \pm 2^m K$ -----(2)

again the plus or minus sign will depend upon whether the SCDX (2) adds or subtracts.

Combining (1) and (2) gives,  $M = K (1 + 2^n + 2^m)$ 

For n and m up to 3 all the odd ratios from 3 - 1 to 17 - 1 are possible. For n = 0 (i.e. direct connection) using an "adding" SCDX (1) and the non-binary even ratios 6 and 10 are obtained for m = 2 and m = 3. Higher ratios can be obtained at the expense of angular resolution by taking n and m greater than 3.

If in Fig. 4 the staggering of the interconnections is reversed i.e. the M.S.B. on the synchro to digital converter is connected to the second M.S.B. on SCDX (1) reduction ratios can be obtained but there will be severe limitations on the total output excursion in angle due to the saw toothed behaviour of the input information to the SCDX's. This difficulty can be overcome by using the system of Fig. 4 in a feed-back loop. Showing the unit of Fig. 4 as a step up ratio box N in Fig. 5 an alternative method of speed reduction is obtained. With such a system however instability may occur unless the frequency response characteristic of the synchro to digital converter in Fig. 5 is shaped for the particular ratio.



Figure 5. Reduction Gearing Using Step Up in the Feedback Path

In Fig. 5 K is the input angle L is the output angle, N is the step up ratio, and the following hold: -

$$M = LN$$

$$L = K - M$$

$$= K - LN$$

$$L = \frac{K}{1 + N}$$

giving a ratio of 1 + N. The problem of shaping the frequency response of the synchro to digital converter or putting some dominant lag around the loop should not be overlooked.

An interesting application of the SCDX occurs in providing a local method of deviating or biasing a controlled system, for example a radar antenna. Fig. 6 shows a system for controlling an output rotation from a digital input. The unit marked SSCT is a solid state control transformer which is another module produced by Analog Devices. This module, the SSCT, is the equivalent of its electromechanical counterpart. It has as inputs an angle in synchro format  $\theta$  and a control angle  $\phi$  in digital form. It gives out a carrier voltage with an amplitude proportional to sin  $(\theta - \phi)$ . By using a phase sensitive detector shown as A and a D.C. motor system the control loop is formed. The output shaft will take up an angle demanded by the digital input angle  $\phi$ .



Figure 6. The Use of an SCDX to Produce an Offset Angle Inside a Control Loop

If an SCDX is inserted in the loop as shown by the dotted lines, the setting of the output angle will be determined by both the input digital angle  $\phi$  and the digital angle  $\alpha$ , being either the sum or difference according to how the SCDX is connected. The input angle  $\alpha$  applies a shift in angle equivalent to altering the mechanical connection between the antenna and the electromechanical control transmitter or adding an angle to the input demand. Such a scheme could be very useful in the initial stages of on site commissioning of equipment.

### **ORDERING INFORMATION**

The module numbers RCDX 1623 and SCDX 1623 must be followed by a code XYZ defining the requirements in more detail. X signifies temperature range, Y signifies the frequency of operation and Z determines the signal and reference voltage levels. XY and Z must be replaced by numbers following the number 1623 where: –

- X = 5 signifies temperature range 0 to 70°C
- X = 6 signifies temperature range  $-55^{\circ}C$  to  $+105^{\circ}C$
- Y = 1 signifies reference frequency of 400Hz
- Y = 2 signifies reference frequency of 60Hz
- Z = 1 signifies synchro signal voltage 11.8 volts, reference 26.0 volts (Y must equal 1)
- Z = 2 signifies synchro signal voltage 90.0 volts, reference 115.0 volts (Y may equal 1 or 2)
- Z = 3 signifies resolver signal voltage 11.8 volts, reference 11.8 volts (Y must equal 1)
- Z = 4 signifies resolver signal voltage 26.0 volts, reference 26.0 volts (Y must equal 1)
- Z = 5 signifies resolver signal voltage 90.0 volts, reference 90.0 volts (Y may equal 1 or 2)
- Z = 6 signifies resolver signal voltage 115.0 volts, reference 115.0 volts (Y may equal 1 or 2)
- Z = 8 signifies resolver signal voltage 11.8 volts, reference 26 volts (Y must equal 1)
- Z = 9 signifies resolver signal voltage 5.0 volts(SCDX only) (Y must equal 1)

EXAMPLE: RCDX 1623/514 is for a solid state control transmitter with resolver inputs, suitable for operation over the temperature range 0 to 70°C working at 400Hz with 26.0 volts signal and 26.0 volts reference.

**Transformer module.** For 60Hz operation the transformer module STM 1671/XYZ is required where the XYZ are as above.

Mounting Cards. For plug-in mounting cards order: AC 1656 - for 60Hz units, AC 1637 - for 400Hz units

# ANALOG DEVICES

# Low Profile Synchro/Resolver-to-Digital Converter

# SDC1700/1702/1704 SERIES

### FEATURES

Internal Microtransformers for 60Hz, 400Hz and 2.6kHz References Low Profile (0,4") 10-, 12- or 14-Bit Resolution for 360° High Tracking Rates (75 revs/sec) Voltage Scaling with External Resistors (Unique Feature) DC Voltage Output Proportional to Angular Velocity Low Cost Lightweight 3oz. (85 grams) MIL Spec/Hi Rel Options Available APPLICATIONS Servo Mechanisms **Retransmission Systems Coordinate Conversion** Antenna Monitoring Simulation **Industrial Controls Fire Control Systems** Machine Tool Control Systems

### **GENERAL DESCRIPTION**

The SDC1700, SDC1702 and SDC1704 are modular, continuous tracking Synchro/Resolver-to-Digital Converters which employ a type 2 servo loop.

They are intended for use in both Industrial and Military applications.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in TTL compatible, parallel natural binary.

One of the outstanding features of the converters is the use of precision Scott T and reference microtransformers. This bas made it possible to include the transformers within the module, even on the 60Hz option, and yet still maintain the profile height of 0.4''.

Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

When SDC's are used in control loops, it is often useful to have a voltage which is proportional to angular velocity. This voltage is available and has been brought out on all the SDC1700 converters.



Extended temperature range versions of all the converters are available.

### MODELS AVAILABLE

The three Synchro-to-Digital Converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model <u>SDC1702XYZ</u> is a 10-bit converter which has an overall accuracy of  $\pm 22$  arc-minutes and a resolution of 21 arc-minutes.

Model <u>SDC1700XYZ</u> is a 12-bit converter with an overall accuracy of  $\pm 8.5$  arc-minutes and a resolution of 5.3 arc-minutes.

Model <u>SDC1704XYZ</u> is a 14-bit converter with an overall accuracy of  $\pm 2.2$  arc-minutes  $\pm 1$ LSB and a resolution of 1.3 arc-minutes.

The XYZ code defines the option thus: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the input voltage and range, and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

### NOTE

For all the standard options, no external transformers are needed with these converters.

# **SPECIFICATIONS** (typical @ +25°C unless otherwise noted)

-

MODELS	SDC1702	SDC1700	SDC1704
ACCURACY <sup>1</sup> (max error)			· · · · · · · · · · · · · · · · · · ·
60Hz	±22 arc-minutes	±8.5 arc-minutes	±2.9 arc-minutes ±1LSB
400Hz	±22 arc-minutes	±8.5 arc-minutes	±2.2 arc-minutes ±1LSB
2.6kHz	±22 arc-minutes	±8.5 arc-minutes	±2.9 arc-minutes ±1LSB
RESOLUTION	10 Bits (1LSB = 21 arc-mins)	12 Bits (1LSB = 5.3 arc-mins)	14 Bits (1LSB = 1.3 arc-mins)
OUTPUT (In Parallel)	10 Bits (Natural Binary)	12 Bits (Natural Binary)	14 Bits (Natural Binary)
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz, 2.6kHz	•	•
SIGNAL VOLTAGE (Line-to-Line)			-
Low Level	11.8V rms	*	•
SIGNAL IMPEDANCES	<u>,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,</u>		
Low Level	26kΩ (Resistive)	•	•
High Level	$200k\Omega$ (Resistive)	•	•
REFERENCE VOLTAGE			
Low Level	26V (11.8V Signal)	•	•
High Level	115V (90V Signal)	•	•
REFERENCE IMPEDANCE	270kΩ (115V Signal)	*	*
	56k $\Omega$ (26V Reference)	•	•
	(Impedance is Resistive)	•	
TRANSFORMER ISOLATION	500V dc	*	•
TRACKING RATE (min)			- 00 <sup>9</sup>
60Hz	5 Revolutions Per Second		500 /sec
400Hz	50 Revolutions Per Second		12 Revolutions Per Second
A cool 1	75 Revolutions fer Second		25 Revolutions Per Second
Constant K.	•		
60Hz	1880/sec <sup>2</sup>	•	520/sec <sup>2</sup>
400Hz	$110,000/sec^{2}$	•	$36,000/sec^2$
2.6kHz	518,000/sec <sup>2</sup>	•	170,000/sec <sup>2</sup>
STEP RESPONSE (179° Step)	· · · · · · · · · · · · · · · · · · ·		
(FOF ILSE EFFOF) 60Hz	1 5sec	•	•
400Hz	125ms	•	•
2.6kHz	50ms	•	•
POWER LINES	±15V @ 25mA)	*	+15V @ 30m 4 )
	+5V @ 70mA } ±5%	•	+5V @ 85mA
POWER DISSIPATION	1.1 Watts	*	1.3 Watts
DATA LOGIC OUTPUT <sup>2</sup>	2TTL Loads SDC17026YZ	2TTL Loads SDC17006YZ	2TTL Loads on
(TTL Compatible)	4TTL Loads SDC17025YZ	4TTL Loads SDC17005YZ	All Options
BUSY LOGIC OUTPUT, POSITIVE P	PULSE (1 TTL Load)		
60Hz	9.0µs	•	9.0µs
400Hz	$2.0\mu s > \pm 30\%$	•	$2.0\mu s > \pm 30\%$
2.6kHz	2.0µs	•	1.3µs
MAX DATA TRANSFER TIME			
60Hz	40µs	₩	35µs
400Hz	5.0µs	•	3.0µs
WARM UR TIME	Logic TU I ITL Load		Logic U 2 IIL Loads
WARM UP TIME	1 sec to Rated Accuracy		
Derating	$0$ to $\pm 70^{\circ}$ C Standard	*	
Operating	$-55^{\circ}C$ to $+105^{\circ}C$ Extended	•	· · ·
Storage	-55°C to +125°C	*	•
DIMENSIONS	3.125" x 2.625" x 0.4" (79.4 x 66.7 x 10 2mm)	*	•
WEIGHT	3 075 (85 grams)	•	•
	- 000. (00 Bruilio)		

NOTES \*Specifications same as SDC1702. \*Specifications same as SDC1702. \*Specified over the appropriate operating temperature range of the option and for: (a)  $\pm 10\%$  signal and reference amplitude variation (b) 10% signal and reference Harmonic Distortion (c)  $\pm 5\%$  power supply variation (d)  $\pm 10\%$  variation in reference fractions

<sup>1</sup>It is recommended that buffers should be used if the above converters are required to drive over a distance greater than 6".

Specifications subject to change without notice.

### DATA TRANSFER (All Models)

The readiness of the converters for data transfer is indicated by the state of the BUSY pin.

The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the model and option (see specification table). The converter is busy when the BUSY pin is at a TTL "High" level. These pulses correspond to those delivered by the VCO to increment or decrement the up-down counter (see schematic diagram). Thus the pulses will occur for increasing and decreasing counts.

The most suitable time for transferring data is when the BUSY is at a logic "Lo" state, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.





### DATA TRANSFER DIAGRAM

Taking the INHIBIT to a logic "Lo" state prevents the VCO (BUSY) pulses from updating the up-down counter. However, if applied during a BUSY pulse, the INHIBIT will not become effective until the end of the BUSY pulse.

The best method of transferring the data is by applying the INHIBIT (taking it to a logic "Lo" state), waiting for at least the width of a BUSY pulse, transferring the data and releasing the INHIBIT.

Note that sustained application of the INHIBIT opens the internal control loop and the converter may take on appreciable time to recover to full accuracy when the loop is restored.

### INTERFACING WITH A COMPUTER

It is recommended that external latches are used to enable data to be transferred onto a computer data bus. One method is shown in the diagram. Using this method will mean that the latches are constantly updated by the BUSY signal, while at the same time enabling inputs to be made to the computer by means of normal data transfer procedures. The AC1755 mounting card contains these external components.





### THEORY OF OPERATION

If the unit is a Synchro-to-Digital Converter, then the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

i.e.,  $V_1 = K E_0 \sin \omega t \sin \theta$  $V_2 = K E_0 \sin \omega t \cos \theta$ 

Where  $\theta$  is the angle of the Synchro Shaft.

If the unit is a Resolver-to-Digital Converter, then the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformer will act purely as an isolator.

To understand the conversion process, then assume that the current word state of the up-down counter is  $\phi$ .

The  $V_1$  is multiplied by  $\cos \phi$  and  $V_2$  is multiplied by  $\sin \phi$  to give

 $\begin{array}{c} {\rm K} \ {\rm E}_{\rm O} \ {\rm Sin} \ \omega {\rm t} \ {\rm Sin} \ \theta \ {\rm Cos} \ \phi \\ {\rm and} \ \ {\rm K} \ {\rm E}_{\rm O} \ {\rm Sin} \ \omega {\rm t} \ {\rm Cos} \ \theta \ {\rm Sin} \ \phi \end{array}$ 



Functional Diagram of the SDC1700/2/4 Converters

These signals are subtracted by the error amplifier to give:

 $K E_{O} Sin \omega t (Sin \theta Cos \phi - Cos \theta Sin \phi)$ 

or  $K E_0$  Sin  $\omega t$  Sin  $(\theta - \phi)$ 

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin  $(\theta - \phi)$ .

When this is accomplished, the word state of the up-down counter ( $\phi$ ), equals within the rated accuracy of the converter, the synchro shaft angle  $\theta$ .

### CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are  $\pm 15V$ and 5V. They must be connected to the " $\pm 15V$ " and "5V" pins with the common connection to the ground pin GND.

It is suggested that  $0.1\mu$ F and  $6.8\mu$ F capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

The digital output is taken from pins:

1 through to 10 for the SDC1702

1 through to 12 for the SDC1700 1 through to 14 for the SDC1704

Pin 1 represents the MSB in each case. The reference con-

nections are made to pins "R<sub>H1</sub>" and "R<sub>LO</sub>".

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1 - S3} = E_{RLO - RHI} \sin \omega t \sin \theta$$
$$E_{S2 - S4} = E_{RHI - RLO} \sin \omega t \cos \theta$$

The analog voltage representing velocity is available between "VEL" and "GND".

The "BUSY" and "INHIBIT" pin (if used), should be connected as described under the heading "Data Transfer".

NOTE: If the INHIBIT pin is used (i.e., driven to 0 volts), the control loop will be opened and a finite time will be required (see spec) for the converter to recover.

### OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).





VOL. II, 13-52 SYNCHRO & RESOLVER CONVERTERS

### **RESISTIVE SCALING OF INPUTS**

A unique feature of the SDC1700 series of converters is that the inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered. In addition it should be noted that a 400Hz unit will operate from a 2.6kHz reference. It will however have the velocity and acceleration characteristics as specified for the 400Hz converter. A 60Hz converter will operate from a 400Hz reference and will have the velocity and acceleration characteristics as specified for the 60Hz converter.

To calculate the values of the external scaling resistors for a synchro converter, add  $1.11k\Omega$  in series with S1, S2 and S3 per extra volt in the case of the signal, and  $2.2k\Omega$  in the case of the reference. In the case of a resolver converter add  $2.22k\Omega$  per extra volt in series with S1 and S2 for the signal and  $2.2k\Omega$  per extra volt in series with R<sub>HI</sub> for the reference.

For example, assume that we have an 11.8 volt line to line signal/26.0 volt reference converter, and we wish to use a 60 volt line to line signal with a 115 volt reference.

Thus in each signal input line, the extra voltage capability required is:

60 - 11.8 = 48.2 volts

Therefore each resistor needs to have a value of  $48.2 \times 1.11 = 53.5 \mathrm{k}\Omega$ . In the case of the reference, the extra voltage capability required is:

115 - 26.0 = 89 volts

Therefore the resistor needs to have a value of:

 $89.0 \ge 2.2 = 195.8 \mathrm{k}\Omega$ 

Thus the inputs can be scaled as in the diagram below.



IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES.

THE ABSOLUTE VALUE OF RF IS NOT CRITICAL.

### **BIT WEIGHT TABLE**

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
- 3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10 (LSB for SDC1702)	0.3516
11	0.1758
12 (LSB for SDC1700)	0.0879
13	0.0439
14 (LSB for SDC1704)	0.0220

### VELOCITY PIN

This pin provides a voltage output which is proportional to the angular velocity of the input. The voltage goes negative for an increasing digital angle and goes positive for a decreasing digital angle.

The characteristics of the velocity pin output are given in the table below.

Scaling of Output Voltage for One Fifth max Velocity	2Volts (Nominal)
Output Voltage Temp. Coeff.	0.05%/°C of Output
Output Voltage Drift (All Models)	0 to +70°C ±50μV/°C
	-55°C to +105°C ±100μV/°C
Linearity:	0 <sup>°</sup> /sec to 800 <sup>°</sup> /sec SDC1704 400Hz 1% 0 <sup>°</sup> /sec to 100 <sup>°</sup> /sec SDC1704 60Hz 1% 0 <sup>°</sup> /sec to 800 <sup>°</sup> /sec SDC1700/2 400Hz 2% 0 <sup>°</sup> /sec to 100 <sup>°</sup> /sec SDC1700/2 60Hz 1.5%
Noise: (0 to 20Hz)	<ul> <li>@1600°/sec SDC1700/2/4</li> <li>400Hz 2mV rms</li> <li>@200°/sec SDC1700/2/4</li> <li>60Hz 2mV rms</li> </ul>
Impedance (Output)	1Ω
max Current Available	1mA

The velocity voltage can be used in closed loop servo systems for stabilization instead of a tachometer.

The SDC1700/2/4 velocity outputs do not have the disadvantages of being inefficient at low speeds and do not need gearing required by tachometers. In addition, the output is available at no extra cost.

For other velocity output scaling and linearity consult the factory.

Two examples of the use of the velocity pin are shown in the diagram below.



Diagram showing a velocity feed forward application. The SDC is used to produce the demanded velocity from Synchro form inputs.



Diagram showing the velocity voltage being used to stabilize an electro-mechanical control loop

# APPLICATIONS OF SYNCHRO-TO-DIGITAL CONVERTERS

SDCs can be used in a variety of ways in control loops as well as for the conversion of angular data into a form which is readily acceptable to digital displays or computers.

The diagram below shows an SDC being used in a digitally controlled feedback loop.



An SDC Being Used in a Digitally Controlled Feedback Loop

Such loops as shown in the diagram above require the high dynamic performance of the SDC1700 series converters. It should be noted that in this application, the SDC1700 series will replace conventional tachometers and phase sensitive detectors while at the same time provide digital position feedback.

Many synchro systems employ a two speed, geared arrangement utilizing one synchro for the fine shaft and one for the coarse. An example of this type is shown below.



Diagram Showing Coarse/Fine Synchro Processor System

In the above example, two tracking SDC's are being used to provide data for coarse/fine (two speed) data transmission systems.

The TSL1612 is a processor which combines the outputs of two SDC's to provide one output word of up to 19 bits in length.

The TSL1612 is available for any ratio between 2:1 and 36:1and provides automatic compensation for misalignment of the coarse synchro relative to its shaft. It also corrects for any overlap between the digits of the coarse and fine shafts.

### SYNCHRO & RESOLVER CONVERTERS VOL. II, 13-53

### **MEAN TIME BETWEEN FAILURES (M.T.B.F.)**

The estimated mean time between failures is given as follows:

SDC1700/2	174,000 Hours
SDC1704	167,000 Hours

Further information relating to M.T.B.F. and to the quality control and test procedures employed by us can be obtained from the factory on request.

### TRANSFER FUNCTION

The transfer function of the SDC1700/2 and SDC1704, 400Hz versions, is given below.

For the transfer functions of the other models or for a detailed analysis of those given here, please contact us.

SDC1700/2 400Hz

 $8.8 \times 10^7 (1 + 6.8 \times 10^{-3} s)$  $\theta_0$  $s^{3} + 8.04 \times 10^{2} s^{2} + 6.1 \times 10^{5} s + 8.8 \times 10^{7}$  $\theta_1$ 

SDC1704 400Hz

 $\frac{2.95 \times 10^7 (1 + 8.2 \times 10^{-3} \text{ s})}{\text{s}^3 + 8.05 \times 10^2 \text{ s}^2 + 1.95 \times 10^5 \text{ s} + 2.95 \times 10^7}$  $\theta_0$  $\theta_1$ 

### CARD MOUNTING

All the converters can be mounted on an AC1755 mounting card. This card contains the latches described under the "Data Transfer" heading, which are necessary to transfer the data on to a computer bus system, and sockets for the converter.

The latches have a tri-state output to facilitate ease of use.

The AC1755 also contains facilities for the inclusion of input signal and reference scaling resistors as described under the heading "Resistive Scaling of Inputs".

The card uses a 22/22 0.156" pitch edge connector. The pin out is shown below. If it is not required to use the external latches, they can be jumpered on the board.



z NOTE: SDC1702 does not use pins 16, 17, 18 or 19. SDC1700 does not use pins 16 and 17.

BIT 11

BIT 10

BIT 9

8 B!T

w

BIT 4

BIT 3

BIT 2

BIT 1

### ORDERING INFORMATION

19

20 21

22

Parts should be ordered by the appropriate part number (i.e.,

SDC1700, SDC1702, SDC1704) followed by the appropriate XYZ option code.

If the unit is to be a Resolver-to-Digital Converter, the SDC should be replaced by RDC in the part number.

The XYZ options are as follows:

X signifies the operating temperature range and the options are:

- X = 5 signifies 0 to +70°C (commercial) temperature.
- X = 6 signifies  $-55^{\circ}C$  to  $+105^{\circ}C$  (extended) temperature.

Y signifies the reference frequency and the options are:

- Y = 1 signifies 400Hz
- Y = 2 signifies 60Hz\*
- Y = 4 signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is an SDC or an RDC. The options are:

- Z = 1 signifies synchro, signal 11.8V rms, reference 26V rms
- Z = 2 signifies synchro, signal 90V rms, reference 115V rms
- Z = 3 signifies resolver, signal 11.8V rms, reference 11.8V rms
- Z = 4 signifies resolver, signal 26V rms, reference 26V rms
- Z = 8 signifies resolver, signal 11.8V rms, reference 26V rms

Thus, for example, an SDC1704 with a commercial (0 to +70°C) operating range, using a 400Hz, 26V reference with an 11.8V signal would be ordered as an SDC1704511.

For other than these options, consult the factory.

### CAUTIONS

Do not reverse the power supplies.

Do not connect signal and/or reference inputs to other than S1, S2, S3, S4, R<sub>HI</sub> or R<sub>LO</sub>.

Do not connect signals and/or references to a lower voltage rated converter. (Such as a 115V Synchro into a 26V Converter).

Misconnections as per the above will damage the units and void the warranty.

### OTHER PRODUCTS

The SDC1700/2/4 converters are just a few of the modules and instruments concerned with Synchro and Resolver conversion manufactured by us.

Other products are listed below and technical data is available. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

### TWO SPEED PROCESSORS

Which utilize the digital outputs of two SDCs in a 2 speed coarse/fine system to produce one combined digital word of up to 19 bits in length. The TSL1612 in particular is available for any ratio between 2:1 and 36:1.

### DIGITAL-TO-SYNCHRO CONVERTERS

Resolutions of between 10 and 14 bits are available.

### BCD OUTPUT SYNCHRO-TO-DIGITAL CONVERTERS

The SBCD1752 and SBCD1753 are converters with a BCD instead of a binary output based upon the SDC1700. They have outputs of ±180.0 degrees and 0 to 360.0 degrees respectively.

### \*50Hz Operation

For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.

# **ANALOG** DEVICES

# 16-Bit, High Accuracy Three-State Latched Output Synchro-to-Digital Converters

# SDC/RDC1721

# Matter 1 1 1 Matter 2 1 1 Matter 2 1 1 S3 Matter 2 1 S4 Matter 2 1 Matter 2 1 1 S4 Matter 2 1 Matter 2 1 1 Matter 2 1 1 Matter 2 1 1

### THEORY OF OPERATION

If the unit is a Synchro-to-Digital Converter the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

i.e.,	$V_1 = K E_0 Sin \omega t Sin \theta$	
	$V_2 = K E_0 Sin \omega t Cos \theta$	

Where  $\theta$  is the angle of the synchro shaft.

If the unit is a Resolver-to-Digital Converter, the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is  $\phi$ .

Then  $V_1$  is multiplied by  $\cos \phi$  and  $V_2$  is multiplied by  $\sin \phi$  to give:

K E<sub>O</sub> Sin  $\omega$ t Sin  $\theta$  Cos  $\phi$ 

and

K E<sub>O</sub> Sin  $\omega$ t Cos  $\theta$  Sin  $\phi$ 

These signals are subtracted by the error amplifier to give:

K E<sub>O</sub> Sin  $\omega$ t (Sin  $\theta$  Cos  $\phi$  ~ Cos  $\theta$  Sin  $\phi$ )

or  $K E_O Sin \omega t Sin (\theta - \phi)$ 

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null  $\sin(\theta - \phi)$ .

FEATURES

High Accuracy ±40 arc-sec 16-Bits Resolution Three State Latched Output Simple Data Transfer Internal Transformers Continuous Tracking—Even During Data Transfer Extended Temp Range Options Available

### APPLICATIONS

Replacing Two Speed Systems Test Equipment Servo Mechanisms Antenna Monitoring Simulation Artillery Fire Control Systems

### **GENERAL DESCRIPTION**

The SDC1721 is a 16-bit output, high accuracy, continuous tracking Synchro- or Resolver-to-Digital Converter with three state latched outputs. The converter employs a type 2 Servo Loop and is accurate to  $\pm 40$  arc-secs.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference depending on the option. The outputs will be present in TTL compatible parallel natural binary, buffered by three-state latches.

The three-state output facility not only simplifies multiplexing of more than one device onto a single data bus but also enables the "INHIBIT" to be used without opening the internal converter loop.

The SDC1721 is available in a 400Hz to 2.6kHz option as standard and contains internal transformers which provide isolation on the signal and reference inputs.

The converter requires no external trims or adjustment components.

### MODELS AVAILABLE

Options of the SDC1721 are available to cover the standard Synchro and Resolver voltages as well as standard and extended temperature ranges.

More information about the options available and their ordering code is given under the heading of "Ordering Information".

# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	SDC/RDC1721
ACCURACY <sup>1</sup>	±40 arc-seconds
RESOLUTION	16 Bits (1LSB = 19.8 arc-seconds)
OUTPUT	16-Bits Parallel Natural Binary
SIGNAL AND REFERENCE	<u> </u>
FREQUENCY	360Hz-2.9kHz
SIGNAL VOLTAGE (Line to Line)	11.8V rms
	26V rms
	90V rms
SIGNAL IMPEDANCES	200kQ min
26V Signal	$500k\Omega$ min
90V Signal	1MΩ min
REFERENCE VOLTAGE	11.8V rms
	26V rms
,	115V rms
<b>REFERENCE IMPEDANCE (Resistive)</b>	
11.8V Reference	27kΩ
26V Reference	56kΩ
115V Reference	270ks2
TRANSFORMER ISOLATION	500V dc
ALLOWABLE PHASE SHIFT	
BETWEEN SIGNAL AND	+20 dag
	2 Developing Dev Course d
TRACKING RATE (Minimum)	3 Revolutions Per Second
ACCELERATION	55.000/sec <sup>2</sup>
(For 11 SB Fror)	250ms
POWER LINES	+15V @ 45mA typ (80mA max)
FOWER LINES	-15V @ 45mA typ (80mA max)
	+5V @ 110mA typ (250mA max)
POWER DISSIPATION	1.9 Watts typ (3.65 Watts max)
DATA LOGIC OUTPUTS <sup>2</sup>	
(TTL Compatible)	6TTL Loads all Options
BUSY LOGIC OUTPUT LOADING <sup>2</sup>	2TTL Loads
BUSY LOGIC OUTPUT WIDTH <sup>2</sup>	330ns max
INHIBIT INPUT (TO INHIBIT)	Logic "0" 1TTL Load
ENABLE INPUTS (TO ENABLE) <sup>3</sup>	Logic "0" 1TTL Load
WARM-UP TIME	Ssec to Rated Accuracy
TEMPERATURE RANGE	
Operating	0 to +70°C Standard
	-55°C to +70°C Extended
Storage	-55°C to +125°C
DIMENSIONS	3.125" × 2.625" × 0.8"
	(79.4 × 66.7 × 20.3mm)
WEIGHT	3.3 ozs (93 G)

### **CONVERTER OUTLINE DIMENSIONS** AND PIN CONNECTION DIAGRAM Dimensions shown in inches and (mm).



### ABSOLUTE MAXIMUM VOLTAGES

R <sub>HI</sub> to R <sub>LO</sub>					•		•			-	± 5	<b>50</b> 0	%	٧	۲ı ۲	ns	
Signal Inputs										1	<u> </u>	09	%	٧	' rı	ns	
(Line to Line)																	
+ 15V Pin														+	- 17	v	
-15V Pin										÷				-	- 17	v	
+ 5V Pin											-	0.	41	V t	o 7	v	
Any Logic Inputs									_	0.	41	<b>√</b> 1	to	+	5.5	5V	

\*where V is voltage option

### NOTES

<sup>1</sup>Specified for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency.

<sup>2</sup> Schottky logic loading rules apply.

<sup>3</sup> ENABLE M enable most significant 8 bits. ENABLE L enable least significant 8 bits.

Specifications subject to change without notice,

When this is accomplished, the word state of the up-down counter ( $\phi$ ) equals, within the rated accuracy of the converter, the synchro shaft angle  $\theta$ .

Assuming that the "INHIBIT" is at a logic high state, then the digital word  $\phi$  will be strobed into the latches 150ns after the up-down counter has been updated. If the three state ENABLE  $\overline{M}$  and  $\overline{L}$  are at a logic low, then the digital output word will be presented to the output pins of the module.



Figure 1. Functional Diagram RDC1721

Bit Number	Weight in Degree
1 (MSB)	180.00000
2	90.00000
3	45.00000
4	22.50000
5	11.25000
6	5.62500
7	2.81250
8	1.40625
9	0.70313
10	0.35156
11	0.17578
12	0.08789
13	0.04395
14	0.02197
15	0.01099
16	0.00549

Bit Weight Table

### **DATA TRANSFER**

Data transfer from the SDC1721 is very straightforward.

Consider the timing sequence shown in the timing diagram, Figure 2 which assumes that the input to the converter is changing.

From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for 330ns while the up-down counters and latches are settling, and transfer data when it is in a low state.



Figure 2. Timing Diagram

However, a much more satisfactory method is to use the "INHIBIT" inputs. As can be seen from the functional diagram application of the "INHIBIT" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid from 330ns after the INHIBIT has been taken to a logic low state, see Figure 3. It can also be seen that this method of data transfer is valid regardless of when the INHIBIT is applied.



### Figure 3. Diagram Showing Data Transfer Using the "INHIBIT" Input

The three-state  $\overrightarrow{\text{ENABLE}}$  can be used at any time in order to present the data in the latches to the output pins.  $\overrightarrow{\text{ENABLE}} \overrightarrow{M}$ enables the most significant 8 bits while  $\overrightarrow{\text{ENABLE}} \overrightarrow{L}$  enables the least significant 8 bits.

Note that the operation of the internal converter loop cannot be affected in anyway by the logic state present on the INHIBIT and ENABLE pins.

### CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "-15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a  $0.1\mu$ F and a  $6.8\mu$ F capacitor is placed in each of the three positions from "+15V" to "GND", from "-15V" to "GND" and from "+5V" to "GND".

The digital output is taken from pins:

"1" through to "16" for the SDC1721

Pin "1" represents the MSB.

The reference connections are made to "R<sub>HI</sub>" and "R<sub>LO</sub>".

In the case of a Synchro the signals are connected to "S1", "S2" and "S3" according to the following convention:

 $E_{S1} - S3 = E_{RLO} - RHI Sin \omega t Sin \theta$ 

- $E_{S3} S2 = E_{RLO} RHI Sin \omega t Sin (\theta + 120^{\circ})$
- $E_{S2 S1} = E_{RLO RHI} Sin \omega t Sin (\theta + 240^{\circ})$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

 $E_{S1 - S3} = E_{RLO - RHI} \sin \omega t \sin \theta$  $E_{S2 - S4} = E_{RHI - RLO} \sin \omega t \cos \theta$ 

The "BUSY", "INHIBIT" and "ENABLE" pins should be connected as described under the heading "Data Transfer".

### DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Open loop gain:

$$\frac{\theta_{\text{OUT}}}{\theta_{\text{IN}}} = \frac{K_a}{S^2} \cdot \frac{1 + ST_1}{1 + ST_2}$$

Closed loop gain:

$$\frac{\theta_{\text{OUT}}}{\theta_{\text{IN}}} = \frac{1 + \text{ST}_1}{1 + \text{ST}_1 + \frac{\text{S}^2}{\text{K}_2} + \frac{\text{S}^3\text{T}_2}{\text{K}_2}}$$

Where:

$$K_a = 55,000$$

 $T_1 = 6.8$  milliseconds

 $T_2 = 1.22$  milliseconds

### ORDERING INFORMATION

When ordering please use the XYZ option code as defined below to fully specify the part number.

SDC1721XYZ

SDC = Synchro-to-Digital Converter RDC = Resolver-to-Digital Converter



Magnitude of Gain vs. Frequency



Output Angular Phase vs. Frequency

### OTHER PRODUCTS

The SDC/RDC1721 is just one of the modules and instruments concerned with Synchro and Resolver conversion manufactured by us. Full technical data and applications literature is available for all products. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

L				
Z = 1 Signal	11.8V	Reference	26V	Synchro
Z = 2 Signal	90V	Reference	115V	Synchro
Z = 3 Signal	11.8V	Reference	11.8V	Resolver
Z = 4 Signal	26V	Reference	26V	Resolver
Z = 8 Signal	11.8V	Reference	26V	Resolver

 $\dot{Y} = 1$  400 Hz Reference Frequency

 $\dot{X} = 5$  0 to 70°C Operating Temperature Range

 $X = 6 -55^{\circ}C$  to +105°C Operating Temperature Range

### VOL. II, 13-58 SYNCHRO & RESOLVER CONVERTERS



# Ultra-Low Profile (0.35") Three-State Latched Output S-to-D Converters

# SDC1725/1726

### FEATURES

Three-State Latched Output Continuous Tracking Even During Data Transfer Simple Data Transfer Facility Low Profile 0.35" (8.9mm) Internal Transformers for 60Hz, 400Hz and 2.6kHz References Signal and Reference Voltage Scaling with External Resistors High Tracking Rates (50 revs/sec) Lightweight 3.3 oz. (93 gms) MIL Spec/Hi Rel Options Available

### APPLICATIONS

Servo Mechanisms Retransmission Systems Coordinate Conversion Antenna Monitoring Simulators Industrial Controls Artillery Fire Control Systems Machine Tool Control Systems

### **GENERAL DESCRIPTION**

The SDC1725 and SDC1726 are modular, continuous tracking Synchro/Resolver-to-Digital Converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference depending on the option. The outputs will be presented in TTL compatible parallel natural binary, buffered by three-state latches.

The three-state output facility not only simplifies multiplexing of more than one device onto a single data bus but also enables the "INHIBIT" to be used without opening the internal converter loop.

Another outstanding feature of these converters is the use of precision Scott T and reference microtransformers. This has made it possible to include internal transformers, even on the 60Hz options, and yet obtain a profile height lower than any other modular Synchro/Resolver to Digital Converter currently available.



### MODELS AVAILABLE

The two Synchro/Resolver-to-Digital Converters described in this data sheet differ primarily in the areas of resolution and accuracy as follows:

<u>Model SDC1725XYZ</u> is a 12-bit converter with an overall accuracy of  $\pm 3.2$  arc-minutes  $\pm 1$ LSB and a resolution of 5.3 arc-minutes.

Model SDC1726XYZ is a 10-bit converter with an overall accuracy of ±22 arc-minutes and a resolution of 21 arc-minutes.

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

### NOTE

No external transformers are required with these converters.

# SPECIFICATIONS (typical at +25°C unless otherwise stated)

Models	SDC1725	SDC1726	
ACCURACY <sup>1</sup>			
(max Error all Options)	±3.2 arc-minutes ±1LSB	±22 arc-minutes	
RESOLUTION	12 Bits	10 Bits	
OUTPUT	12-Bits Parallel Natural Binary	10-Bits Parallel Natural Binary	
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz, 2.6kHz	•	
SIGNAL VOLTAGE (Line to Line)			
Low Level	11.8V rms	• 3	
High Level	90.0V rms	•	
SIGNAL IMPEDANCES			
Low Level	$26k\Omega$ Resistive	•	
High Level	200k12 Resistive		
REFERENCE VOLTAGE			
Low Level	26V rms (11.8V Signal)		
	115 v mis (90.0 v Signal)	· · · · · · · · · · · · · · · · · · ·	
Low Level	S6kO (26V Reference)	•	
High Level	$270k\Omega$ (115V Reference)	•	
••• <b>8</b> •• <b>•••••</b>	(Impedance is Resistive)	•	
TRANSFORMER ISOLATION	500V dc	•	
TRACKING RATE (Minimum)		· · · · ·	
60Hz Options	5 Revolutions Per Second	•	
400Hz Options	36 Revolutions Per Second	•	
2.6kHz Options	50 Revolutions Per Second	•	
ACCELERATION			
Constant Ka	2000/	•	
400Hz Options	$120.000/sec^2$	•	
2.6kHz Options	600,000/sec <sup>2</sup>	•	
STEP RESPONSE (179° Step)		· ·	
(For 1LSB Error)			
60Hz Options	1.5sec	•	
400Hz Options	125ms	• · · · · · · · ·	
2.6kHz Options	50ms	•	
POWER LINES	+15V @ 25mA		
· · ·	-15V @ 25mA		
	+5V @ 120mA		
POWER DISSIPATION	1.35 Watts	· · · · · · · · · · · · · · · · · · ·	
(TTL Compatible)	6TTL Loads All Ontions	•	
	arri t de	•	
BUSY LOGIC OUTPUT LOADING <sup>2</sup>	211L Loads	-	
BUSY LOGIC OUTPUT WIDTH*	550hs max, 200hs min	• · · · · · · · · · · · · · · · · · · ·	
INHIBIT INPUT (TO INHIBIT)	Logic "0" 1 TTL Load	•	
ENABLE INPUT (TO ENABLE)	Logic "0" 1 TTL Load	• .	
WARM UP TIME	1sec to Rated Accuracy	•	
TEMPERATURE RANGE			
Operating	0 to +70°C Standard	÷	
Storage	$-55^{\circ}$ C to $+125^{\circ}$ C	•	
DIMENSIONS	2 125" Y 2 625" Y 0 25"	•	
DIMENSIONS	(79.4 X 66.7 X 8 9mm)	•	
WEIGHT	3.3 ozs (93 gms)	•	

NOTES <sup>1</sup> Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency. <sup>2</sup> Schottky logic loading rules apply.

\*Specifications the same as for SDC1725.

Specifications subject to change without notice.
#### THEORY OF OPERATION

If the unit is a Synchro-to-Digital Converter the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

- i.e.,  $V_1 = K E_0 \sin \omega t \sin \theta$ 
  - $V_2 = K E_0 Sin \omega t Cos \theta$

Where  $\theta$  is the angle of the synchro shaft.

If the unit is a Resolver-to-Digital Converter, the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is  $\phi$ .

Then  $V_1$  is multiplied by  $\cos \phi$  and  $V_2$  is multiplied by  $\sin \phi$  to give:

K E<sub>O</sub> Sin ωt Sin  $\theta$  Cos  $\phi$ 

and

or

K E<sub>O</sub> Sin ωt Cos  $\theta$  Sin  $\phi$ 

These signals are subtracted by the error amplifier to give:

K E<sub>O</sub> Sin ωt (Sin  $\theta$  Cos  $\phi$  – Cos  $\theta$  Sin  $\phi$ )

K E<sub>O</sub> Sin  $\omega$ t Sin ( $\theta - \phi$ )

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null Sin  $(\theta - \phi)$ .

When this is accomplished, the word state of the up-down counter ( $\phi$ ) equals, within the rated accuracy of the converter, the synchro shaft angle  $\theta$ .

Assuming that the "INHIBIT" is at a logic high state, then the digital word  $\phi$  will be strobed into the latches 150ns aft<u>er</u> the up-down counter has been updated. If the three state "EN-ABLE" is at a logic low, then the digital output word will be presented to the output pins of the module.

#### DATA TRANSFER

Data transfer from the SDC1725 and SDC1726 is very straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for 330ns while the up-down counters and latches are settling, and transfer data when it is in a low state.

However, a much more satisfactory method is to use the "INHIBIT" input. As can be seen from the functional diagram application of the "INHIBIT" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid from 330ns after the INHIBIT has been taken to a logic low state. It can also be seen that this method of data transfer is valid regardless of when the INHIBIT is applied.

The three-state ENABLE can be used at any time in order to present the data in the latches to the output pins. A logic low on this pin will cause the data to be presented to the outputs. Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the INHIBIT and ENABLE pins.



11.2500

5.6250

2.8125

1,4063

0.7031

0.3516

0.1758

0.0879



Functional Diagram SDC1725

#### CONNECTING THE CONVERTER

5

6

7

8

11

10 (LSB - SDC1726)

12 (LSB - SDC1725)

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "-15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a  $0.1\mu$ F and a  $6.8\mu$ F capacitor is placed in each of the three positions from "+15V" to "GND", from "-15V" to "GND" and from "+5V" to "GND".

The digital output is taken from pins:

"1" through to "10" for the SDC1726

"1" through to "12" for the SDC1725

Pin "1" represents the MSB in each case.

The reference connections are made to "RHI" and "RLO".

In the case of a Synchro the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$\begin{split} & E_{S1 - S3} = E_{RLO - RHI} \sin \omega t \sin \theta \\ & E_{S3 - S2} = E_{RLO - RHI} \sin \omega t \sin (\theta + 120^\circ) \\ & E_{S2 - S1} = E_{RLO - RHI} \sin \omega t \sin (\theta + 240^\circ) \end{split}$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

 $E_{S1 - S3} = E_{RLO - RHI} \sin \omega t \sin \theta$  $E_{S2 - S4} = E_{RHI - RLO} \sin \omega t \cos \theta$ 

The "BUSY", "INHIBIT" and "ENABLE" pins should be connected as described under the heading "Data Transfer".

#### **RESISTIVE SCALING OF INPUTS**

A feature of this range of converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11k $\Omega$  per extra volt of signal in series with "S1", "S2" and "S3", and 2.2k $\Omega$  per extra volt of reference in series with "R<sub>H</sub>".

In the case of a Resolver-to-Digital Converter, add  $2.22k\Omega$  in series with "S1" and "S2" per extra volt of signal and  $2.2k\Omega$ per extra volt of reference in series with "R<sub>HI</sub>".

For example, assume that we have an 11.8V line to line, 26V reference Synchro Converter, and we wish to use it with a 60V line to line signal with a 115V reference.

In each signal input line, the extra voltage capability required is:

60 - 11.8 = 48.2V

Therefore each one of the three resistors needs to have a value of:

#### $48.2 \times 1.11 = 53.5 \mathrm{k}\Omega$

Similarly the single resistor needed in series with " $R_{HI}$ " can be calculated as being 195.8k $\Omega$ .

The inputs of the converter can therefore be scaled as in the diagram below.

### USING THE CONVERTERS WITH OTHER THAN THE SPECIFIED REFERENCE FREQUENCY

A 60Hz converter can be used from 50Hz to 400Hz, and a 400Hz converter can be used from 400Hz up to 2.6kHz, but they will have the dynamic characteristics specified for the unit concerned.



Dimensions shown in inches and (mm).



MATING SOCKET: CAMBION 450-3388-01-03

ORDERING INFORMATION When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

Part Number	Resolution	Operating Temp. Range	L to L Voltage/Format	Ref. Voltage	Ref. Freq.
SDC1725511	12 Bits	6 to +70°C	11.8V Synchro	26 Volts	400Hz
SDC1725611	12 Bits	-55°C to +105°C	11.8V Synchro	26 Volts	400Hz
SDC1725512	12 Bits	0 to +70°C	90.0V Synchro	115 Volts	400Hz
SDC1725612	12 Bits	-55°C to +105°C	90.0V Synchro	115 Volts	400Hz
RDC1725518	12 Bits	0 to +70°C	11.8V Resolver	26 Volts	400Hz
RDC1725618	12 Bits	-55°C to +105°C	11.8V Resolver	26 Volts	400Hz
SDC1725522	12 Bits	0 to +70°C	90.0V Synchro	115 Volts	60Hz
SDC1725622	12 Bits	–55°C to +105°C	90.0V Synchro	115 Volts	60Hz
SDC1725541	12 Bits	0 to +70°C	11.8V Synchro	26 Volts	2.6kHz
SDC1725641	12 Bits	-55°C to +105°C	11.8V Synchro	26 Volts	2.6kHz
RDC1725548	12 Bits	0 to +70°C	11.8V Resolver	26 Volts	2.6kHz
RDC1725648	12 Bits	-55°C to +105°C	11.8V Resolver	26 Volts	2.6kHz

· NOTE

For 10-bit resolution, substitute 1726 in place of 1725 in the part number above.



## Synchro/Resolver Power Amplifier

## SPA1695

#### FEATURES

5VA Output — Capable of Driving 4 Size 11 CT's Indefinite Short Circuit Protection Metal Case Acts as Heatsink Easily Mounted Voltage Sensing Facility Operation with No Derating Up to +105°C Suitable for 50 to 400Hz Operation

#### APPLICATIONS

Can Be Used With the Digital Vector Generators (DTM1716 and DTM1717) to Drive Control Transformers (CT's)



#### **GENERAL DESCRIPTION**

The SPA1695 is a two channel amplifier intended for use in conjunction with the DTM1716 and DTM1717 Digital Vector Generators for driving Control Transformers (CT's).

The unit is capable of supplying 5VA to the load and therefore can be used in cases where the internal amplifiers of a Digitalto-Synchro Converter are not sufficient (i.e., in general when the load exceeds 1.3VA).

The SPA1695 is contained in an aluminium case which has predrilled flanges for mounting purposes and excellent heatsinking properties.

The amplifier has no derating up to +105°C and is indefinitely short circuit protected at 25°C ambient.

The unit accepts resolver format inputs (Sine and Cosine) at 7 volts rms max. The output of the amplifier is in resolver format at 7 volts rms max and should be fed into suitable transformers (see ordering information).

Voltage sensing pins are provided to compensate for any voltage drop which may occur between the output of the amplifier and the output transformer.

#### MODELS AVAILABLE

The SPA1695 does not require any option numbers in order to fully specify it. The standard unit operates over the frequency range 50 to 400Hz and over the temperature range of  $-55^{\circ}C$  to  $+105^{\circ}C$ .



Implementation of the SPA1695 Amplifier

#### SCHEMATIC DIAGRAM OF AN SPA1695 AMPLIFIER BEING USED TO DRIVE A CONTROL TRANSFORMER (CT)

The above diagram shows a Digital Vector Generator being used in conjunction with the SPA1695 amplifier and external transformers to drive a Control Transformer.

The diagram illustrates the use of the Sine and Cosine feedback pins ("Sin F/B" and "Cos F/B").

#### SPECIFICATIONS (typical at 25°C unless otherwise noted)

POWER OUTPUT <sup>1</sup>	5VA
ACCURACY <sup>2</sup> (between channels)	2 arc-minutes
GAIN ACCURACY <sup>2</sup> (matching)	0.1%
INPUT VOLTAGE (per channel)	7V rms
OPERATING FREQUENCY	50 to 400Hz
INPUT IMPEDANCE	Greater than 50kΩ
INPUT BIAS CURRENT	Less than 1µA
GAIN (per channel)	Unity
INPUT DRIFT	50µV/°C
INITIAL OUTPUT OFFSET	3mV max at 25°C
CROSS OVER DISTORTION	0.01% max
DERATING OF AMPLIFIER	None up to +105°C
POWER SUPPLY REQUIREMENTS: ±15V(P) No Load ±15V(P) Average Full Load ±15V	115mA Unregulated 630mA Unregulated 15mA Regulated
WEIGHT	275 Grams (9.7 ozs)
SIZE	3.46" x 2.68" x 0.98" (88mm x 68mm x 25mm)
OPERATING TEMERATURE RANG	E -55°C to +105°C
STORAGE TEMPERATURE RANGE	E -55°C to +125°C

NOTES

1. Power output is sufficient to drive four 400Hz 90 volts line to line control transformers.

2. Valid over full temperature range of -55°C to +105°C.

Specifications subject to change without notice.

#### **CONNECTING THE SPA1695**

The diagram shows the connection of the SPA1695 to the DTM1716 or DTM1717 Digital Vector Generator, and STM1686 output and reference transformers.



#### Diagram Showing Connection of the SPA1695 to a DTM1716 or DTM1717 and STM1686

#### NOTES:

- The "Sin F/B" and the "Cos F/B" pins of the SPA1695 should be connected directly the the "Sin" and "Cos" terminals on the output transformer at the transformer. This is to compensate for any drop in voltage along the connections between the "Sin O/P" and "Cos O/P" pins of the amplifier and the transformer.
   The "+15V" and "-15V" pins of the SPA1695 should be connected
- 2. The "+15V" and "-15V" pins of the SPA1695 should be connected to a regulated power supply in order to drive the internal operational amplifiers. The "+15V(P)" and "-15V(P)" are used for the output stage and these supplies need not be a precision source. The minimum voltage when considering all tolerances including ripple, should be between 14.75 and 20 volts.
- 3. The part of the 0 volt system local to the amplifier and converter should be tapped from the "GND(SIG)" pin on the transformer and should not interconnect with any other part of the 0 volt system by any other method (see above diagram).
- In the above diagram, connection is also shown between the reference transformers, contained in the STM1686 and the Digital Vector Generator.

### USING TWO SPA1695 AMPLIFIERS IN PUSH-PULL CONFIGURATION

Twice the output power may be achieved by connecting the outputs from two SPA1695 amplifiers in push-pull configuration, the two devices being fed with out of phase signals.

For more information consult the factory.

#### ADDITIONAL HEATSINKING

Although the SPA1695 case will provide the necessary heatsink properties to allow the amplifier to provide the 5VA power output over the full temperature range, it is recommended that additional heatsinking be provided where possible.

#### ORDERING INFORMATION AND TRANSFORMER TYPE

Part number SPA1695 is sufficient to specify the amplifier – no option codes are needed.

The transformers should be ordered according to the following:

STM1686611	400Hz, Synchro output, 11.8 volt signal, 26 volt reference.
STM1686612	400Hz, Synchro output, 90 volt signal, 115 volt reference.
RTM1686618	400Hz, Resolver output, 11.8 volt signal, 26 volt reference.
STM1687622	50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

#### NOTES:

- Above transformers are suitable for use over the temperature range -55°C to +105°C.
- 2. If it is required to use the SPA1695 with Digital to Resolver converters, then use:
  - a. STM1736 for 400HZ and STM1737 for 50/60Hz systems in the case of the DRC1605 and DRC1606 converters.
  - b. STM1696 for 400Hz and STM1697 for 50/60Hz systems in the case of the DRC1705 and DRC1706 converters.

#### AMPLIFIER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

#### Dimensions shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



# 

## Solid State Control Transformer

#### FEATURES

DESCRIPTION

Accuracy ±4 Minutes of Arc Low Power Dissipation Accommodates ±12.5° Error Angle About Null Synchro Input Isolation Transformer Output Isolation No 5 Volt Line Required

The SSCT 1621 and RSCT 1621 are solid state control

transformers which perform identical functions to electro-

mechanical control transformers except that the mechanical inputs have been replaced by digital inputs. The SSCT is for

three wire synchro inputs the RSCT is for four wire resolver

inputs. In other respects they are idential. The solid state

information together with a 14 bit digital angle input and

gives out a voltage at the carrier frequency with a magnitude

proportional to the sine of the difference between the two

angles. The output can be described by A sin  $2\pi$ ft sin $(\theta - \phi)$ 

where " $\phi$ " represents the 14 bit parallel binary input angle,

" $\theta$ " represents the input angle from the three wire synchro

The scaling of the output is 0.4 volts/degree and the nominal

or four wire resolver, and f is the excitation frequency.

control transformer accepts three or four wire input

## SSCT/RSCT1621



ouput voltage range is  $\pm 5$  volts rms. This implies a span of  $\pm 12.5^{\circ}$  for full scale ouput (These voltages are for the ouput side of the output transformer which has a step down ratio of 7 to 5).

The solid state control transformer 1621 is intended for use as an error generator in follow up servo systems and for this reason the span of the output is more than adequate for all such systems. Since the output is by transformer coupling various output voltage scalings can be obtained on special order.

The solid state control transformer 1621 provides an attractive alternative to digital-to-synchro converters in follow up servo applications, the elimination of the balanced output transformers removes constraints associated with Digital to Synchro converters.



Figure 1. SSCT Schematic Diagram

## SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

Accuracy*	± 4 minutes of arc.
Resolution	14 bits (1 LSB = 1.3 arc minutes)
Digital input	14 bits natural parallel binary
Logic levels	DTL/TTL
Digital input loading	"1" 0.4 mA, "0" 1.6 mA
Scaling	0.4 volts/degree
Output signal	400 Hz: 5 volts rms (max) into 500 ohms 60 Hz: 7 volts (max) into 1K ohms
Output angle range	± 12.5 degrees
Output impedance	10 ohms
Step response time, synchro or digital input	Less than 1 milli-second
Synchro/Resolver input	-All standard 60Hz or 400Hz synchro or resolver levels (see ordering code overleaf)
Power supplies	± 15 volts at 40 mA/line
Size	3·125'' x 2·625'' x 0·8'' 79·4 mm x 66·6 mm x 20·5 mm
Operating Temperature	0 to +70 degrees C. -50 to +105 degrees C.
Storage Temperature	-50 to +125 degrees C.

\*Accuracy applies over the operating temperature range for:-

(a)  $\pm$  10% signal variation

- (b) 10% signal harmonic distortion
- (c)  $\pm 5\%$  power supply variation



Figure 2. Pin Arrangement of the SSCT1621 (400Hz)



Figure 3. Pin Arrangement of the STM1636

#### ELECTRICAL CONNECTIONS

**400 Hz operation.** The physical form and dimensions of the 1621 for 400 Hz use are shown in Fig. 2. For operation on 400 Hz both the signal input transformers and an output transformer are encapsulated within the module. The signal connections are made via the pins marked  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$ . For synchro use only the pins  $S_1$ ,  $S_2$  and  $S_3$  are used ( $S_4$  is not used). For resolver use, the sine input is applied between pins  $S_1$  and  $S_3$  and the cosine input between  $S_2$  and  $S_4$  and the polarities are such that if  $S_1$  is connected to  $S_2$  and both to common, then the voltages on  $S_3$  and  $S_4$  will be in time phase in the first quadrant.

The output which is provided on the pins marked O/P Hi and O/P Lo has a maximum voltage of 5 volts rms and is suitable for driving loads of 500 ohms or greater. This output is coupled from the output operational amplifier by means of a 7:5 step down transformer which is contained inside the SSCT module.

60 Hz operation. When used on 60 Hz the SSCT has an external transformer module for the signal input transformers (see Fig. 3). No output transformer is used on 60Hz, the output being taken directly from the pins V and U (output Hi and Lo respectively) on the SSCT module. The output voltage is 7 volts rms directly from the output of an operational amplifier (it is short-circuit proof) and is suitable for driving into loads of 1K ohms or more. The signal inputs to the module are in resolver form and connect via the pins marked Q.R.S.T. The pins Q.R.S.T. on the SSCT module must be connected to the pins marked Q.R.S.T. on the transformer module  $Q \longrightarrow Q$ etc. (see Fig. 4). The input signal connections are made to the transformer module pins marked S1 S2 S3 and W. For synchro use the signals are connected to  $S_1$   $S_2$  and  $S_3$ , no use being made of pin W. For resolver use the sine input is applied between pins  $S_1$  and  $S_3$  and the cosine input between  $S_2$  and W. The polarity should be such that if  $S_1$  and  $S_2$  are connected together and regarded as common, the voltages on  $S_3$  and W will be in time phase in the first quadrant.

The remaining pins on the transformer module i.e. U, V, RLo, RHi and Q' should not be used in this application.

The SSCT module makes use of only  $\pm 15$  volts which should be connected to the pins marked  $\pm 15$ ,  $\pm 15$  and GND on the module.

### Applying the SSCT/RSCT1621



Figure 4. Pin Arrangement of the SSCT1621 (60Hz)

Table 1 shows the bit weights for the digital inputs which connect to pins 1 through to 14. The levels required are TTL with loading of 0.4 mA for the "1" state and 1.6 mA for the "0" state.

DIT WEICHT TADI E

DIT WEIGHT TABLE		
Bit Number	Weight in Degrees	
1 (MSB)	180.0000	
2	90.0000	
3	45.0000	
4 .	22.5000	
5	11.2500	
6	5.6250	
7	2.8125	
8	1.4063	
9	0.7031	
10	0.3516	
11	0.1758	
12	0.0879	
13	0.0439	
14 (LSB)	0.0220	
	,	

#### TABLE 1.

### DIGITALLY CONTROLLED SERVO LOOP USING THE SSCT 1621

Fig. 5 shows how the SSCT would be used in a servo loop where the input angle is defined digitally as a 14 bit word into the SSCT. If the servo power drive is a D.C. motor the SSCT signal is fed into a phase sensitive detector together with the reference signal which is followed by a suitable power amplifier to drive the motor. The mechanically coupled synchro transmitter energised by the reference signal provides the angular feedback signal to the SSCT. In low power systems a bi-phase motor might be used in which case the phase sensitive detector would be omitted and the reference signal fed to the motor as well as to the synchro transmitter.



Figure 5. Servo Using S.S.C.T.

The system using the SSCT provides an alternative to the use of a digital to synchro converter followed by an electromechanical control transformer; the SSCT control loop is simpler than the DSC system and is capable of providing higher accuracy.

In addition to its use in the simple servo control loop as shown, the SSCT has application in electronic speed changing systems where it is used in conjunction with synchro to digital converters (SDC's) and solid state control transformers (SCDX's) which are also available in encapsulated modules.

The output of the 400 Hz SSCT is from a transformer contained inside the module the standard ratio of which is 7:5, but other ratios can be provided to meet special needs.

#### ORDERING INFORMATION

synchro or resolver use.

The model Number SSCT/1621 for Synchro use or RSCT/ 1621 for resolver use, must be followed by a 3 digit number XYZ which defines the operating conditions and signal levels. X defines the operating temperature range, Y determines the frequency and Z determines the signal voltage level and synchro or resolver use as follows:-

Х	=	5	signifies temperature range 0 - 70°C
Х	=	6	signifies temperature range - 55°C to +105°C
Y	=	1	signifies carrier frequency of 400 Hz
Y	=	2	signifies reference frequency of 60Hz
Z	=	1	signifies synchro signal voltage 11.8 volts (Y must = 1)
Z	=	2	signifies synchro signal voltage 90 volts $(Y = 1 \text{ or } 2)$
Z	=	3	signifies resolver signal voltage 11.8 volts (Y must = 1)
Z	=	4	signifies resolver signal voltage 26.0 volts (Y must = 1)
Z	=	5	signifies resolver signal voltage 90.0 volts $(Y = 1 \text{ or } 2)$
Z	=	,6	signifies resolver signal voltage 115.0 volts $(Y = 1 \text{ or } 2)$
Z	=	8	signifies resolver signal voltage 11.8 volts (Y must = 1)
Th des	e ex igna	ternal i <b>ted S</b>	l signal transformer module for 60 Hz use is TM 1636/XYZ or RTM 1636/XYZ for either

CARD MOUNTING A printed circuit card for holding the 400 Hz version of the 1621 is available, it is the P.C. card type AC 1637.

13

SYNCHRO & RESOLVER CONVERTERS VOL. II, 13-67





## Two Speed Processor (for Coarse/Fine Synchro/Resolver Systems)

## TSL1612

13

#### FEATURES

36:1, 18:1 or 9:1 Ratios with Same Module
No False Output Readings
Fast (500ns) Parallel Operation
Easy to Use
Up to 19-Bits Resolution
Automatic Correction for Misalignment Between Synchros or Resolvers
Low Profile - 0.4" (10.2mm)

#### APPLICATIONS

Combining the Digital Outputs of Synchro-or-Resolver-to-Digital Converters in Coarse/Fine Systems



#### **GENERAL DESCRIPTION**

The TSL1612 is used for combining the digital outputs of two Synchro- or Resolver-to Digital Converters in a mechanically or electrically geared coarse/fine system in order to produce a single unambiguous digital word representing the coarse shaft angle (see diagram).



The unit described in this data sheet provides for ratios of 9:1, 18:1 and 36:1 in a single module. However, other ratios are sometimes encountered in coarse/fine Synchro or Resolver Systems, and details of special versions of the TSL1612 for use with ratios of 2:1 thru 35:1 are available on request. The digital inputs to the TSL1612 are up to 14 bits from the fine converter and up to 7 bits from the coarse converter according to the gear ratio required. The output is up to 19bits parallel binary angle data. The module may be used with any Synchro or Resolver Converters which produce parallel binary output.

#### MODELS AVAILABLE

The standard TSL1612 which provides for ratios of 36:1, 18:1 and 9:1 has two options. They are as follows:

TSL16125000 to +70°C Operating TemperatureTSL1612600-55°C to +105°C Operating Temperature

#### OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).



MATING SOCKET: CAMBION 450-3388-01-03

SYNCHRO & RESOLVER CONVERTERS VOL. II, 13-69

<b>SPECIF</b>	<b>ICAT</b>	IONS

(typical @ +25°C unless otherwise noted)

Ratios:	36:1, 18:1, 9:1
Fine Synchro Input	Up to 14-Bits Parallel Binary Angle
Coarse Synchro Input	Up to 7-Bits Parallel Binary Angle
Logic Levels	DTL/TTL Compatible
Input Loading	2TTL Loads
Output Fan Out	5TTL Loads
Digital Output	Up to 19-Bits Parallel Binary Angle
Accuracy	±1LSB
Conversion Time	500ns
Temperature Range Storage Operating	-55°C to +125°C 0 to +70°C Standard -55°C to +105°C Extended
Power Supplies	+5V ±5% @ 600mA
Size	3.125" X 2.625" X 0.4" 79.4mm X 66.6mm X 10.2mm
Weight	3.502s. 100 grams

Specifications subject to change without notice.

#### **CONNECTING THE TSL1612**

For all ratios the fine SDC outputs connect directly to the fine TSL1612 inputs i.e. bit (1) out to bit (1) in through to bit 14 out to bit 14 in. If a Synchro- or Resolver-to-Digital Converter with a resolution of less than 14 bits is used to provide the fine input, then the unused inputs to the TSL1612 should be grounded and the output accuracy will be reduced accordingly by the same number of bits.

The connections of the coarse inputs and the TSL1612 outputs change according to the ratio to be obtained ie:-.

#### 36:1 RATIOS

Bits 1 to 7 from the coarse Synchro- or Resolver-to-Digital Converter should be connected to bits 1 to 7 on the coarse input of the TSL1612. The output is taken from bits 1 to 19.

#### 18:1 RATIOS

Bits 1 to 6 from the coarse Synchro- or Resolver-to-Digital Converter should be connected to bits 2 to 7 on the coarse input of the TSL1612. The output is taken from bits 2 to 19 (bit 2 is the MSB of the output word).

#### 9:1 RATIOS

Bits 1 to 5 from the coarse Synchro- or Resolver-to-Digital Converter should be connected to bits 3 to 7 on the coarse input of the TSL1612. The output is taken from bits 3 to 19 (bit 3 is the MSB of the output word).

#### CORRECTION FOR MISALIGNMENT OF THE COARSE AND FINE SYNCHROS OR RESOLVERS

In the two speed digital converters which receive inputs from both the coarse and fine synchros, circumstances will occur when the coarse angle determined by the most significant digits of fine synchro will conflict with the overlapping least significant digits of the coarse synchro. (This is due to the backlash in the gearing or misalignment in the synchros causing different readings at the major transition points.) Digital logic circuits for resolving this conflict are included in the TSL1612. The digital reading from the fine synchro is made to dominate in the overlapping region, and a correction is made bringing the coarse reading into line to provide an unambiguous digital representation of the angle of the coarse shaft. The TSL1612 will correct for a misalignment of (90 divided by the ratio) degrees.

#### DATA TRANSFER FROM THE TSL1612

Data transfer can be made in a number of ways in which two are listed below.

- The BUSY outputs of the fine and coarse Synchro/Resolverto-Digital Converter can be "OR"ed together to give an indication of when neither converter is being updated (see appropriate converter data sheet). The data can then be taken from the TSL1612. (The conversion time of the TSL1612 is usually insignificant.)
- 2. The INHIBIT can be applied to both the Synchro/Resolverto-Digital Converters simultaneously in order to freeze their outputs (see appropriate data sheet). When the inputs to the TSL1612 are frozen the output data can be taken. In cases where 12 bits is sufficient for the fine input, the three-state input SDC1725 Synchro/Resolver-to-Digital Converter should be used in conjunction with the SDC1726 on the coarse input. These converters allow the INHIBIT to be used without any risk of opening the internal converter tracking loop (see data sheet).

#### THEORY OF OPERATION

The theory of operation of the TSL1612 is shown in the diagram below.



FUNCTIONAL DIAGRAM OF TSL1612

#### ORDERING INFORMATION

Order:-

- TSL1612500 for 0 to +70°C Operating Temperature Range.
- TSL1612600 for -55°C to +105°C Operating Temperature Range.

## Sample/Track-Hold Amplifiers

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## Selection Guide Sample/Track-Hold Amplifiers

### **General Purpose**





### AD582

Suitable for 12-Bit Applications High Sample/Hold Current Ratio: 10<sup>7</sup> Low Acquisition Time: 6µs to 0.1% Low Charge Transfer: <2pC High Input Impedance in Sample and Hold Modes Connect in Any Op Amp Configuration Differential Logic Inputs

#### AD583

High Sample-to-Hold Current Ratio: 10<sup>6</sup> High Slew Rate: 5Vµs High Bandwidth: 2MHz Low Aperture Time: 50ns Low Charge Transfer: 10pC DTL/TTL Compatible May Be Used as Gated Op Amp Vol. I 14–27

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### AD346

Fast 2.0µS Acquisition Time to ±0.01% Vol. I Low Droop Rate: 0.5mV/ms 14-11 Low Offset Low Glitch: <40mV Aperture Jitter: 400ps Extended Temperature Range: -55°C to +125°C Internal Hold Capacitor

#### AD585

Fast 2.5µs Acquisition Time to ±0.01%	Vol. I
Low Droop Rate: 0.5mV/ms	14-31
Low Offset: 1mV	
Sample/Hold Offset Step: 1mV	
Aperture Jitter: 0.5ns	
Extended Temperature Range: -55°C to +125°C	
Internal Hold Capacitor	
APPLICATIONS	

Data Acquisition Systems Data Distribution Systems Analog Delay & Storage Peak Amplitude Measurements

14

Page

## Selection Guide Sample/Track-Hold Amplifiers

## **High Speed**



### HTC-0500

700ns Acquisition Time <750mW Power Dissipation 14-Pin DIP 0.01% Linearity

APPLICATIONS Data Acquisition Systems Data Distribution Systems Analog Delay and Storage Peak Amplitude Measurements





#### ADSHC-85

Improved SHC-85 Replacement 500ns Sample-to-Hold Transient 50µV rms Noise Low Droop Rate of 0.2mV/ms Vol. I 14-37



Very High Speed



### ADSHM-5

2nd Source-Replaces All SHM-5 Series Fast 350ns Acquisition Time to ±0.01% Aperture Uncertainty 250ps ADSHM-5K Ultra Fast 250ns Acquisition Time to ±0.01% 100ns Acquisition Time to ±0.1% Wide 12MHz Bandwidth 300Vµs Slew Rate Super Low 2nA Input Bias Current

### HTS-0010

Aperture Jitter of 5ps Acquisition Time 10ns Output Current ±40mA Slew Rate 300V/µs Vol. I 14–49

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## Selection Guide Sample/Track-Hold Amplifiers

## Very High Speed





### HTS-0025

Aperture Time to 20ps Acquisition Time to 20ns Linearity 0.01%  $10^{10}\Omega$  Input Z (HTS-0025) ±50mA Output Current Page Vol. I 14-55

### HTC-0300

Aperture Jitter of 100ps Input Range ±10V Output Current ±50mA Max Droop Rate 5μV/μs Vol. I 14-41

#### VOL. II, 14-6 SAMPLE/TRACK-HOLD AMPLIFIERS

### **High Resolution**



### AD389

Companion to High Resolution A/D Converters Fast Acquisition Time:  $2.5\mu s$  to  $\pm 0.003\%$ Low Droop Rate:  $0.1\mu V/\mu s$ Aperture Jitter: 400ps Internal Hold Capacitor Unity Gain Inverter Low Power Dissipation: 300mW



#### ANALOG GROUND + 15V -15V c Q የ HOLD CAPACITOR 1500pF VOLTAGE TO CURRENT CONVERTER 1.5mA/V +INPUT C -INPUT MODE CONTROL 6 DIGITAL GROUND SHA1144 c

### SHA1144

 High Resolution 14-Bit Sample-and-Hold Amplifier
 Vol. II

 ± 10V Range
 14-15

 50ns Aperture Delay
 14-15

 0.5ns Aperture Jitter
 4

 Acquisition Time:
 6µs Settling Time

 0.001% Max Gain Linearity Error
 Complete with Input Buffer: No External

 Components Required to Meet Rated Performance
 1

## **Orientation** Sample/Track-Hold Amplifiers

The technical data in this volume embrace high-performance (high-resolution and high-speed) sample/track-holds, in the form of encapsulated modules. As the Selection Guide indicates, data on a variety of monolithic and hybrid sample/ track-holds can be found in Volume I.

Besides the products in this section (stand-alone devices for performing the sample/track-hold function) similar functions can be found integrated into a variety of component and subsystem products. Component examples: a number of video A/D converters have on-board track-holds (MOD-1205); some high-speed D/A converters have on-board sample-holds for deglitching (MDD); and high-resolution D/A converters have deglitcher options (Deglitcher IV for the DAC1138). Besides these, sample-hold functions are inherent in Data-Acquisition Subsystems, Microcomputer Analog I/O Boards, Intelligent Measurement-and-Control Subsystems, and MACSYM.

The principal application for sample/track-hold amplifiers is to maintain an analog-to-digital converter's input constant during conversion, at a value representing the analog input as of a certain precisely known time. The characteristics of the SHA are crucial to system accuracy and the reliability of the digital data, especially in 12-bit and/or high-throughput-rate applications.

A sample/track-hold amplifier (s/h or SHA), as its name indicates, has two modes of operation, programmed by a digital control-input. In the *track*- or *sample*-mode, the output follows the input, usually with a gain of +1. When the modeinput switches to *hold*, the output of the SHA ideally retains the last value it had when the command to hold was given, and it retains that value until the logic input dictates *track* (*sample*), at which time the output ideally jumps to the input value and follows the input until the next *hold* command is given.

Analog Devices *track-bolds* and *sample-bolds* are functionally identical; they are designed to acquire input signals for either immediate hold or for a possibly extended period of tracking. They should not be confused with ac devices termed "sample-hold" that can *only* obtain quick samples and cannot track the input continuously.

#### SHA CIRCUITRY AND HARDWARE

A sample-hold amplifier usually consists of a storage capacitor, input- and output buffer-amplifiers, and a switch and its drivecircuitry. During *sample*, the circuit is connected to promote rapid charging of the capacitor. During *bold*, the capacitor is disconnected from its charging source and -ideally – retains its charge. The figure below shows a typical feedback configuration: the input buffer is a high-gain differential amplifier with a current output that charges the capacitor through the logic-controlled switch. The capacitor is unloaded by a unitygain buffer-follower. The output is fed back to the negative input (as in an op-amp follower configuration), and thus, in *sample*, the charge on the capacitor is compelled to follow the input. In *bold*, the input amplifier no longer drives the capacitor; it retains its charge, unloaded by the output follower. In another popular configuration, the capacitor is used as the feedback element of an inside-the-loop integrator (SHA1144). The highest-speed devices usually run open-loop.



Since drive current is finite, and leakage current in *bold* is not zero, the capacitance—if large—limits the slewing rate in *sample* and—if small—converts leakage current to "droop" in *bold*. In *s/h modules*, the capacitance is usually fixed, and the properties of the complete device are optimized for one condition— and so specified. In *s/h monolithic ICs*, the capacitor is omitted, and furnished by the user (both for flexibility and because good capacitors for this purpose are hard to integrate). The optimum capacitance can be selected for the specific application. In some types, (e.g., SHA1144), the gain connections are external, like those of an op amp, permitting gains other than +1.

#### PERFORMANCE

In the *sample* mode, it is useful to consider that a SHA's performance can be characterized by specifications similar to those of a closed-loop operational amplifier (offset, drift, nonlinearity, gain error, bias current, etc.), but with somewhat slower response (gain-bandwidth, slewing rate, settling time) because of the need to charge the storage capacitor.

However, during the sample-to-bold, bold, and bold-to-sample states, the dynamic nature of the mode-switching introduces a number of specifications that are peculiar to SHAs. The mostimportant of these are defined below and illustrated in the adjoining figure. They include the aperture time and its uncertainty, the sample-to-bold step, feedtbrough and droop (in hold), and acquisition time.



#### VOL. II, 14-8 SAMPLE/TRACK-HOLD AMPLIFIERS

#### DEFINITIONS

Acquisition Time is the time required by the output of the device to reach its final value, within a specified error band, after the sample command has been given. Included are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.

Aperture (Delay) Time is the time required after the *bold* command for the switch to open fully. The sample is, in effect, delayed by this interval, and the *bold* command would have to be advanced by this amount for precise timing.

Aperture Uncertainty-or Aperture (Delay) Jitter-is the range of variation in the aperture time. If the aperture time is "tuned out" by advancing the *hold* command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution. For example, the ADSHM-5K specs are 20ns and 100ps.

Charge Transfer (or offset step), the principal component of sample-to-hold offset (or pedestal), is the charge transferred to the storage capacitor via stray capacitance when switching to the hold mode. It can sometimes be reduced by lightly

coupling an appropriate-polarity version of the *bold* signal to the capacitor for cancellation. The associated voltage error  $(\Delta Q/C)$  can be reduced by using greater capacitance for storage; but this increases response time.

Droop is the change of the output voltage during *bold* as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current within a given device. In ICs, it is specified as a (droop or drift) current, in modules, a dV/dt. (Note: I = CdV/dt.)

Feedtbrough is the fraction of the input signal variation or ac input waveform that appears at the output in *bold*. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Sample-to-Hold Offset, a shift in level between the last value in sample and the value settled-to in *hold*, is the residual step error after the *charge transfer* is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as offset nonlinearity.





## Ultra Fast 0.01% Track/Sample - Hold Amplifiers

## ADSHM-5/ADSHM-5K

### FEATURES

2nd Source – Replaces all SHM-5 Series Fast 350ns Acquisition Time to ±0.01% Aperture Uncertainty 250ps ADSHM-5K Ultra Fast 250ns Acquisition Time to ±0.01% 100ns Acquisition Time to ±0.1% Wide 12MHz Bandwidth 300V/µs Slew Rate Super Low 2nA Input Bias Current

#### APPLICATIONS

Fast Data Acquisition Data Distribution Systems Peak Measurement Simultaneous Sample & Hold Analog Delay & Storage

#### **GENERAL DESCRIPTION**

The ADSHM-5 is a new ultra-fast (350ns to 0.01%) samplehold amplifier designed for use with high-speed 10- and 12-bit analog-to-digital converters, such as Analog Devices' MAH, MAS, and HAS Series, as well as other manufacturers' types.

Designed specifically to second source other SHM-5's, the ADSHM-5 is a fit, form and function equivalent for these modules.

When used in a 12-bit data acquisition system, the ADSHM-5 acquires to within 12 bits ( $\pm 0.01\%$ ) in 350ns for a 10V step change. For systems requiring 10-bit performance, the ADSHM-5 acquires to within  $\pm 0.1\%$  in just 200ns max.

Other salient features of the ADSHM-5 include 0.005% max Tracking Nonlinearity and a Small Signal Bandwidth of 5MHz.

To upgrade system performance one need only to look at the new ADSHM-5K. While sharing the same pinout and package of the ADSHM-5, this all new module utilizes the latest "stateof-the-art" hybrid techniques to offer the user the optimum in specifications. The ADSHM-5K features a maximum 12-bit acquisition time of only 250ns and 10-bit acquisition time of an astonishing 100ns max. Another improvement is in acquisition time where the input buffer must also respond to a 10V step change, such as in multiplexed applications. The total acquisition time in this application is only 350ns max. Further, the Small Signal Bandwidth has been improved from 5MHz to 12MHz.

Both units are packaged in a  $2'' \times 2'' \times 0.4''$  case. The operating temperature range is 0 to +70°C, and the power requirements are  $\pm 15V$  dc @ 75mA max.





Figure 1. ADSHM-5; ADSHM-5K Block Diagram

#### TRACK-AND-HOLD (T/H) MODE

When a unit is operated in the T/H mode, it is allowed to "track" the input signal for a period of time prior to initiating a "Hold Command." During the track period, the output follows the input, and the device functions like a unity gain amplifier.

When a Logic "0" is applied to the "Sample Control" input of the T/H, its output is frozen. This output level is held until the track mode is reestablished by a Logic "1" at the "Sample Control" input. This operation is shown graphically in Figure 4. The held output level is the voltage value at the input at the instant the hold command is applied, plus the aperture time. 14

## **SPECIFICATIONS** (typical @ +25°C and ±15V dc power supplies unless otherwise noted)

MODEL	UNITS	ADSHM-5	ADSHM-5K
ANALOG INPUT			
Input Voltage Range	V min	±10	•
Input Overvoltage, No Damage	V max	±15	•
Input Impedance	Ω	100M	10 <sup>10</sup>
Input Bias Current	nA max	250	2
Offset Adjustment Range	mV	±300	•
SAMPLE CONTROL INPUT			
Sample Mode: Logic "1" TTL <sup>1</sup>	v	+2 0 to +5 5	•
Hold Mode: Logic "0" TTI	v	0 to +0.8	•
Loading	mA	+1	•
Loading			
ANALOG OUTPUT			
Output Voltage Range	v min	±10	-
Output Current	mA	±40	150
Output Impedance	12 max	0.1	
Noise (dc to 2.5MHz)	μν	100	
ACCURACY/STABILITY DC			
Gain <sup>2</sup>	V/V	-1.000 ±0.1%	•
Gain vs. Temperature	ppm/°C	±10	•
Output Offset vs. Temperature	$\mu V/^{\circ} C max$	±30	•
Output Offset vs. Supply	mV/V	1	•
Tracking Nonlinearity	% max	±0.005	•
Output Offset Voltage, Sample Mode	mV max	±50	•
DYNAMIC RESPONSE <sup>3</sup>			
Acquisition Time <sup>4</sup> 10V to 0.1%	ns max	200	100
Acquisition Time <sup>4</sup> 10V to 0.01%	ns max	350	250
Acquisition Time <sup>5</sup> 10V to 0.01%	ns typ	1.000	300
Bandwidth Traching 2dB	M11-		10
Bandwidth, Tracking, -3dB	MHZ	5	12
Siew Rate, Tracking	v/μs	25	500
Aperture Delay Time	ns	20	100
Aperture Uncertainty Time	ps	250	100
Hold Mode Droop	μv/μs max	20	12
Hold Mode Feedthrough, dc to 500kHz	aв	70	
Sample to Hold Offset Error	mV max	±5	
POWER REQUIREMENT			
Power Supply Voltage	V dc	±15 ±0.5	•
Quiescent Current	mA max	75	•
PHYSICAL-ENVIRONMENTAL	· · · · · · · · · · · · · · · · · · ·	* <u></u>	
Operating	°c	0 to +70	•
Storage	°c	-55 to +125	•
Relative Humidity	%	Up to 100%	•
,		noncondensing	
Case Size	<i>II</i> .	2.0 X 2.0 X 0.4	•
Case Material	N/A	Diallyl Phthalate	er MIL-M-14
		Type SDG-f	
Pins	N/A	0.020" round. gol	d plated; 0.25"
		long min	• •



Figure 2. Mechanical Dimensions Dimensions shown in inches and (mm).

PIN	FUNCTION
1	SAMPLE CONTROL
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	NC
18	OFFSET ADJUST
19	+15V POWER
20	-15V POWER
21	POWER GROUND
31	ANALOG INPUT GND
32	ANALOG INPUT

Figure 3. Pin Designations

NOTES <sup>1</sup> TTL compatible. Schottky Pull Up (74S132 or equivalent) recommended to supply the 1mA required. <sup>3</sup> The Gain Error of ±0.1% can be adjusted out most easily by using the Gain Adjust of the companion

A/D converter. <sup>3</sup>When switched into Hold, about 50ns is required for switching transients to settle. This time should be allowed before initiating the first conversion.

<sup>4</sup> From Tracking Mode.

From Input Buffer

<sup>4</sup> The Analog Signal Delay from the input to the Sampling Switch is approximately 32ns. Aperture Delay time is 20ns.

\*Specifications same as ADSHM-5.

Specifications and prices subject to change without notice.

### **Applications**

Variations in the instants of sampling are called Aperture Uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled.



Figure 4. Track/Hold Waveforms

During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track-and-hold have high feedthrough rejection to prevent input to output leakage during the hold period. The droop rate is the amount the output changes during the hold period, as a result of loading on the internal hold capacitor.

When the sample control input returns to the track condition, the amount of time required for the T/H output to reestablish accurate tracking of the input signal is called the acquisition time. Figure 5 shows settling accuracy versus acquisition time for the ADSHM-5 and ADSHM5-K.



Figure 5. Acquisition Time vs. Settling Accuracy

#### SAMPLE-AND-HOLD (S/H) MODE

In the S/H mode of operation, devices are normally left in the hold condition. A very short sample pulse is applied to the sample control input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time.

#### **OPERATION WITH A/D CONVERTER**

The most common use for a track-and-hold is to place it ahead of an A/D converter to allow the digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the ADSHM series track-and-holds can allow a reduction of system aperture to 100ps. These track-and-holds may also be used for peak holding functions, simultaneous sampling A/Ds (with appropriate analog multiplexing), and other high-speed analog signal processing applications. The ADSHM series is designed to operate in either the track-and-hold or sampleand-hold modes. They perform well with the MAH series A/D converters as well as several other manufacturers' types, such as the Datel ADCEH series.

By using the circuit shown in Figure 6 using a 12-bit,  $2\mu$ s A/D converter, throughput rates of up to 450kHz can be achieved for ultra-high-speed data acquisition applications.

The maximum value of input signal frequency that can be acquired and digitized (by the A/D converter) to within  $\pm 1/2$ LSB can be determined by the following:









#### PEAK DETECTOR

Figure 7 shows a slope-sensitive circuit which is capable of finding the peaks of positive excursions of an input waveform and digitizing the result. The circuit may be implemented without the A/D converter, in which case the output is an analog level held by the T/H module that may be observed or measured in some other manner.

The comparator triggers the T/H module when the positive slope of the input signal drops below a threshold slope equal to 15V/R2C1. A minimum positive slope of 15V/R1C1 is required to arm the detector. Resistors R1 and R2 are used to provide a guard band to prevent noise from triggering the circuit. The guard-band voltage is equal to 15V X R1/R2 and is generally set to approximately 5mV to 20mV.

SAMPLE/TRACK-HOLD AMPLIFIERS VOL. II, 14-13



Figure 7. Peak Detector Circuit

#### **OFFSET ADJUSTMENT**

The maximum sample-to-hold offset error of 5mV is constant with signal level. The circuit of Figure 8 can be used to adjust this error out while in the hold mode. Please note that the ADSHM-5 or ADSHM-5K can be adjusted for zero output offset in either the tracking (sample) mode or the hold mode, but not in both at the same time.







Figure 9. Timing Diagram Acquisition Time  $T_A = ADSHM-5 = 350ns; T_A = ADSHM-5K = 250ns$ 

### RECOMMENDED FOR USE WITH THESE POPULAR A/D CONVERTERS

#### MAS SERIES



#### FEATURES

High Speed at Low Cost 8 Bits 1μs max 10 Bits 1.5μs max 12 Bits 2μs max No Missing Codes Over Temperature Low Power Industry Standard Pin Out Parallel and Serial Outputs Pin and Function Compatible with ADCEH Series





#### FEATURES

Reliable Hybrid Construction Conversion Times as Low as 1.2µs Resolution: 8, 10 and 12 Bits Exceptional Accuracy, 0.012% of FS Low Power Contained in Glass or Metal 32-Pin DIP Adjustment-Free Operation



FEATURES High Speed at Low Cost 8 Bits @ 750ns max 10 Bits @ 1µs max Monotonic Over Temperature Differential Nonlinearity ±1/4LSB typ Parallel and Serial Outputs Pin and Function Compatible with 4130, 4131

# 

## High Resolution 14-Bit Sample and Hold Amplifier SHA1144

#### FEATURES

±10V min Input/Output Range 50ns Aperture Delay 0.5ns Aperture Jitter 6μs Settling Time ±0.001% Max Gain Linearity Error Complete with Input Buffer

#### APPLICATIONS Track and Hold Feak Measurement Systems Data Acquisition Systems Simultaneous Sample-and-Hold



#### **GENERAL DESCRIPTION**

The SHA1144 is a fast sample-hold amplifier module with ac curacy and dynamic performance appropriate for applications with fast 14-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" is appropriate to allow accurate conversion by 14-bit A/D converters having conversion times of up to 150 $\mu$ s.

#### DYNAMIC PERFORMANCE

The SHA1144 was designed to be compatible with fast 14-bit A/D converters such as the Analog Devices' ADC1130 and ADC1131 series, which convert 14 bits in  $25\mu s$  and  $12\mu s$ , respectively. Maximum acquisition time of  $8\mu s$  for the SHA1144 permits high sampling rates for 14-bit conversions. The SHA1144 is guaranteed to have a maximum gain nonlinearity of  $\pm 0.001\%$  of full scale to insure 1/2LSB accuracy in 14-bit systems. When in the "hold" mode, the droop rate is  $1\mu V/\mu s$ , so the SHA1144 will hold an input signal to  $\pm 0.003\%$  of full scale (20V p-p) for over 600 $\mu s$ .

#### PRINCIPLE OF OPERATION

The SHA1144 consists basically of two high speed operational amplifiers, a storage capacitor, and a digitally controlled switch. It differs from typical sample-and-hold modules in one important respect; application versatility. The user completes the SHA1144 feedback circuit external to the module. Therefore, the module may be used in inverting or noninverting configurations and can easily be arranged to provide circuit gain of more than unity to simplify signal conditioning in a subsystem.

#### FEEDBACK CONNECTIONS

A block diagram of the SHA1144 is shown in Figure 1. The input section acts as a voltage-to-current converter, providing the current needed to charge the "hold" capacitor. The output amplifier isolates the "hold" capacitor and provides low output impedance for driving the load. Since feedback is not hardwired in the module, both inverting and noninverting input terminals are available, and the SHA1144 can be connected as a follower with unity gain or potentiometric gain, as well as inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data listed in the Specifications table is based on this operating mode.



#### Figure 1. Block Diagram – SHA1144

**SPECIFICATIONS** (typical @ +25°C, gain = +1V/V and nominal supply voltages unless otherwise noted)

OUTPUT

 $GAIN = 1 + \frac{R_2}{R_1}$ OMODE

Figure 3. Noninverting Operation

+INPUT

MODEL		SHA1144	<b>OUTLINE DIMENSIONS</b>		
ACCURACY			Dimensions shown in inches and (mm).		
Gain		+1V/V	2.015 MAX (51.18)		
Gain Error		±0.005%			
Gain Nonlinearity	_	±0.0005% (±0.001% max)	SHA1144 0.42 MAX		
Gain Temperature Coefficient (0	to +70°C)	±1ppm/°C (±2ppm/°C max)			
INPUT CHARACTERISTICS					
Input Voltage Range		±10V			
Impedance		$10^{11} \Omega \  10 pF$			
Bias Current		0.5nA max			
Initial Offset Voltage		Adjustable to Zero			
Offset vs. Temperature (0 to +70°	°C)	$\pm 30 \mu V/^{\circ} C max$			
OUTPUT CHARACTERISTICS		· · · · · · · · · · · · · · · · · · ·	Q 4		
Voltage		±10V min			
Current		±20mA min			
Resistance		<1Ω			
Capacitive load		350pF			
Noise @ 100kHz Bandwidth		70µV p-p	BOTTOM VIEW		
@ 1MHz Bandwidth		175μV p-p			
SAMPLE MODE DYNAMICS		· · · · · · · · · · · · · · · · · · ·	PIN DESIGNATIONS		
Frequency Response					
Small Signal (–3dB)		1MHz	1. TRIM 7. ANALOG GROUND		
Full Power		50kHz	2. TRIM 8. –15V		
Slew Rate		<u>3V/µs</u>	3. +INPUT 9. ANALOG OUTPUT		
SAMPLE-TO-HOLD SWITCHING			4. –INPUT 10. MODE CONTROL		
Aperture Delay Time		50ns	5. TRIM 11. DIGITAL GROUND		
Aperture Uncertainty		0.5ns	6. +15V		
Offset Step		1mV ·	<b>OFFSET ZERO ADJUST</b>		
Offset Nonlinearity		160µV	(OPTIONAL)		
Switching Transient		·			
Amplitude		50mV			
Settling Time to ±0.003%	· · · · · · · · · · · · · · · · · · ·	1µs	r-101 \		
HOLD MODE DYNAMICS			OFFSET		
Droop Rate		$1\mu V/\mu s (2\mu V/\mu s max)$	ADJUST		
Variation with Temperature		double every +10°C	10kΩ 0 2		
Feedthrough (for 20V p-p Input 0	9 1kHz)	80dB	0.5		
HOLD-TO-SAMPLE SWITCHING					
Acquisition Time to ±0.003% (	(20V Step)	6μs (8μs max)			
(	10V Step)	5µs			
±0.01% (	(20V Step)	5µs	· · ·		
· (	10V Step)	4μs	+15V		
DIGITAL INPUT					
Sample Mode (Logic "1")		+2V <logic "1"="" <+5.5v<="" td=""><td></td></logic>			
		@ 15nA max	+INPUT 0 + 10 PIN 9		
Hold Mode (Logic "0")		0V < Logic = 0.0 < +0.8V			
DOWED DEOLUDED			-15V		
POWER REQUIRED		+15V ±3% @ 60mA -15V ±3% @ 45mA	Figure 2. Unity Gain Follower		
TEMPERATURE RANGE					
Operating		0 to +70°C	R1 1k		
Storage		-55°C to +85°C			
			+15V >nn		

NOTES <sup>1</sup> Recommended Power Supply ADI Model 902-2, ±15V @ ±100mA output.

Specifications subject to change without notice.

### Applying the SHA1144

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



Figure 4. AC1580 Mounting Board

#### **OPTIONAL AC1580 EVALUATION BOARD**

The optional AC1580, shown in Figure 4, is available for benchtop-evaluation of the SHA1144.

S1, S2: Harris HI508A multiplexers (optional, not included).

#### DATA ACQUISITION APPLICATION

Successive-approximation A/D converters can generate substantial linearity errors if the analog input varies during the period of conversion; even the fast 14-bit models available cannot tolerate input signal frequencies of greater than a few Hz. For this reason, sample-and-hold amplifiers like the SHA1144 are connected between the A/D and its signal source to hold the analog input constant during conversion.

When the SHA1144 is connected to an A/D, its aperture time uncertainty, rather than the A/D's conversion time, is the factor which limits the allowable input signal frequency. The SHA1144, with a typical aperture delay time of 50ns and an uncertainty of 0.5ns, will change from the sample mode to the hold mode 50 to 50.5ns after the "1" to "0" transition of the mode control input. If the system timing is so arranged as to initiate the mode control signal 50ns early, then switching will actually occur within 0.5ns of the desired time as shown below.



#### Figure 5. Aperture Uncertainty

The maximum allowable slew rate will thus equal the quotient of the maximum allowable voltage uncertainty and the 0.5ns aperture uncertainty. For sinewave inputs, the corresponding maximum frequency is expressed by:

$$f_{max} = \left(\frac{\Delta E}{E_{FS}}\right) \left(\frac{1}{2\pi\Delta t}\right) \cong 3.18 \times 10^8 \left(\frac{\Delta E}{E_{FS}}\right)$$

where:  $\Delta E$  = the allowable voltage uncertainty E<sub>FS</sub> = the sinewave magnitude

For a system containing a SHA1144 and a 14-bit A/D with  $\pm$ 10V input signals and an allowable input uncertainty of  $\pm$ 1/2LSB ( $\pm$ 620 $\mu$ V), the maximum allowable signal frequency will be 19.7kHz.

#### POWER SUPPLY AND GROUNDING CONNECTIONS

The proper power supply and grounding connections are shown below in Figure 6.



#### Figure 6. Power Supply and Grounding Connections

The  $\pm 15V$  power supplies must be externally bypassed as shown. The capacitors should be tantalum types and should be installed as close to the module pins as possible. The analog and digital ground lines should be run separately to their respective power supply commons to prevent coupling of digital switching noise to the sensitive analog circuit section.

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#### **OPERATION WITH AN A/D CONVERTER**

Figure 7 below shows the appropriate connections between the SHA1144 and a successive approximation A/D converter in block diagram form.



Figure 7. SHA1144 and A/D Connections

The resulting timing sequence at the start of conversion is illustrated in Figure 8.



#### Figure 8. A/D and SHA Timing at Start of Conversion

Note that the leading edge of the convert command pulse causes the converter's STATUS output to go to Logic "0" which in turn switches the SHA1144 from sample to hold. As discussed previously, the typical SHA1144 actually changes modes 50 to 50.5ns after the "1" to "0" transition of the mode control input. This mode switching causes a transient on the output terminal which decays to within 0.003% of the final value in approximately 1 $\mu$ s. Once the transient has settled, the convert command input is returned to Logic "0" and the conversion proceeds. As shown in Figure 9, the STATUS signal returns to Logic "1" and the SHA1144 returns to the sample mode at the end of conversion. Within 6 $\mu$ s, it will have acquired the input signal to 0.003% accuracy and a new conversion cycle may be started.



Figure 9. A/D and SHA Timing at End of Conversion

#### **OPERATION WITH AN A/D AND MULTIPLEXER**

The subsystem of Figure 10 may also be connected to a multiplexer like the Harris HI508A as shown below.



Figure 10. A/D, SHA, and MPX Connections

The leading edge of the convert command pulse sets the STATUS output to Logic "0" thereby switching the SHA1144 to "hold"; the corresponding change to Logic "1" of the STATUS output increments the binary counter and changes the multiplexer address. Since the SHA1144's aperture time is small with respect to the multiplexer switching time, it will have switched to the hold mode before the multiplexer actually changes channels. The multiplexer switching transients will settle out long before the SHA returns to "sample" at the end of conversion. The timing sequence described above is illustrated in Figure 11.



Figure 11. A/D, SHA, and MPX Timing

This method of sequencing the multiplexer may be altered to permit random addressing or addressing in a preset pattern. The timing of the multiplexer address changes may also be altered but consideration should be given to the effects of feedthrough in the SHA1144. Feedthrough is the coupling of analog input signals to the output terminal while the SHA is in "hold". Large multiplexer switching transients occuring during A/D conversion may introduce an error.

# 

## Ultra High Speed Sample/Track-and-Hold Amplifiers

#### FEATURES

20ps Aperture Uncertainty (THS) 25 or 100ns Acquisition Times 0.01% Linearity DC Coupled High Input Z Buffer

#### APPLICATIONS

Data Acquisition Systems Peak Measurement Systems Simultaneous Sample & Hold Analog Delay & Storage





#### **GENERAL DESCRIPTION**

The THC-0300 and THS-0025 Sample/Track-and-Hold Amplifiers offer designers a choice of modules which can best meet the needs for various kinds of applications.

The THS-0025 has an acquisition time of 25ns and is capable of sample rates of 30MHz or higher for use in systems requiring this type of performance. The THC-0300 is not as fast as its companion T/H, but offers low droop rates, high output drive, and low feedthrough for situations which need those parameters. The combination of the two devices allows the system designer to make economical tradeoffs in choosing the precise characteristics needed for his design.

Both units feature high input impedance buffer amplifiers. The HTS-0025 is an "open-loop" T/H and achieves its speed with a dc-coupled Schottky diode sampling bridge; the "closed loop" HTC-0300 uses MOS FET switches.

#### APPLICATIONS

The most common use for a track and hold is to place it ahead of an A/D converter to allow the digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the THS-0025 can allow a reduction of system aperture to 20ps while THC-0300 units provide 100ps. These track and holds may also be used for peak holding functions, simultaneous sampling A/D's (with appropriate analog multiplexing), and other high speed analog signal processing applications. These modules have been used to construct 13-bit A/D converters with word rates as high as 10MHz. The THS/THC series is designed to operate in either the trackand-hold or sample-and-hold modes. They perform well with the MAS series' A/D converters.

#### TRACK-AND-HOLD (T/H) MODE

When a THS/THC unit is operated in the T/H mode, it is allowed to "track" the input signal for a period of time prior to initiating a "hold command". During the track period, the output follows the input, and the device functions as an amplifier. In the THC-0300, a resistor-gain-programmable op amp provides this function.

When a Logic "1" is input to the "hold command" input of the T/H, its output is frozen. This output level is held until the track mode is reestablished by a Logic "0" at the "hold command" input. This operation is shown graphically in Figure 1. The held output level is the voltage value at the input at the instant the hold command is applied, plus the aperture time.

Variations in the instants of sampling are called aperture uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled.

During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track and hold have high feedthrough rejection to prevent input to output leakage during the hold period. The droop rate is the amount the output changes during the hold period, as a result of loading on the internal hold capacitor.



Figure 1. Track-and-Hold Operation

## **SPECIFICATIONS** (typical at 25°C and nominal supply voltages)

-

		FAST	ULTRA FAST
MODEL	UNITS	THC 0200	TUC.0025
	UNITS	140-0300	143-0023
DYNAMIC CHARACTERISTICS		100	ar
Acquisition Time (to 0.1%)	ns MUz	100	25
Sample Rate (max)	MHZ	5 18	30
FCI	115	9	6
Settling Time THC to 0.1% THS to 1%	ns	80	15
(See Figure 2)	115		15
Bandwidth (Small Signal 3dB)	MHz	12	60
Slew Rate	V/μs	300	300
Aperture Uncertainty	ps max	100	20
Harmonic Distortion, 500kHz THC, 5MHz THS	dB	68	
(dc to 5MHz THS)	dB	63	65
Droop Rate	μV/μs	12	5000
ACCURACY/STABILITY DC			· · · · · · · · · · · · · · · · · · ·
Gain	V/V	–1 ±2% (Pin 6 to Pin 15)	0.975
Gain vs. Temperature	ppm/°C	10	5
Zero Offset Voltage		Adjustable to Zero	•
Offset vs. Temperature	ppm/°C	10	30
Linearity	%	±0.01	•
INPUT			
Voltage .	V max	±10	
Impedance	52	10-3	1.
Bias Current	nA	0.05	
OUTPUT			
Voltage	V max	±10	±2 (No Load)
Current	mA	$\pm 50$	50 (Output 1 Bin 21)
Impedance		Less than 0.0112 @ dc	$75\Omega$ (Output 1, Pin 21) $75\Omega$ (Output 2, Pin 22)
Noise (dc to 15MHz THS) (dc to 2.5MHz THC)	μV rms	100	200
HOLD COMMAND (DIGITAL INPUTS)			(TTL or ECL Offered as no cost Options)
TTL Single Line Input (2 Std. TTL Loads)			
"0" = Sample/Track		0 to +0.4V	•
"1" = Hold		+2.4 to +5V	•
ECL		Single Line Input <sup>2</sup>	Two Line Complementary <sup>3</sup>
"0" = Sample/Track	v	-1.7	*
"1" = Hold	v	-0.8	• • · · · · · · · · · · · · · · · · · ·
POWER REQUIREMENTS		· · · · · · · · · · · · · · · · · · ·	
+15V ±5% (THC) +12V to +15V (THS)	mA max	90	100
-15V ±5% (THC) -12V to -15V (THS)	mA max	80	100
+5V ±5% (THS) TTL Option	mA max	N/A	20
-5.2V ±5% (THS)	mA max	N/A	80
-5.2V ±5% (THS) ECL Option	mA max	N/A	24
Power Supply Rejection Ratio ±15V	mV/V max	10	20
TEMPERATURE RANGE			
Operating	°C	0 to +70	
Storage	°C	-55 to +125	l
PHYSICAL CHARACTERISTICS			
Case	- • · · · · · · · · · · · · · · · · · ·	diallyl phthalate per MIL-	• ·
		M-14 type SDG-F	

NOTES <sup>1</sup> Sample rates shown are a guide only and are based on system acquisition times—not logic speed. These rates can be exceeded with acquisition time trade-offs.

<sup>2</sup> These inputs are unterminated. An external pull down resistor should be used when driven by ECL 10k logic

source. <sup>3</sup> These inputs are each terminated with a  $330\Omega$  pull down resistor to -5.2V.

\*Specifications same as THC-0300.

Specifications subject to change without notice.

#### **OUTLINE DIMENSIONS**



When the hold command input returns to the track condition, the amount of time required for the T/H output to reestablish accurate tracking of the input signal is called the acquisition time. Figure 2 shows settling accuracy versus acquisition time. Figure 3 shows superimposed photographs of the input and output waveforms of a THS-0025 operated as a track-andhold amplifier. Note that the output re-acquires the input just 12ns after the end of the hold time.



Figure 2. Acquisition Time vs. Settling Accuracy

# 0.2V/DIV 20ns/DIV

10MHz SINE WAVE INPUT

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Figure 3. Track-and-Hold Operation (THS-0025)

#### SAMPLE AND HOLD (S/H) MODE

In the S/H mode of operation, devices are normally left in the hold condition. A very short sample pulse is applied to the hold command input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time. For small sample-to-sample variations, a pulse width as narrow as 12ns may be used for THS-0025 units and 80ns for THC-0300 units. For greater accuracy, sample pulses should be wider (see Figure 2).

In general, however, the pulse width to the THS-0025 should be 15ns to 50ns, depending on required accuracy. Figure 4 shows the input and output waveforms of a THS-0025 used in the S/H mode.



125kHz SINE WAVE INPUT

1µs/DIV (SAMPLE WINDOW IS 20ns) Figure 4. Sample-and-Hold Operation (THS-0025)

#### APPLICATION NOTES

Figure 5 shows a slope sensitive circuit which is capable of finding the peaks of positive excursions of an input waveform and digitizing the result. The circuit may be implemented without the A/D converter, in which case the output is an analog level held by the T/H module that may be observed or measured in some other manner.



Figure 5. Peak Detector (THC-0300)

The comparator triggers the T/H module when the positive slope of the input signal drops below a threshold slope equal to 15V/R2C1. A minimum positive slope of 15V/R1C1 is required to arm the detector. Resistors R1 and R2 are used to provide a guard band to prevent noise from triggering the circuit. The guardband voltage is equal to 15V X R1/R2 and is generally set to approximately 5 to 20mV.



Figure 6. A/D Conversion System (THC)

Throughput Rate Overall Accuracy Resolution	Greater than 400kHz 0.05% One Part in 1024 (10 Bit)
Aperture Uncertainty	100ps
Analog Input	Digital Output
0V	0000000000
+5.000V	1000000000
+9.990V	. 1111111111

#### Table I. Capsule Performance for the A/D System

Analog Devices' THC series track-and-holds are designed to interface directly with the MAS series A/D converters as well as other commercially available modular A/Ds. In the above application, the THC module is used to acquire the analog signal to be converted and hold the sampled output over a much longer time period to permit the A/D module to accurately encode the analog data sample. In this way, the system aperture time is reduced to less than 100ps, and analog bandwidths up to the Nyquist limit may be accurately digitized.







Figure 8. Sample/Track-and-Hold THS-0025 Block Diagram



Figure 9. Optional Offset Adjustments

#### ORDERING INFORMATION

- Order THS-0025 TTL, THS-0060 TTL, or THS-0225 TTL for TTL Hold Command Option.
- Order THS-0025 ECL, THS-0060 ECL, or THS-0225 ECL for Balanced ECL Hold Command Input.
- Order THC-0300, THC-0750, THC-1500 as required. All have available TTL and ECL Logic Inputs.

## **Data Acquisition Subsystems**

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## Selection Guide Data Acquisition Subsystems







### AD362

16 Single-Ended or 8 Differential Channels with Switchable Mode Control

True 12-Bit Precision: Nonlinearity ≤±0.005% High Speed: 10μs Acquisition Time to 0.01% Complete and Calibrated: No Additional Parts Required

Small, Reliable: 32-Pin Hermetic Metal DIP Versatile: Simple Interface to Popular Analog-to-Digital Converters

High Differential Input Impedance ( $10^{10}\Omega$ ) and Common-Mode Rejection (80dB) Fully Protected Multiplexer Inputs

#### AD363

Complete System in Reliable IC Form	Vol. I
Small Size	15-13
16 Single-Ended or 8 Differential Channels	
with Switchable Mode Control	
Versatile Input/Output/Control Format	
Short-Cycle Capability	
True 12-Bit Operation: Nonlinearity $\leq \pm 0.012\%$	
Guaranteed No Missing Codes Over Temperature	
Range	

High Throughput Rate: 30kHz Low Power: 1.7W

### AD364

Complete Data Acquisition System in 2-Package IC Form

Full 8- or 16-Bit Microprocessor Bus Interface

16 Single-Ended or 8 Differential Channels with Switchable Mode Control

True 12-Bit Operation: Nonlinearity  $\leq \pm 0.012\%$ Guaranteed No Missing Codes Over Specified

Temperature Range

High Throughput Rate: 20kHz

Fast Successive Approximation Conversion: 25µs

Buried Zener Reference for Long-Term Stablility and Low Gain TC

Small Size: Requires Only 2.8 Square Inches Short Cycle Capability

Low Power: 1.4W

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### **DAS1128**

**Complete Data Acquisition System** 12-Bit Digital Output 16 Single or 8 Differential Analog Inputs **High Throughput Rate** Selectable Analog Input Ranges Versatile Input/Output/Control Format Low 3 Watt Power Dissipation Small 3" × 4.6" × 0.375" Module

#### Page Vol. II 15-5

### DAS1152/DAS1153

14-Bit & 15-Bit Sampling A/D Converter	Vol. II
Complete with High Accuracy Sample/Hold and A/D Converter	15-13
Differential Nonlinearity: ±0.002% FSR max (DAS1153)	
Nonlinearity: DAS1152: ±0.005% FSR max DAS1153: ±0.003% FSR max	
Low Differential Nonlinearity T.C.: ±2ppm/°C max High Throughput Rate: 25kHz min (DAS1152) High Feedthrough Rejection: -96dB Byte-Selectable Tri-State Buffered Outputs Internal Gain & Offset Potentiometers Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules	,

### DAS1155/DAS1156

14-Bit & 15-Bit Low Level Data Acquisition System
Functionally Complete:
Includes Instrumentation Amplifier, Sample/Hold
Amplifier, and Analog-to-Digital Converter
Differential Nonlinearity: ±0.002% FSR max
(DAS1156)
Guaranteed Nonlinearity: ±0.005% FSR (DAS1155)
±0.003% FSR (DAS1156)
High Common-Mode Rejection: - 80dB (up to
500Hz)

High Feedthrough Rejection: -96dB

Resistor Programmable Gain: 1V/V to 1000V/V Byte Selectable Tri-State Buffer Outputs Internal Gain and Offset Potentiometers

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**Complete Data Acquisition System** 

16 Single or 8 Differential Analog Inputs

**FEATURES** 

12-Bit Digital Output

High Throughput Rate Selectable Analog Input Ranges Versatile Input/Output Control Format Low 3 Watt Power Dissipation Small 3" x 4.6" x 0.375" Module

### Low-Cost, High Speed Data Acquisition Module

# DAS1128



#### **GENERAL DESCRIPTION**

The DAS 1128 is a complete self-contained miniature high speed data acquisition system. The compact  $3'' \ge 4.6'' \ge 0.375''$ module provides the designer with an easily implemented solution to the data acquisition problem. It contains an analog input signal multiplexer, a sample-and-hold amplifier, a 12-bit A/D converter, and all of the programming, timing and control circuitry needed to perform the complete data acquisition function. The DAS1128 is a high performance device which can digitize an analog signal to an accuracy of  $\pm\frac{1}{2}$ LSB out of 12 bits, relative to full scale. It has  $\pm 8$ ppm/°C gain temperature coefficient, and the maximum throughput rate can be varied from 50,000 conversions/second for a 12 bit conversion from different analog input channels, to 200,000 conversions/second for a successive 4-bit conversion made on a single channel.



Figure 1. Functional Block Diagram

### SPECIFICATIONS

ANALOG INPUTS

Number of Inputs to Multiplexer

Input Voltage (Full Scale Range)

Maximum Input Voltage Input Current (per channel) Input Impedance Input Capacitance

Input Fault Current (power off or MUX failure) Direct ADC Input Impedance ACCURACY<sup>1</sup> Resolution Error Relative to F.S. Quantization Error Differential Nonlinearity Error @ 33kHz throughput rate @ 50kHz throughput rate Noise Error -FS to +FS Error Between Successive Channel Transitions

**TEMP. COEFFICIENTS** Gain Offset Differential Nonlinearity SIGNAL DYNAMICS Throughput Rate (12 Bits)

MUX Crosstalk ("OFF" channels to "ON" channel) Differential Amplifier CMRR SHA Acquisition Time to 0.01% SHA Aperture Uncertainty SHA Feedthrough

#### DIGITAL INPUT SIGNALS Compatibility

MUX Address Inputs (8, 4, 2, 1; Pins 19B through 22B)

MUX ENABLE HI (Pin 18T)

MUX ENABLE LO (Pin 17B)

STROBE (Pin 24T or 25T)

LOAD ENABLE (Pin 24B)

CLEAR ENABLE (Pin 25B)

TRIGGER (Pin 26T)

TRIGGER (Pin 27T)

(typical @ +25°C and ±15V unless otherwise noted) 16 Single Ended, 8 True-Differential, 16 Pseudo-Differential -10V to +10V, 0V to +10V, -5V to +5V, 0V to +5V, -10.24V to +10.24V, 0V to +10.24V, -5.12V to +5.12V, or 0V to +5.12V. ±15V 5nA max >10<sup>10</sup> ohms 10pF for "OFF" channel 100pF for "ON" channel

Internally limited to 20mA  $10k\Omega$  for each input line

12 Bits ±½LSB ±½LSB

±1/2LSB, 1LSB max ±1LSB ±%LSB

±1LSB

8ppm/°C, 20ppm/°C max 5ppm/°C, 15ppm/°C max 2.5ppm/°C, 6ppm/°C max

50kHz (max) (includes 5µs for MUX and SHA settling time plus 15µs for ADC)

>80dB down @ 1kHz 70dB to 1kHz 4.5µs max 10ns 70dB down @ 1kHz

Standard DTL/TTL logic levels, 1 unit load/line Positive true natural binary coding selects channel for random addressing mode. Must be stable for 100ns after STROBE. High (Logic "1") input enables MUX "HI" output (for inputs 0 through 7) High (Logic "1") input enables MUX "LO" output (for inputs 8 through 15) Negative going transition (Logic "1"

to Logic "0") updates MUX address register. STROBE 1 must be a Logic "1" to enable STROBE 2. STROBE 2 must be at Logic "1" to enable STROBE 1. High (Logic "1") input allows next

STROBE command to sequentially advance MUX address register. Low (Logic "0") input allows next STROBE command to update MUX address register according to external address inputs. Low (Logic "0") input allows next STROBE command to reset MUX address to channel "0" overriding LOAD ENABLE. Positive going transition (Logic "0" to Logic "1") initiates A/D conversion (even during conversion);

TRIGGER (Pin 27T) must be at Logic "0" to allow TRIGGER function. Negative going transition (Logic "1" to Logic "0") initiates A/D conversion; Pin 26T (TRIGGER) must be at Logic "1" to allow TRIGGER

#### DIGITAL OUTPUT SIGNALS Compatibility

Parallel Outputs Coding

MUX Address Outputs (8, 8, 4, 2, 1; pins 18B, 19T through 22T) DELAY OUT (Pin 23T)

#### EOC (Pin 27B)

ADJUSTMENTS & TRIMS Offset Adjust Internal Adjustment (Externally Accessible) Remote External Adjustment (Pin 16T) Range Adjust Internal Adjustment (Externally Accessible) Remote External Adjustment (Pin 16B) Clock Trim (Pin 26B) Factory Setting (Pin 26B "OPEN") External Adjustment Range Delay Trim (Pin 23B) Factory Setting (Pin 23B "OPEN") External Adjustment Range

#### CONTROLS SHORT CYCLE (Pin 28T)

Channel Selection Mode (MUX Address Loading Mode)

A-D Conversion/Channel-Select Sequences

Range Select (Pin 12T)

#### **BINARY SCALE (Pin 15B)**

**OUTPUT CODING (Pin 17T)** 

POWER REQUIREMENTS +15V ±3% -15V ±3% +5V ±5% Power Supply Sensitivity<sup>2</sup>: Gain Offset Ref

**ENVIRONMENT & PHYSICAL Operating Temperature** Storage Temperature **Relative Humidity Electrical Shielding** 

Packaging

Standard DTL/TTL logic levels; 5 unit loads/line. BI, B1 through B12 Natural binary, two's complement, offset binary, or one's complement. Pin selectable. Positive true natural binary coding indicates channel selected.

Negative going transition (Logic "1" to Logic "0") occurring normally  $5\mu s$  (adjustable from 3.0 $\mu s$  to 20µs) after STROBE command initiates A/D conversion automatically when connected to the TRIGGER. High (Logic "1") output during A/D conversion.

±10LSBs (min)

±10LSBs (min)

±10LSBs (min)

±10LSBs (min)

1.25µs/Bit 1.25µs/Bit to 2.08µs/Bit

3.0µs 3.0µs to 20µs

Connect to ground for full 12 bit resolution. Connect to Bn output for resolution to B<sub>n-1</sub> bits. Random, sequential continuous, and sequential triggered. Pin selectable.

Normal (input channel remains selected during its A/D conversion) and overlap (next channel selected during A/D conversion). Pin selectable

Differential Amplifier gain control: connect to ANA RTN (Pin 2T) for X1 gain; connect to AMP OUT (Pin 13B) for X2 gain. This control is used in FSR selection procedure. Connect to REF ADJ (Pin 16B) to set reference to 10.24V. This control is used in FSR selection procedure, see Table II. Ground for 1's complement output code; connect to -15V dc for other available codes.

40mA, 50mA max 70mA, 100mA max 250mA, 500mA max

±2.0mV/V ±4.0mV/V ±0.5mV/V

0 to +70°C -25°C to +85°C Up to 95% noncondensing RFI & EMI 6 sides (except connector area) Insulated steel cased module 3.00" x 4.60" x 0.375

NOTES

Warm-Up time to rated accuracy is 5 minutes

<sup>2</sup>Specification applies only when tracking +15V and -15V supplies are used, and for slowly occuring variations in power supply voltages.

function.

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Specifications subject to change without notice.

### Applying the DAS1128

#### THEORY OF OPERATION

A block diagram of the DAS1128 is shown in Figure 1. Analog input signals are applied to the various inputs of the 16 channel CMOS multiplexer. This multiplexer in conjunction with the differential amplifier that follows it, can be configured by the user to accept 16 single ended analog inputs, or 8 fully differential analog inputs. It can also be connected as a 16 channel "pseudo-differential" input device, which permits some of the benefits of differential operation while maintaining a 16 channel input capability.

The differential buffer amplifier is gain programmable by the user via jumpers at the module pins. This feature, along with the selectable reference voltages, permits the user to set up the DAS1128 to operate on any of 8 input voltage ranges. The differential amplifier drives a sample-and-hold amplifier, whose function it is to hold the selected analog input signal at a constant level while the A/D converter is making a conversion.

The A/D converter is a high speed 12-bit successive approximation device that has been designed using the Analog Devices' AD562, 12-bit integrated circuit D/A. The reference voltage for the conversion is supplied by an adjustable precision reference circuit that has a temperature coefficient of  $5ppm/^{\circ}C$ .

In addition to these basic functional blocks, the DAS1128 also contains all of the clock circuitry necessary to perform the complete data acquisition function. The internal clock can be externally adjusted to provide various throughput rates at different accuracies. Input channel addressing logic is provided, as is the capability to short cycle the A/D converter (i.e. perform conversions of less than 12-bits resolution). It is also possible for the user to adjust the time interval between input channel selection and the commencement of a conversion. The user can thus trade off speed vs. accuracy in the settling time of the multiplexer and sample-and-hold amplifier, as well as speed versus accuracy of the A/D converter.



Figure 2. Simplified Timing Diagram, Showing Time-Interval Assignments and Constants

#### INPUT CONNECTIONS

As shown in Figure 3, three input configurations can be used. 16 single-ended inputs (3a) can be connected to the multiplexer, all referenced to analog gnd. In the second configuration (3b), the inputs are connected individually as 8 true differential pairs. In this case the differential amplifier is connected "Differentially" with the output of the MUX. Finally, a "Pseudo-Differential" connection (3c) can be realized under favorable ground path conditions. In this configuration the differential amplifier Lo terminal is used as the ground return for all sensors. In each of these input schemes, it should be noted that the input multiplexer has been designed to protect itself and signal sources from both overvoltage failure and from fault currents due to power-off loading or MUX failure.



### Figure 3. Signal Input Connections for Three Different Configurations

Full scale range of the DAS1128 may be set by appropriate jumper connections for 8 different ranges: 0 to +10V; 0 to +5V; 0 to +10.24V; 0 to +5.12V; -10 to +10V; -5 to +5V; -10.24 to +10.24V; -5.12 to +5.12V.

Note that 10.24 and 5.12 ranges are commonly used since conversion increments become 5mV/bit, 2.5mV/bit, and 1.25mV/bit.

#### MUX AND S/H DYNAMICS - OVERLAP MODE

The overlap mode is defined as the ability of MUX to accept a new channel address thereby selecting the next channel to be sampled while the previously acquired sample is being held by the S/H for conversion. The dynamic characteristics of the S/H circuit are shown in Figure 4. Maximum throughput rates are obtainable when a single channel is held at a single address and the channel is sampled repeatedly. In a dynamic condition, data-throughput rates obtainable are shown in Figure 5.



Figure 4. Sample-Hold Parameters Defined and Specified

#### DATA ACQUISITION SUBSYSTEMS VOL. II, 15-7

#### SHORT CYCLE

It is possible to short cycle the DAS1128, i.e. stop the conversion after less than 12 bits. This can be done by connecting an external jumper between short cycle terminal and one of the output terminals. With shorter cycles the attainable throughput rate increases, see Figure 5. In short cycle operation the EOC will decrease proportionately to the number of bits selected. Note the short cycle terminal *must* be grounded for full 12-bit operation.



Figure 5. DAS1128 Throughput Rates

#### MUX ADDRESSING

External terminals have been provided for the address counter. Thus the address counter can be configured to produce the following modes: Continuous sequential scanning (free running), sequential scanning with external step command, abbreviated scan continuously, random channel selection. See Figure 6 and set up procedure for details.



Figure 6. To shorten scanning sequence of multiplexer channels, make the appropriate connections, (as shown in the chart) between an external NAND gate and MUX ADDRESS terminals 19T to 21T

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#### **GROUNDING CONSIDERATIONS**

Attention should be given to the methods of connection for electrical returns and voltage reference points. Analog return (ANA RTN) and digital return (DIG RTN) are provided. The following rules should be applied when integrating the DAS1128 into the system.

- If the ±15V power supply is floating (for optimum analog accuracy), connect its return to ANA RTN (Pin 2B or 2T). If the ±15V power supply is *not* floating, connect its return to DIG RTN (Pin 35T or 35B).
- Connect the +5V supply return to DIG RTN (Pin 35T or 35B). If this supply also powers additional equipment, run separate, parallel returns to the equipment ground and to DIG RTN (Pin 35T or 35B).
- To minimize signal grounding problems, single-ended input signals should only be returned to ANA RTN (Pin 2B or 2T). If this is not possible, then connect the input signals in either the "true differential" or "pseudo-differential" configurations (see Figure 3).
- 4. Connect computer ground to DIG RTN (Pin 35T or 35B). Use heavy wire or ground planes.
- 5. The computer chassis should be connected to the computer and power supply grounds at only one point.
- 6. Connect the third-wire ground from main ac power input to the computer power supply return.

#### GAIN AND OFFSET ADJUSTMENTS

The DAS1128 is calibrated with external gain and offset adjustment potentiometers connected as shown in Figure 7 and 8. The offset adjustment potentiometer has an adjustment range of at least  $\pm 10$ LSBs, and the gain range adjustment potentiometer has an adjustment range of at least  $\pm 10$ LSBs.

Offset calibration is not affected by changes in gain calibration, and should therefore be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within ±1/10LSB of the desired value at any point within its range.

These adjustments are not made with zero and full scale input signals, and it may be helpful to understand why. An A/D converter will produce a given digital word output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the converter to be on the verge of switching between two adjacent digital outputs, the unit can be calibrated so that it does switch at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D converters.

#### **OFFSET CALIBRATION**

For unipolar +10V operation set the input voltage precisely to +0.0012V and adjust the offset potentiometer until the converter is just on the verge of switching from 00000000000 to 00000000001.

For  $\pm 5V$  bipolar operation set the input voltage precisely to -4.9988V; for  $\pm 10V$  units set it to -9.9976V. Adjust the offset

potentiometer, Figure 7, until Offset Binary coded units are just on the verge of switching from 000000000000 to 000000000001 and Two's Complement coded units are just on the verge of switching 10000000000 to 10000000001.



Figure 7. Ext. Offset Adjustment

#### GAIN CALIBRATION

Set the input voltage precisely to +9.9963V for unipolar operation, +4.9963V for inputs of  $\pm 5V$  or +9.9926V for inputs of  $\pm 10V$ . Note that these values are 1%LSBs less than nominal full scale. Adjust the 20k variable gain resistor, Figure 8, until Binary and Offset Binary coded units are just on the verge of switching from 111111111110 to 111111111111 and Two's Complement coded units are just on the verge of switching from 011111111110 to 011111111111.



Figure 8. Ext. Ref. Adjustment

#### CLOCK RATE ADJUSTMENT

The clock rate may be adjusted for best conversion time/accuracy trade-off. The conversion time is varied by means of the external circuitry shown in Figure 9. An open CLK TRIM terminal (Pin 26B) results in  $1.25\mu$ s/bit nominal conversion time. A grounded CLK TRIM terminal (for highest accuracy) results in  $2.08\mu$ s/bit conversion.



Figure 9. Clock Trim

#### DELAY TIME ADJUSTMENT

The DLY OUT signal may be adjusted to vary the A/D converter triggering time by means of the external circuitry shown in Figure 10. An open DLY TRIM terminal (Pin 23B) results in a nominal delay time of  $3.0\mu$ s. A grounded DLY TRIM terminal (for highest-accuracy) results in  $20\mu$ s delay time nominal.



Figure 10. Delay Trim

INPUT CONFIGURATION	ANALOG INPUT CONNECTIONS	ANALOG INPUT RETURN	JUMPER CONNECTIONS	
16 Single-Ended Inputs (Figure 3a)	3T thru 10T and 3B thru 10B	All input returns to 2B or 2T	11B to 11T 12B to 2B or 2T 17B to 19T 18T to 18B	
8 Differential Inputs (Figure 3b)	3T thru 10T	3B thru 10B	11B to 12B 17B to 18T to "1"	
16 Pseudo-Differ- ential Inputs (Figure 3c)	3T thru 10T and 3B thru 10B	Common Input return to 12B	11B to 11T 17B to 19T 18T to 18B	

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#### **RECOMMENDED SET-UP PROCEDURE**

1. Select input configuration, see Table I.

2. Select MUX address mode. The method of addressing the multiplexer can be selected by connecting the unit as follows:

<u>RANDOM</u>. Set Pin 24B (<u>LOAD ENB</u>) to Logic "0". The next falling edge of <u>STROBE</u> will load the address presented to Pins 19B through 22B (8, 4, 2, 1). The code on these lines must be stable during the falling edge of <u>STROBE</u> plus 100ns.

SEQUENTIAL FREE RUNNING. Set to Logic "1", Pin 24B (LOAD ENB) and 25B (CLR ENB). Connect Pin 27B (EOC) to Pin 24T (STROBE 1). Connect Pin 23T (DLY OUT) to Pin 27T (TRIG). Use Pin 26T (TRIG) as a run/ stop control (i.e., A/D conversion will continue while TRIG is high and will stop while TRIG is low).

SEQUENTIAL TRIGGERED. Set to Logic "1", Pins 24B (LOAD ENB) and 25B (CLR ENB). Connect Pin 24T (STROBE) to external triggering source. The multiplexer address register will automatically advance by one channel whenever a STROBE command is received. The initial channel can be selected by setting Pin 24B (LOAD ENB) to Logic "0" during only one STROBE command. The multiplexer address will then be determined by the logic levels on Pins 19B through 22B (the external MUX address lines). Channel "0" can be selected as the initial channel by setting Pin 25B (CLR ENB) to Logic "0" during only one STROBE command. The final channel can be selected by following the procedure presented in Figure 6.

- 3. Select A-D conversion/channel select sequence (see Figure 5).
  - NORMAL (input channel remains selected during its A/D conversion). Connect Pin 23T (DLY OUT) to Pin 27T (TRIG).
  - (2) OVERLAP (next channel is selected during A/D conversion). Connect Pin 27B (EOC) to TTL compatible inverter input. Connect inverter output to Pin 24T (STROBE). Connect Pin 23T (DLY OUT) to Pin 27T (TRIG). Adjust the delay to at least 4μs greater than EOC, 20μs max (see Figure 10). The signal on Pin 26T (TRIG) serves as RUN/STOP control.
  - (3) REPETITIVE SINGLE CHANNEL. After selecting the input channel to be repetitively sampled (see MUX ADDRESS MODE, above), set Pin 27T (TRIG) to Logic "0". Connect Pin 26T (TRIG) to a triggering source. Conversion process is initiated by positive edge of TRIG command.

- 4. Select output resolution.
  - a. Full 12-bit resolution: connect Pin 28T (SHORT CYCLE) to Pin 35B (DIG RTN).
  - b. Bn (Bn < 12) bit resolution: connect Pin 28T to the output pin for Bn + 1.
- Select optimum throughput rate. The system clock frequency and the STROBE to TRIG delay (if used) can be trimmed to optimize the accuracy/ throughput rate trade-off. See Figures 9 and 10.
- 6. Select input voltage full scale range. See Table II.
- 7. Select output digital coding. See Table III.

	TABLE II
FOR FULL SCALE RANGE OF:	MAKE THE FOLLOWING CONNECTIONS
0 to +10V	12T to 2T; 14T to 14B to ADC Source*.
0 to +10.24V	same as 0 to +10V, <i>plus</i> 15B to 16B.
0 to +5V	12T to 13B; 14T and 14B to ADC Source*
0 to +5.12V	same as 0 to +5V, plus 15B to 16B.
-10V to +10V	12T to 2T; 14T to 15T; and 14B to ADC Source*.
-10.24V to +10.24V	same as -10V to +10V, <i>plus</i> 15B to 16B.
-5V to +5V	12T to 13B; 14T to 15T and 14B to ADC Source*.
-5.12V to +5.12V	same as -5V to +5V, <i>plus</i> 15B to 16B.

•ADC Source is usually Sample and Hold Output (13T), but may be any signal source including Diff. Amp. Output (13B) if Sample and Hold is not desired.

TABLE III

IABLE III		
OUTPUT CODE	CONNECTIONS	
Unipolar Binary	Connect 17T to -15V Use 29T (B1) for MSB	
2's Complement	Connect 17T to -15V Use 28B (B1) for MSB	
Offset Binary	Connect 17T to -15V Use 29T (B1) for MSB	
1's Complement	Connect 17T to 2B Use 28B (B1) for MSB	

### **Timing Diagrams**



Figure 11. Timing for Non-Overlap Operation in Both Random and Sequential Addressing Modes. For Status Keys and Signal Condition Data, Refer to Box Below.



Figure 12. Timing Diagram for Overlap Operation in the Sequential Addressing Mode. For Status Keys and Signal Condition Data, See Box at Right.

#### SIGNAL CONDITIONS AND STATUS KEYS FOR FIGURES 11 AND 12.

CH. 2 = -3.415V CODE 010 101 010 101 CH. 3 = +10.235V CODE 111 111 111 111 CH. 0 = -10.240V CODE 000 000 000 CH. 1 = +3.410V CODE 101 010 101 010

> ADC SET UP FOR ±10.24V. INPUT, OFFSET BINARY. (FOR TWO'S COMPLEMENT, USE BI FOR MSB.)

KEY	INPUTS	OUTPUTS
$\overline{XX}$	May change	Don't know
ZZZ	May change 0 to 1	Changes 0 to 1
Ш	May change 1 to 0	Changes 1 to 0
<u>OR</u>	Must be stable	Will be stable

#### DATA ACQUISITION SUBSYSTEMS VOL. II, 15-11

### **Outline Drawings and Pin Designations**

#### **DAS1128 CONNECTOR PIN DIAGRAM**

+15V	1T	1B	-15V
ANA RTN	2T	28	ANA RTN
CH 0 IN	31	3B	CH 8 IN (CHORTN)
CH 1 IN	4T	4B	CH 9 IN (CH 1 RTN)
CH 2 IN	51	5B	CH 10 IN (CH 2 RTN)
CH 3 IN	6T	6B	CH 11 IN (CH 3 RTN)
CH 4 IN	7T	7B	CH 12 IN (CH 4 RTN)
CH 5 IN	8T	8B	CH 13 IN (CH 5 RTN)
CH 6 IN	9T	9B	CH 14 IN (CH 6 RTN)
CH 7 IN	10T	10B	CH 15 IN (CH 7 RTN)
MUX HI OUT	11T	11B	MUX LO OUT
RANGE SEL	12T	12B	AMP IN LO
S& HOUT	13T	13B	AMP OUT
ADC IN 1	14 T	14B	ADC IN 2
+10V REF	15T	15B	BINARY SCALE
EXT OFFSET	16T	16B	REF ADJ
OUTPUT CODING	17T	17B	ENABLE LO
ENABLE HI	18T	18B	8 OUT
8 OUT   MUX	19T	19B	8 IN ) MUX
4 OUT ADDRESS	20T	20B	4 IN   ADDRESS
2 OUT LINES	21T	21B	2 IN LINES
10UT	22T	22B	1 IN 1
DLY OUT	23T	23B	DLY TRIM
STROBE 1	24T	24B	LOAD ENB
STROBE 2	25T	25B	CLR ENB
TRIG	26T	26B	CLK TRIM
TRIG	27T	27B	EOC
SHORT CYCLE	28T	28B	BTOUT
· B1 OUT	29T	29B	B2 OUT
B3 OUT	30T	30B	B4 OUT
B5 OUT	31T	31B	B6 OUT
B7 OUT	32T	32B	B8 OUT
B9 OUT	33T	33B	B10 OUT
B11 OUT	34T	34B	B12 LSB OUT
DIG RTN	35T	35B	DIG RTN
+5V	36T	36B	+5V

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



#### P. C. BOARD LAYOUT



### **Typical Applications**

#### DAS1128 WITH MOTOROLA 6800



6. 8255 SHOWN, HOWEVER 6820 CAN ALSO BE USED

DAS1128 WITH INTEL 8080



1. 2255 USED IN MODE 1 (STROBED I/O) 2. CS TO A; (WHERE, A; IS AN ADDRESS BIT OTHER THAN A<sub>0</sub> OR A<sub>1</sub>) 3. PC6 INDEXES MUX TO DESIRED CHANNEL 4. PC7 INITIATES CONVERSION 6. EOC STROBES IN DATA AND MUX INFO

# 

## 14-Bit & 15-Bit Sampling Analog-to-Digital Converter

#### FEATURES

Complete with High Accuracy Sample/Hold and A/D Converter

Differential Nonlinearity: ±0.002% FSR max (DAS1153)

Nonlinearity: DAS1152: ±0.005% FSR max DAS1153: ±0.003% FSR max Low Differential Nonlinearity T.C.: ±2ppm/°C max High Throughput Rate: 25kHz min (DAS1152) High Feedthrough Rejection: -96dB Byte-Selectable Tri-State Buffered Outputs Internal Gain & Offset Potentiometers Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules

#### APPLICATIONS

Process Control Data Acquisition Automated Test Equipment Seismic Data Acquisition Nuclear Instrumentation Medical Instrumentation Robotics

#### **GENERAL DESCRIPTION**

The DAS1152/DAS1153 are 14-/15-bit sampling analog-to-digital converters having a maximum throughput rate of 25kHz/20kHz. They provide high accuracy, high stability, and functional completeness all in a  $2^{"} \times 4^{"} \times 0.44^{"}$  metal case.

Guaranteed high accuracy system performance such as nonlinearity of  $\pm 0.005\%$  FSR (DAS1152)/ $\pm 0.003\%$  FSR (DAS1153) and differential nonlinearity of  $\pm 0.003\%$  FSR (DAS1152)/ $\pm 0.002\%$ FSR (DAS1153) are provided. Guaranteed stability such as differential nonlinearity T.C. of  $\pm 2ppm/^{\circ}C$  (DAS1153) maximum, zero T.C. of  $\pm 80\mu V/^{\circ}C$  maximum, gain T. C. of  $\pm 8ppm/^{\circ}C$ maximum and power supply sensitivity of  $\pm 0.001\%$  FSR/% V<sub>S</sub> are also provided by the DAS1152/DAS1153.

The DAS1152/DAS1153 make extensive use of both integrated circuit and thin film components to obtain their excellent performance, small size, and low cost. The devices contain a precision sample/hold amplifier, high accuracy 14-/15-bit analog-to-digital converter, tri-state output buffers, internal gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

### DAS1152/DAS1153





#### Figure 1. DAS1152/DAS1153 Block Diagram

Four analog input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V,  $\pm5V$ , and  $\pm10V$ . Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement. Tri-state buffers provide easy interface to bus structured applications.

### **SPECIFICATIONS**

(typical @  $+25^{\circ}$ C unless otherwise specified)

MODEL	DAS1152	DAS1153
RESOLUTION	14 Bits	15 Bits
DYNAMIC PERFORMANCE	1	
Throughput Rate	25kHzmin	20kHz min
Conversion Time	35µs max	44µs max
S/H Acquisition Time	4µs max	5µs max
S/H Aperture Delay	50ns	* .
S/H Aperture Uncertainty	Ins	*
Feedthrough Rejection	-96dB	*
Droop Rate Dislostric Absorption E-roz	$0.05\mu V/\mu s(0.1\mu V/\mu s max)$	*
Dielectric Absorption Error	± 0.005% of input voltage Change	
ACCURACY	+ 0.005% ECB3	+ 0.0030/ ESB3-man
Differential Nonlinearity	+ 0.003% FSR max	± 0.003% FSR max
No Missing Codes	Guaranteed	*
$+ 3\sigma$ Noise (S/H plus A/D)	75uV rms	*
$\pm 3\sigma$ Noise (A/D)	50µV rms	*
STABILITY		
Differential Nonlinearity T C	+ 2ppm/°C max	*
Gain T.C.	+ 8ppm/°C max	*
Zero T.C.	$\pm 30\mu V/^{\circ}C typ, \pm 80\mu V/^{\circ}C max$	*
Power Supply Sensitivity	± 0.001% FSR <sup>3</sup> /% V	* 1
ANALOGINPUT		
Voltage Range		
Bipolar	$\pm 5V, \pm 10V$	*
Unipolar	0 to + 5V, 0 to + 10V	*
ADC Input Impedance 0 to + 5V	2.5kΩ	*
$0 \text{ to } + 10 \text{V}, \pm 5 \text{V}$	5kΩ	*
± 10V	10.0kΩ	*
S/H Input Impedance	100MΩ 5pF	*
DIGITALINPUTS		
Convert Command <sup>4</sup>	1TTL Load, Positive Pulse	*
	Negative Edge Triggered	* .
S/H Control	HOLD = Logic 0	*
Low Enable High Enable	SAMPLE = Logic 1 ENABLE = Logic 0	* .
DIGITAL OUTDUTS	LIAMBLE - Logic 0	
DIGITAL OUTPUTS		
Lunipolar	Binam	*
Bipolar	Offset Binary 2's Complement	*
Output Drive	2TTL Loads	*
Status	Logic "1" During Conversion	*
Output Drive	2TTL Loads	*
INTERNAL REFERENCE VOLTAGE	$+10V, \pm 0.3\%$	*
External Load Current (Rated Performance)	2mA max	*
Temperature Stability	± 5ppm/°C max	*
POWER REQUIREMENTS		
Rated Voltages	$\pm 15V(\pm 3\%), \pm 5V(\pm 5\%)$	*
Operating Voltages <sup>5</sup>	$\pm 12V$ to $\pm 17V$ , $\pm 4.75V$ to $\pm 5.25V$	*
Supply Current Drain ± 15V	± 37mA	*
+ 5V	80mA	*
TEMPERATURERANGE		
Specified	0 to + 70°C	*
Operating	-25°C to +85°C	*
Storage .	-25"Cto +85"C	-
Shielding	meets MIL-SID-202E, Method 103B	•
Suciang	Electromagnetic (EMI) 5 Sides	*
0175	2 A A A A A A A A A A A A A A A A A A A	•
SIZE	2" × 4" × 0.44" Metal Package	*

**OUTLINE DIMENSIONS** 

Dimensions shown in inches and (mm).



NOTES

\*Specifications same as DA\$1152

<sup>1</sup>Measured in hold mode, input 20V pk-pk @ 10kHz. <sup>2</sup>Worst-case summation of S/H and A/D nonlinearity errors.

<sup>3</sup>FSR means Full Scale Range.

\*When connecting the Convert Command and the S/H control terminals together, the pulse width must be long enough for the S/H

When connecting the Convert Command and the S/H control terminals together, the pulse width must be long enough for the S/H is applifier to acquire the input signal to the required accuracy 4 µs (max, DAS1152)/5 µs (max, DAS1153). If the A/D converter is only used, the Convert Command pulse width should be 100ns min (see Figure 2). <sup>1</sup>If only the ADC portion is used, the operating power supply voltage can be maintained at  $\pm 12V$  to  $\pm 17V$ . But if the S/H section is required, the operating voltage must be maintained at  $\pm 15V (\pm 3\%)$  or the S/H input voltage must be limited to -7V<sup>1</sup>Converse of the Power Supply voltage.

\*Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

### Applying the DAS1152/DAS1153

#### **OPERATION**

The DAS1152/DAS1153 are functionally complete data acquisition subsystems being fully characterized as such. All the necessary data acquisition and microprocessor interface elements are provided internal to these devices. Accuracy and performance criteria are tested and specified for the entire system. Thus, design time and associated high accuracy problems are minimized because layout and component optimization have already been performed.

For operation, the only connections necessary to the DAS1152/ DAS1153 are the  $\pm$ 15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tristate controls. Analog input and digital output programming are user selectable via external jumper connections.

#### ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table I. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V <sub>IN</sub> or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to + 5V	ANA IN 1,		
	ANA IN 2,	Ground	NC*
	ANA IN 3		
0 to + 10V	ANA IN 2	Ground	NC*
	ANA IN 3	ANA IN 1	
±5V	ANA IN 1	Ground.	ANA IN 2
		ANA IN 3	
$\pm 10V$	ANA IN 3	Ground,	ANA IN 2
	· .	ANA IN 1	

\*No Connection

Table I. Analog Input Pin Programming

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.



Figure 2. Analog Input Block Diagram

#### TIMING DIAGRAM

The timing diagram for the DAS1152/DAS1153 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of  $4\mu$ s (DAS1152)/ $5\mu$ s (DAS1153) to insure accuracy is attained. If the sample/hold amplifier is not used, the trigger pulse needs to be only 100ns (min) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking  $35\mu s/$  $44\mu s$  maximum for the DAS1152/DAS1153 respectively. At this time, the STATUS line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tristate buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.



#### DATA ACQUISITION SUBSYSTEMS VOL. II, 15-15

#### GAIN AND OFFSET ADJUSTMENT

The DAS1152/DAS1153 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within  $\pm 1/10LSB$  of the desired value at any point within its range.

#### OFFSET CALIBRATION

For a 0 to +10V unipolar range set the input voltage precisely to +305 $\mu$ V for the DAS1152 and +153 $\mu$ V for the DAS1153. For a 0 to +5V unipolar range set the input to +153 $\mu$ V for the DAS1152 and +76 $\mu$ V for the DAS1153. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000......000 to 000......001.

For the  $\pm 5V$  bipolar range set the input voltage precisely to + 305µV for the DAS1152 and + 153µV for the DAS1153. For a  $\pm 10V$  bipolar range set the input voltage precisely to + 610µV for the DAS1152 and + 305µV for the DAS1153. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000......001 to 000......001 and the two's complement coded units are just on the verge of switching from 100......000 to 100......001.

#### GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1152)/ +9.99954V (DAS1153) for the 0 to +10V units, +4.99954V (DAS1152)/+4.99977V (DAS1153) for 0 to +5V units, +9.99817V (DAS1152)/+9.99909V (DAS1153) for  $\pm 10V$  units, or +4.99909V (DAS1152)/+4.99954V (DAS1153) for  $\pm 5V$  units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

#### DAS1152/DAS1153 INPUT/OUTPUT RELATIONSHIPS

The DAS1152/DAS1153 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ( $\overline{\text{MSB}}$ ) is used to obtain two's complement coding. Table II shows the DAS1152/DAS1153 unipolar analog input/digital output relationships. Tables III and IV show the DAS1152/DAS1153 bipolar analog input/digital output relationships.

#### NOMINAL BIPOLAR INPUT-OUTPUT RELATIONSHIPS

0 to +5V Ran	ige	0 to + 10V R	ange
DAS1152	DAS1153	DAS1152	DAS1153
+ 4.99969V	+4.99984V	+ 9.99939V	+ 9.99969V
+ 2.50000V	+2.50000V	+ 5.0000V	+ 5.00000V
+0.62500V	+0.62500V	+1.25000V	+1.25000V
+0.0003V	+0.00015V	+0.0006V	+0.0003V
+ 0.0000V	+0.0000V	+0.0000V	+0.0000V

#### DIGITAL OUTPUT Binary Code DAS1152 DAS1153

111 111 111 111 111
100 000 000 000 000
001 000 000 000 000
000 000 000 000 001
000 000 000 000 000

#### Table II. Unipolar Input/Output Relationships

1				
Analog Input		Digital Output		
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code	
+ 4.99939V	+ 9.99878V	11 111 111 111 111	01 111 111 111 111	
+ 2.50000V	+ 5.0000V	11 000 000 000 000	01 000 000 000 000	
+0.00061V	+0.00122V	10 000 000 000 001	00 000 000 000 001	
+ 0.00000V	+0.00000V	10 000 000 000 000	00 000 000 000 000	
- 5.00000V	- 10.00000V	00 000 000 000 000	10 000 000 000 000	

#### Table III. DAS1152 Bipolar Input/Output Relationships

Analog Input		Digital Output		
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code	
+ 4.99969V	+9.99939V	111 111 111 111 111	011 111 111 111 111	
+ 2.50000V	+ 5.0000V	110 000 000 000 000	010 000 000 000 000	
+0.0003V	+0.00061V	100 000 000 000 001	000 000 000 000 001	
+0.00000V	+0.00000V	100 000 000 000 000	000 000 000 000 000	
- 5.00000V	- 10.00000V	000 000 000 000 000	100 000 000 000 000	

Table IV. DAS1153 Bipolar Input/Output Relationships

#### TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

#### POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1152/DAS1153, care must still be taken to provide proper grounding due to the high accuracy nature of these devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1152/DAS1153 terminals.

No power supply decoupling is required since, the DAS1152/ DAS1153, contain high quality tantalum capacitors on each of the power supply inputs to ground.



## 14-Bit & 15-Bit Low Level Data Acquisition Systems

#### FEATURES

**Functionally Complete:** 

Includes Instrumentation Amplifier, Sample/Hold Amplifier, and Analog to Digital Converter Differential Nonlinearity: ±0.002% FSR max (DAS1156) Guaranteed Nonlinearity: ±0.005% FSR (DAS1155) ±0.003% FSR (DAS1156) High Common Mode Rejection: -80dB (up to 500Hz) High Feedthrough Rejection: -96dB

Resistor Programmable Gain: 1V/V to 1000V/V Byte Selectable Tri-State Buffer Outputs Internal Gain and Offset Potentiometers

#### APPLICATIONS

Low Level High Accuracy Data Acquisition Systems Process Control Nuclear Instrumentation Automated Test Equipment Medical Instrumentation

#### **GENERAL DESCRIPTION**

The DAS1155/DAS1156 are 14-/15-bit low level data acquisition systems having a minimum throughput rate of 25kHz/20kHz. These data acquisition systems provide high accuracy, high stability, and functional completeness all in a  $2'' \times 4'' \times 0.44''$  metal case.

Guaranteed high accuracy system performance such as nonlinearity of  $\pm 0.005\%$  FSR (DAS1155)/ $\pm 0.003\%$  FSR (DAS1156) and differential nonlinearity of  $\pm 0.003\%$  FSR (DAS1155)/ $\pm 0.002\%$ FSR (DAS1156) are provided. Guaranteed stability such as differential nonlinearity T.C. of  $\pm 2ppm/^{\circ}C$  maximum, offset T.C. of  $\pm (1 + 50/G) \mu V/^{\circ}C$  (RTI) and gain T.C. (RTI) of  $\pm 16ppm/^{\circ}C$  are also provided by the DAS1155/DAS1156.

Each DAS1155/DAS1156 makes extensive use of both integrated circuit and thin-film components to obtain its excellent perfor-



Figure 1. DAS1155/DAS1156 Block Diagram

## DAS1155/DAS1156



mance and small size. Incorporated in these devices are a gain programmable instrumentation amplifier, precision sample/hold amplifier, high accuracy 14-/15-bit analog to digital converter, tri-state output buffers, gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

Unipolar coding is provided for true binary format with bipolar coding displayed in offset binary or two's complement. Tri-state buffers are available for easy interface to bus structured applications.

#### **OPERATION**

The DAS1155/DAS1156 are designed, built, and tested to meet system data acquisition requirements. These units can significantly reduce design and debug time by providing, in one package, all of the circuitry necessary for low level data acquisition and microprocessor bus interface.

For operation, the only connections necessary to the DAS1155/ DAS1156 are the  $\pm$  15V and + 5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Digital output programming is user selectable via external jumper connections.

#### ANALOG INPUT SECTION

The analog input section consists of a true differential instrumentation amplifier used to obtain high accuracy measurements in the presence of noise (as shown in Figure 2). It also provides input impedance of (100M $\Omega$ ) and high common mode rejection of (-80dB). User selectable gain of 1V/V to 1000V/V via an external resistor enables either low level or high level full scale ranges to be applied to the input (+10mV to +10V unipolar,  $\pm5mV$  to  $\pm5V$  bipolar) with gain determined by the following formula:

$$\text{GAIN} = 1 + \left(\frac{20k}{R_G}\right)$$

### 15

### **SPECIFICATIONS**

MODELDASI153DASI151PRODUCL14 Bits15 BitsDYNAMIC CHARACTERISTICS35 µs max44 µs maxADC Conversion Time35 µs max44 µs max1000038 FSR @ G = 1015 µs max1000038 FSR1000038 FSR @ G = 1025 µs max1000038 FSRAcquisition Time4 µs max5 µs maxAcquisition Time4 µs max5 µs maxAperture Uncertainty Time1 as1Peoro Rate0.05 µV µs10.003% max100028 FSR @ G = 100.003% max10.003% max100028 FSR @ G = 1000380.003% max10.003% max100028 FSR @ G = 1000380.003% max10.003% maxApertur Uncentrainty Time1 as1100028 FSR @ G = 0.05 µV µs0.003% max10.003% max100028 FSR @ G = 0.05 µV µs0.003% max10.003% max100028 FSR @ G = 0.05 µV µs0.003% max10.003% max100138 FSR @ G = 0.05 µV µs0.003% max10.003% max100140 FSR @ G = 0.05 µV µs0.003% max10.003% max100158 CoreAdjustable to Zero41016 minital Nonlinearity T.C. $2 (pm^2 C max)$ 1016 minital Nonlinearity T.C. $2 (pm^2 C max)$ 1016 minital Nonlinearity T.C. $2 (pm^2 C max)$ 1016 minital Nonlinearity T.C. $2 (pm^2 C max)$ 1017 Lingt Lingt Amage $100100$	wopst	DAGUE	DAGUIG
RESOLUTION14 Bits15 BitsDYNAMIC CHARACTERISTICS ADC Conversion Time $35\mu s max$ $44\mu s max$ 1A Setting Time, (100 Output Swing) to 0.003% FSR @ G = 1 $15\mu s max$ •to 0.003% FSR @ G = 10 $15\mu s max$ •to 0.003% FSR @ G = 10 $25kH z min$ $20kH z min$ SAMPLE HOLD Acquisition Time $4\mu s max$ $5\mu s max$ Aperature Delay Time $9608$ •Aperature Delay Time $-9648$ •Drough Rejection 1 $-9648$ •Drough Rejection 1 $-9648$ •CCURACYDifferential Nonlinearity (FSR) <sup>2</sup> $\pm 0.003\% max$ $\pm 0.003\% max$ Differential Nonlinearity (FSR) <sup>2</sup> $\pm 0.003\% max$ $\pm 0.003\% max$ $\pm 0.003\% max$ Integral Nonlinearity (FSR) <sup>3</sup> $\pm 0.003\% max$ $\pm 0.003\% max$ $\pm 0.003\% max$ No Missing CodesGuaranteed••Offset (RTI) T. C. $\pm (1 + \frac{50}{2}) \mu VrC$ •Gain ErrorAdjustable to Zero•STABILITY $0.015\% FSR ?\% V_S$ •Voltage Input Range (ADC FSR) $\pm 10m V to + 10V (Unipolar)$ •Joffset RTI) T. C. $\pm 16ppm ^{C} max$ •Gain RangeI to 1000••Gain Guartend AmbliferZnA•Gain Guartend AmbliferI to 1000•Ga	MODEL	DASIISS	DASIIS
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$\begin{aligned} & \text{Instrume transmission} \\ & \text{10} 0.003 \text{k} FSR (@ G = 10 \\ & \text{15} \text{Js} \text{smax} \\ & \text{10} 0.003 \text{k} FSR (@ G = 10 \\ & \text{10} 0.003 \text{k} FSR (@ G =$	ADC Conversion 1 ime IA Settling Time (10V Output Swing)	35µs max	44µs max
io 0.003% FSR @ G = 10015µs max*to 0.01% FSR @ G = 1.0025kHz min20kHz minSAMPLE HOLD4µs max5µs maxAcquisition Time4µs max5µs maxAperture Delay Time1ns*Aperture Uncertainty Time1ns*Droop Rate0.05µV/µs*ACCURACYDifferential Nonlinearity (FSR) <sup>2</sup> $\pm 0.003\%$ max $\pm 0.002\%$ maxIntegral Nonlinearity (FSR) <sup>2</sup> $\pm 0.003\%$ max $\pm 0.003\%$ max $\pm 0.003\%$ maxIntegral Nonlinearity (FSR) <sup>2</sup> $\pm 0.003\%$ max $\pm 0.003\%$ max $\pm 0.003\%$ maxNo Missing CodesGuaranteed**Offset ErrorAdjustable to Zero**STABILITYOffset (RTI) T.C. $\pm (1 + \frac{50}{9})$ µV/C*Offset ERT) T.C. $\pm (1 + \frac{50}{9})$ µV/C**Offset (RTI) T.C. $\pm (1 + \frac{50}{9})$ µV/C**Gain ErrorAdjustable to Zero**ANLOG INFUTS $\pm 0.0015\%$ FSR ?% Vs**Notage Input Range (ADC FSR) $\pm 100$ Vo + 10V (Unipolar)**Voltage Input Range (ADC FSR) $\pm 100$ Vo + 10V (Unipolar)**Instrumentation AmplifierGainCain**Gain Range10 1000***Gain Gain Range10 1000***Instrumentation AmplifierSata**Gain Range10 1000***Inguit Inpedance10%1**	to 0.003% FSR @ $G = 1$	15us max	*
to 0.0% FSR @ G = 100S045*SAMPLE HOLDAperature Delay Time445 maxSus maxAperature Delay TimeIns*Feedthrough Rejection 1Peedthrough Rejection 1Peedthrough Rejection 1Differential Nonlinearity (FSR)3±0.003% max±ACCURACYDifferential Nonlinearity (FSR)3±0.003% max±0.002% maxDifferential Nonlinearity (FSR)3±0.003% max±0.003% max±0.003% maxACCURACYDifferential Nonlinearity (FSR)3±0.003% max±0.003% max±0.003% maxNo Missing CodesGuaranteed• <td>to 0.003% FSR @ G = 10</td> <td>15µs max</td> <td>*</td>	to 0.003% FSR @ G = 10	15µs max	*
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SAMPLE HOLD Acquisition Time 4 us max 5 us max Aperature Delay Time 5 on 4 $-96dB$	Throughput Rate @ G = 1, 10	25kHz min	20kHz min
Acquisition Time4 smax5 ps maxAperature Delay TimeIns•Feedthrough Rejection 1-96dB•Droop Rate $0.65 \mu V / \mu s$ •ACCURACYDifferential Nonlinearity (FSR)2 $\pm 0.003\%$ max $\pm 0.002\%$ maxDifferential Nonlinearity (FSR)3 $\pm 0.003\%$ max $\pm 0.003\%$ maxNo Missing ColesGuaranteed•Offset ErrorAdjustable to Zero•Gain ErrorAdjustable to Zero•STABILITY $\pm (1 \pm \frac{50}{G}) \mu V/C$ •Offset (RTI) T.C. $\pm (1 \pm \frac{50}{G}) \mu V/C$ •Differential Nonlinearity T.C. $\pm 2ppm'C$ max•Power Supply Sensitivity $\pm 0.0015\%$ FSR $^{2}\%$ Vs•ANALOG INPUTS $\pm 10mV$ to $\pm 10V$ (Unipolar)•Voltage Input Range ( $\frac{ADC FSR}{Gain}$ $\pm 10mV$ to $\pm 10V$ (Unipolar)•Instrumentation AmplifierGaineGain Range1 to 1000•Gain Range1 to 1000•Input Impedance $10^4\Omega$ •Differential Notifier $\pi A = 0.0000$ Gain Range1 to 1000•Gain Corrent $2nA$ •MC Corvert Command*ITTL Load, Positive PulseNord Corrent RangeIto V•DIGITAL UTTUTS $\pi i Sate$ Parallel Data OutputsTri-StateUnipolar $\pm 15V \pm 5\%$ , $+5V \pm 5\%$ Output Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 10V \pm 0.3\%$ StatusLogic "I" During Conversion <td>SAMPLEHOLD</td> <td></td> <td></td>	SAMPLEHOLD		
Aperture Delay LineJonsAperture Uncertainty TimeInsPeedthrough Rejection 1 $-96dB$ Droop Rate $0.05\mu/V\mu s$ ACCURACY $1.0003\%$ maxDifferential Nonlinearity (FSR)2 $\pm 0.003\%$ maxIntegral Nonlinearity (FSR)3 $\pm 0.003\%$ maxNo Missing CodesGuaranteedOffset ErrorAdjustable to ZeroGain ErrorAdjustable to ZeroSTABILITY $\pm (1 + \frac{50}{G}) \mu V/rC$ Offset Error $\pm 10007\%$ maxCain (RTI) T.C. $\pm (1 + \frac{50}{G}) \mu V/rC$ Differential Nonlinearity T.C. $\pm 2ppm^2C$ maxPower Supply Sensitivity $\pm 0.0015\%$ FSR $^{2}\%$ VsANALOG INPUTS $\pm 10mV$ to $\pm 10V$ (Unipolar)Voltage Input Range (ADC FSR) $\pm 10mV$ to $\pm 5V$ (Bipolar)Instrumentation Amplifier $50nA$ Gain Range $110 1000$ Gain Equation $G = 1 + (\frac{20k\Omega}{R_0})$ Input Impedance $10^3 R_1$ Bias Current $50nA$ Offset Current $2nA$ CMV $\pm 10V$ DIGITAL INPUTSTri-StateValue Iob to S0H2) $-80dB$ CMV $\pm 10V$ DIGITAL OUTPUTSParallel Data OutputsTri-StateUnipolarBinaryBipolarOffset ErrorsionOutput DriveTTI-LoadsINTERNAL REFERENCE VOLTAGE $+10V, \pm 0.3\%$ External Load Current (Rated Performance) $2nA$ (max)Temperature Stability $\pm 40mA$ Temperature Stability $\pm 15V \pm 5\%, +5V \pm 5\%$ <td>Acquisition Time</td> <td>4µs max</td> <td>5µs max</td>	Acquisition Time	4µs max	5µs max
$\begin{tabular}{lllllllllllllllllllllllllllllllllll$	Aperature Delay Time	50ns	
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Integral Nonlinearity (FSR) <sup>3</sup> $\pm 0.005\%$ max $\pm 0.003\%$ maxNo Missing CodesGuaranteed $\star$ Offset ErrorAdjustable to Zero $\star$ Gain ErrorAdjustable to Zero $\star$ STABILITY $\pm (1 + \frac{50}{G}) \mu V/C$ $\star$ Offset (RTI) T.C. $\pm (1 + \frac{50}{G}) \mu V/C$ $\star$ Gain (RTI) T.C. $\pm (1 + \frac{50}{G}) \mu V/C$ $\star$ Differential Nonlinearity T.C. $\pm 2ppm^{n}C$ $\star$ Power Supply Sensitivity $\pm 0.005\%$ FSR <sup>1/N</sup> V <sub>5</sub> $\star$ ANALOG INPUTS $\pm 0.005\%$ FSR <sup>1/N</sup> V <sub>5</sub> $\star$ Voltage Input Range ( $\frac{ADC FSR}{Gain}$ ) $\pm 100W$ to $\pm 10V$ (Unipolar) $\pm$ Instrumentation AmplifierResistor Programmable $\bullet$ Gain Range1 to 1000 $\bullet$ $\bullet$ Gain Equation $G = 1 + (\frac{20k\Omega}{R_0})$ $\bullet$ Input Impedance10 <sup>6</sup> 1 $\bullet$ Bias Current50nA $\bullet$ Offset Current2nA $\bullet$ CMR (up to 500Hz) $-80dB$ $\bullet$ CMR (up to 500Hz) $-80dB$ $\bullet$ DIGITAL UNPUTSTrit. Load, Positive PulseNoccovert Command <sup>4</sup> Trit. Load, SomplementOutput Drive21TL LoadsStatusLogic "1" During ConversionOutput Drive21TL LoadsINTERNAL REFERENCE VOLTAGE $\pm 10V, \pm 0.3\%$ Paralle Data Outputs $\pm 15V \pm 5\%, \pm 5\%$ Optarting thability $\pm 240mA$ POWER REQUIREMENTS $\pm 15V \pm 5\%, \pm 5\%$ Rated Voltages $\pm 15V \pm 5\%, \pm 5\%$ Operating Voltages <sup>5</sup>	Differential Nonlinearity (FSR) <sup>2</sup>	± 0.003% max	± 0.002% max
No Missing CodesGuaranteed•Offset ErrorAdjustable to Zero•Gain ErrorAdjustable to Zero•STABILITY $\pm (1 + \frac{50}{C}) \mu V/C$ •Offset (RTI) T.C. $\pm 16 \text{ppm}^{N} \text{C}$ •Differential Nonlinearity T.C. $\pm 2 \text{ppm}^{N} \text{Cmax}$ •Power Supply Sensitivity $\pm 0.0015\% \text{FR}^{1/6} \text{Vs}$ •ANALOG INPUTS+100V (Unipolar)•Voltage Input Range ( $\underline{ADC FSR}$ ) $\pm 5 \text{mV to } \pm 5V (Bipolar)$ •Instrumentation AmplifierGainResistor Programmable•Gain Range1 to 1000••Gain Equation $G = 1 + (\frac{20k\Omega}{R_0})$ ••Instrumentation AmplifierSonA••Gain Equation $G = 1 + (20k\Omega)$ ••Input Impedance10^{8}\Omega••Offset Current2nA••CMV $\pm 10V$ ••DIGITAL INPUTSTTL Load, Positive Pulse•ADC Convert Command <sup>4</sup> TTL Load, Positive Pulse•Noc Convert Command <sup>4</sup> Tri-State•UnipolarBinary2150 ComplementOutput Drive2TTL Loads•StatusLogic ''I' During ConversionOutput Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 10V, \pm 0.3\%$ External Load Current (Rated Performance)2mA (max)Temperature Stability $\pm 49mA$ + 5V80mATEMPERATURE RANGE5pecified <t< td=""><td>Integral Nonlinearity (FSR)<sup>3</sup></td><td>± 0.005% max</td><td>±0.003% max</td></t<>	Integral Nonlinearity (FSR) <sup>3</sup>	± 0.005% max	±0.003% max
Offset ErrorAdjustable to ZeroGain ErrorAdjustable to ZeroSTABILITY $\pm (1 + \frac{50}{G}) \mu V/^{C} $ Offset (RTI) T. C. $\pm (1 + \frac{50}{G}) \mu V/^{C} $ Differential Nonlinearity T. C. $\pm 2ppm^{P}C$ aPower Supply Sensitivity $\pm 0.0015\% FSR^{2}\% V_{S}$ ANALOG INPUTS $\pm 0.0015\% FSR^{2}\% V_{S}$ Voltage Input Range ( $\frac{ADC FSR}{Gain}$ ) $\pm 10mV to \pm 10V (Unipolar)$ Instrumentation Amplifier $\pm 5mV to \pm 5V (Bipolar)$ Gain RangeI to 1000Gain Equation $G = 1 + (\frac{20kf1}{R_G})$ Input Impedance $10^{6}f1$ Bias Current $5nA$ Offset Current $2nA$ CMV Up to 500Hz) $-80dB$ CMV Up to 500Hz) $-80dB$ CMV Up to 500Hz) $-10V$ Parallel Data OutputsTri-StateUnipolarBinaryBipolarOffset Binary, 2's ComplementOutput Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 10V \pm 0.3\%$ External Load Current (Rated Performance) $\pm 3.5pm^{P}C (max)$ POWER REQUIREMENTS $\pm 15V \pm 5\%, + 5V \pm 5\%$ Rated Voltages $\pm 15V \pm 5\%, + 5V \pm 5\%$ Operating Voltages? $\pm 15V \pm 5\% + 5V \pm 5\%$ Storage $-25'C to + 85'C$ Storage	No Missing Codes	Guaranteed	*
UnderstructAdjustable (J2E0)STABILITY Offset (RTI) T.C. $\pm (1 + \frac{50}{G}) \mu V/^{\circ}C$ Gain (RTI) T.C. $\pm (1 + \frac{50}{G}) \mu V/^{\circ}C$ Differential Nonlinearity T.C. $\pm 2ppm'^{\circ}Cmax$ Power Supply Sensitivity $\pm 0.0015\% FSR'/\% V_S$ ANALOG INPUTS $\pm 10mV to \pm 10V (Unipolar)$ Voltage Input Range ( $\underline{ADC FSR}$ ) $\pm 10mV to \pm 5V (Bipolar)$ Instrumentation Amplifier $\equiv 5mV to \pm 5V (Bipolar)$ Gain Range1 to 1000Gain Range $10000$ Gain Range $10000$ Input Impedance $10^8 \Omega$ Diffset Current $2nA$ CMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*ITTL Load, Positive PulseNDC Convert Command*NTTL Load, Positive PulseNDC Convert Command*BinaryBipolarOffset Eliary, 2's ComplementOutput Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 15V \pm 5\%, \pm 5V \pm 5\%$ Status $Logie'' During Conversion$ Output Drive $2TTL Loads$ INTERNAL REFERENCE VOLTAGE $\pm 15V \pm 5\%, \pm 5V \pm 5\%$ Supply Current (Rated Performance) $2mA (max)$ Temperature Stability $\pm 5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%, \pm 5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%$ Operating Voltages $\pm 25'C = 25'C + 85'C$ Storage $-25'C + 85'C$ Stor	Offset Error	Adjustable to Zero	•
STABLITY Offset (RTI) T. C. $\pm (1 + \frac{50}{G}) \mu V/^{\alpha}C$ Gain (RTI) T. C. $\pm (1 + \frac{50}{G}) \mu V/^{\alpha}C$ Differential Nonlinearity T. C. $\pm 2ppm'^{\alpha}C$ Power Supply Sensitivity $\pm 0.0015\% FSR^{3/6}V_S$ ANALOG INPUTS $\pm 0.0015\% FSR^{3/6}V_S$ Voltage Input Range ( $\frac{ADC FSR}{Gain}$ ) $\pm 10mV$ to $\pm 10V$ (Unipolar)Instrumentation AmplifierResistor ProgrammableGain Range10 000Gain Range $10 000$ Gain Range $10 000$ Gain Equation $G = 1 + (\frac{20k\Omega}{R_G})$ Input Impedance $10^{\beta}\Omega$ Bias Current $50nA$ Offset Current $2nA$ CMR (up to 500Hz) $-80dB$ CMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*ITTL Load, Positive PulseNegative Edge TriggeredSHA ControlHOLD = Logic 0SAMPLE = Logic 1Low Enable, High EnableENABLE = Logic 0DIGITAL OUTPUTSParallel Data OutputsTri-StateUnipolarBinaryBipolarOffset Binary, 2's ComplementOutput Drive2TTL LoadsNTERNAL REFERENCE VOLTAGE $\pm 10V \pm 0.3\%$ External Load Current (Rated Performance) $\pm 15V \pm 5\%, +5V \pm 5\%$ Operating Voltages' $\pm 15V \pm 5\%, +5V \pm 5\%$ Operating Voltages' $\pm 15V \pm 5\%, +5V \pm 5\%$ Operating Voltages' $\pm 15V \pm 5\%, -5V \pm 5\%$ Storage $-25'C$ to $+85'C$ Storage $-25'C$ to $+85'C$ Storage $-25'C$ to $+85'C$ Storage<	Gain Error	Adjustable to Zero	
Other (N II) 1.C. $\pm (1 + \frac{-}{G}) \mu V^{-C}$ Gain (RTI) T.C. $\pm 16pm^{0}C$ Differential Nonlinearity T.C. $\pm 2ppm^{0}C \max$ Power Supply Sensitivity $\pm 0.0015\% FSR^{2}\% V_{S}$ ANALOG INPUTS $\pm 0.0015\% FSR^{2}\% V_{S}$ Voltage Input Range ( $\frac{ADC FSR}{Gain}$ ) $\pm 10mV to \pm 10V (Unipolar)$ Instrumentation Amplifier $\pm 5mV to \pm 5V (Bipolar)$ GainRange $1 to 1000$ Gain Equation $G = 1 + \frac{(20k\Omega)}{R_G}$ Input Impedance $10^{6}\Omega$ Bias Current $20A$ CMR (up to 500Hz) $- 60dB$ CMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*ITTL Load, Positive PulseNADC Convert Command*NTL Load, Positive PulseNABLE = Logic 0DIGITAL OUTPUTSParallel Data OutputsTri-StateUnipolarOffset Binary, 2's ComplementOutput Drive2TTL LoadsStatusLogic ''' During ConversionOutput Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 15V \pm 5\%, + 5V \pm 5\%$ Ated Voltages $\pm 15V \pm 5\%, + 5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%, + 5V \pm 5\%$ Supply Current Drain $\pm 15V$ $\pm 40mA$ +5V80mATEMPERATURE RANGESpenifiedSpecified $0 to + 70^{\circ}C$ Operating $-25^{\circ}C to + 85^{\circ}C$ Storage $-25^{\circ}C to + 85^{\circ}C$	STABILITY	(	
Gain (RTI) T.C. $\pm 16ppm/^{C}$ Differential Nonlinearity T.C. $\pm 2ppm/^{C}C$ axPower Supply Sensitivity $\pm 0.0015\% FSR^{2}\% V_{S}$ ANALOG INPUTS $\pm 0.0015\% FSR^{2}\% V_{S}$ Voltage Input Range ( $\underline{ADC FSR}$ ) $\pm 5mV$ to $\pm 5V$ (Bipolar)Instrumentation Amplifier $ESmV$ to $\pm 5V$ (Bipolar)GainRange $10000$ Gain Equation $G = 1 + (\frac{20kf1}{R_G})$ Input Impedance $10^8f1$ Bias Current $50nA$ Offset Current $2nAA$ CMR (up to 500Hz) $-80dB$ CMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*TTTL Load, Positive PulseNADC Convert Command*SAMPLE = Logic 0SHA ControlHOLD = Logic 0DIGITAL OUTPUTSParallel Data OutputsTri-StateUnipolarBinaryBipolarOffset Binary, 2's ComplementOutput Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 15V \pm 5\%$ , $+5V \pm 5\%$ External Load Current (Rated Performance) $2m(max)$ Temperature Stability $\pm 15V \pm 5\%$ , $+5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%^{C}$ Storage $-25^{CC}$ to $+85^{CC}$ Storage $-25^{CC}$ to	Offset (RTI) T.C.	$\pm (1 + \frac{1}{G}) \mu V/C$	*
$\begin{array}{llllllllllllllllllllllllllllllllllll$	Gain (RTI) T.C.	±16ppm/°C	*
Power Supply Sensitivity $\pm 0.0015\% FSR'7\% V_S$ ANALOG INPUTS $\pm 0.0015\% FSR'7\% V_S$ Voltage Input Range $\left(\frac{ADC FSR}{Gain}\right)$ $\pm 10mV$ to $\pm 5V$ (Bipolar)Instrumentation Amplifier $\pm 5mV$ to $\pm 5V$ (Bipolar)Gain Range1 to 1000Gain Equation $G = 1 + \left(\frac{20k\Omega}{R_G}\right)$ Input Impedance10%1Bias Current50nAOffset Current2nACMR (up to 500Hz) $- 60dB$ CMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*ITTL Load, Positive PulseNegative Edge TriggeredSHA ControlHOLD = Logic 0SAMPLE = Logic 1Low Enable, High EnableENABLE = Logic 0DIGITAL OUTPUTSParallel Data OutputsTri-StateUnipolarOffset Binary, 2's ComplementOutput Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 10V, \pm 0.3\%$ External Load Current (Rated Performance) $2mA(max)$ POWER REQUIREMENTS $\pm 15V \pm 5\%, \pm 5V \pm 5\%$ Rated Voltages $\pm 15V \pm 5\%, \pm 5V \pm 5\%$ Operating Voltages 3 $\pm 15V \pm 5\%, \pm 5V \pm 5\%$ Storage $-25^{\circ}$ C to $\pm 85^{\circ}$ CStorage $-25^{\circ}$ C to $\pm 85^{\circ}$ CStora	Differential Nonlinearity T.C.	± 2ppm/°C max	*
ANALOG INPUTS Voltage Input Range $\left(\frac{\text{ADC FSR}}{\text{Gain}}\right)$ + 10mV to + 10V (Unipolar) + $\pm 5\text{mV to } \pm 5\text{V}$ (Bipolar) + Instrumentation Amplifier Gain Range I to 1000 + Gain Equation G = 1 + $\left(\frac{20\text{kfl}}{R_G}\right)$ + Input Impedance 10 <sup>6</sup> Ω + Bias Current 50nA + CMR (up to 500Hz) - 80dB + CMV ± 10V + DIGITAL INPUTS ADC Convert Command + NC = 200 Hz + 10V + DIGITAL OUTPUTS ADC Convert Command + SHA Control HOLD = Logic 0 DIGITAL OUTPUTS Parallel Data Outputs Tri-State Unipolar Binary Bipolar Offset Binary, 2's Complement Output Drive 2TTL Loads Status Logic **** During Conversion Output Drive 2TTL Loads INTERNAL REFERENCE VOLTAGE + 10V, ± 0.3% External Load Current (Read Performance) 2mA (max) Temperature Stability ± 8.5ppm/*C (max) POWER REQUIREMENTS Rated Voltages ± 15V ± 5%, + 5V ± 5% Operating Voltages ± 15V ± 5%, + 5V ± 5% Operating Voltages ± 15V ± 5%, + 5V ± 5% Stapp (Current Drive 27TCL Conds ± 17V, + 4.75V to + 5.25V Supply Current Drine 275°C to + 85°C Storage - 25°C to	Power Supply Sensitivity	±0.0015%FSR <sup>-</sup> %V <sub>S</sub>	<u> </u>
Voltage Input Range $(ADCFSR)$ + 10mV to + 100V (Unipolar)Instrumentation Amplifier $\pm 5mV$ to $\pm 5V$ (Bipolar)Gain Range1 to 1000Gain Range1 to 1000Gain Equation $G = 1 + (\frac{20K1}{R_G})$ Input Impedance10 <sup>8</sup> ftBias Current20AOffset Current2nACMR (up to 500Hz)- 80dBCMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*TTL Load, Positive PulseNegative Edge TriggeredSHA ControlHOLD = Logic 0SAMPLE = Logic 1Low Enable, High EnableENABLE = Logic 1UnipolarUnipolarOutput DriveOutput DriveOutput DriveOutput DriveOutput DriveZTTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 15V \pm 5\%$ , $\pm 5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%$ , $\pm 5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%$ , $\pm 12V$ to $\pm 17V$ , $\pm 4.75V$ to $\pm 5.25V$ SupplyCurrent Drian $\pm 15V \pm 40mA$ $\pm 5V$ Storage $-25°C$ to $\pm 85°C$ StorageRelative HumidityElectromagnet (EMI) 5 sidesSHZE $27 \cdot 4^{\circ} \times 0.44^{\circ}$ netal package	ANALOGINPUTS		
UsinEntrumentationInstrumentationAmplifierGainRangeGain RangeI to 1000Gain Equation $G = 1 + \left(\frac{20k\Omega}{R_G}\right)$ Input Impedance $10^5$ Bias Current50nAOffset Current2nACMR (up to 500Hz)- 80dBCMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*ITTL Load, Positive PulseNegative Edge TriggeredSHA ControlHOLD = Logic 0SAMPLE = Logic 1Low Enable, High EnableENABLE = Logic 0DIGITAL OUTPUTSParallel Data OutputsTri-StateUnipolarBinaryBipolarOffset Binary, 2's ComplementOutput Drive2TTL LoadsStatusLogic "I" During ConversionOutput Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE $\pm 10V \pm 5\%$ , $\pm 5V \pm 5\%$ POWER REQUIREMENTS $\pm 15V \pm 5\%$ , $\pm 5V \pm 5\%$ Rated Voltages $\pm 15V \pm 5\%$ , $\pm 5V \pm 5\%$ Operating Voltages? $\pm 12V to \pm 17V$ , $\pm 4.75V$ to $\pm 5.25V$ Supply Current Drain $\pm 15V$ $\pm 40mA$ $\pm 5V$ 80mATEMPERATURE RANGESpecifiedOperating Voltages? $-25^{\circ}C to \pm 85^{\circ}C$ Storage $-25^{\circ}C to \pm 85^{\circ}C$ Relative HumidityElectromagnet (EMI) 5 sidesSHIELDINGElectromagnet (EMI) 5 sidesSHIELDINGElectromagnet (EMI) 5 sidesSIZE2" 4" × 0.44" aretal package	Voltage Input Range (ADC FSR)	+10mV to $+10V$ (Unipolar)	*
Gain Gain RangeResistor Programmable 	Instrumentation Amplifier	± 5mv to ± 5v (Bipolar)	•
Gain Range1 to 1000Gain Equation $G = 1 + \frac{(20kf1)}{R_G}$ Input Impedance10%1Bias Current50nAOffset Current2nACMR (up to 500Hz)- 80dBCMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*ITTL Load, Positive PulseNCC Convert Command*Negative Edge TriggeredSHA ControlHOLD = Logic 0SAMPLE = Logic 1Low Enable, High EnableENABLE = Logic 0DIGITAL OUTPUTSParallel Data OutputsTri-StateUnipolarBinaryBipolarOffset Binary, 2's ComplementOutput Drive2TTL LoadsINTERNAL REFERENCE VOLTAGE+ 10V, $\pm 0.3\%$ External Load Current (Rated Performance)2nA (max)Temperature Stability $\pm 15V \pm 5\%$ , $+ 5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%$ , $+ 5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%$ , $+ 5V \pm 5\%$ Operating Voltages $\pm 15V \pm 5\%$ , $- 52SV$ Supply Current Drina $\pm 15V \pm 40mA$ $\pm 30mA$ TEMPERATURE RANGESpecifiedOut + 70°COperatingOperating- 25°C to $\pm 85°C$ Storage- 25°C to $\pm 85°C$ Relative Humidity(Meets MIL-STD-202E, Method 103B)SHIELDINGElectromagnet (EMI) 5 sidesSIZE $2^* \times 4^* \times 0.44^*$ metal package	Gain	Resistor Programmable	*
Gain Equation $G = 1 + \frac{(20kT)}{R_G}$ Input Impedance $10^{8}\Omega$ Bias Current $50nA$ Offset Current $2nA$ CMR (up to 500Hz) $-80dB$ CMV $\pm 10V$ DIGITAL INPUTSADC Convert Command*ITTL Load, Positive PulseNegative Edge TriggeredSHA ControlHOLD = Logic 0SAMPLE = Logic 1Low Enable, High EnableENABLE = Logic 0DIGITAL OUTPUTSParallel Data OutputsTri-StateUnipolarDifartyBipolarOffset Binary, 2's ComplementOutput Drive2TTL LoadsNTERNAL REFERENCE VOLTAGE $\pm 10V, \pm 0.3\%$ External Load Current (Rated Performance) $2mA (max)$ Temperature Stability $\pm 8.5ppm'C(max)$ POWER REQUIREMENTS $\pm 15V \pm 5\%, \pm 5V \pm 5\%$ Rated Voltages $\pm 15V \pm 5V\%, \pm 0.25V$ Supply Current Drain $\pm 15V \pm 40mA$ $\pm 5V$ 80mATEMPERATURE RANGE $0 to + 70^{\circ}C$ Operating Voltages $-25^{\circ}C to + 85^{\circ}C$ Storage	Gain Range	1 to 1000	*
Input Impedance 10 <sup>4</sup> C1 Bias Current 50nA CMR 200 CMV 200Hz) - 80dB CMV 200Hz CMV ±10V 200Hz CMV 200Hz C	Gain Equation	$G = 1 + \left(\frac{20k\Omega}{D}\right)$	*
Input impedance     10°11       Biss Current     2nA       CMR (up to 500Hz)     -80dB       CMV     ± 10V       DIGITAL INPUTS     Negative Edge Triggered       ADC Convert Command*     ITTL Load, Positive Pulse       NCBUT     Negative Edge Triggered       SHA Control     HOLD = Logic 0       SAMPLE = Logic 1     Edwards       Low Enable, High Enable     ENABLE = Logic 1       Low Enable, High Enable     ENABLE = Logic 0       DIGITAL OUTPUTS     Tri-State       Unipolar     Binary       Bipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       Status     Logic*1" During Conversion       Output Drive     2TATL Loads       INTERNAL REFERENCE VOLTAGE     +10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     Rated Voltages       Rated Voltages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages3     ± 12V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     Soma       Specified     0 to + 70°C       Operating     -25°C to + 85°C       Relative Humidity	I	KG /	*
Differ Current     2nA       Offset Current     2nA       CMR (up to 500H2)     -80dB       CMV     ± 10V       DIGITAL INPUTS     TTTL Load, Positive Pulse       ADC Convert Command <sup>4</sup> ITTL Load, Positive Pulse       Negative Edge Triggered     HOLD = Logic 0       SHA Control     HOLD = Logic 0       SAMPLE = Logic 1     Low Enable, High Enable       Enable, High Enable     ENABLE = Logic 0       DIGITAL OUTPUTS     Parallel Data Outputs       Parallel Data Outputs     Tri-State       Unipolar     Binary       Bipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2nA (max)       Temperature Stability     ± 8.5ppm/°C(max)       POWER REQUIREMENTS     Rated Voltages       Active Adoma     + 5V       SomA     + 5V       TEMPERATURE RANGE     SomA       Specified     Oto + 70°C       Operating     - 25°C to + 85°C       Storage     - 25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electronstatic RFI) 6 sides, Electronstatic RFI) 5 sides       SIZE     2″ 4″ 4′ × 0.44″ metal package <td>Bias Current</td> <td>10-17 50m A</td> <td>*</td>	Bias Current	10-17 50m A	*
CMR (up to 500Hz)     - 80dB       CMV     ± 10V       DIGITAL INPUTS     Negative Edge Triggered       ADC Convert Command <sup>4</sup> ITTL Load, Positive Pulse       Negative Edge Triggered     SHA Control       HOLD = Logic 0     SAMPLE = Logic 1       Low Enable, High Enable     ENABLE = Logic 0       DIGITAL OUTPUTS     Parallel Data Outputs       Parallel Data Outputs     Tri-State       Unipolar     Binary       Bipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       Status     Logie "I" During Conversion       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA(max)       POWER REQUIREMENTS     ± 3.5pm/°C(max)       POWER REQUIREMENTS     ± 15V ± 5%, + 5V ± 5%       Operating Voltages     ± 15V to ± 17V, ± 4.75V to ± 5.25V       Supply Current Drain ± 15V     ± 40mA       + 5V     80mA       TEMPERATURE RANGE     Specified       Operating Voltages     - 25°C to ± 85°C       Storage     - 25°C to ± 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electromagnet (EMI) 5 sides       SHIELDING     Electromagnet (EMI) 5 sides	Offset Current	2nA	*
CMV     ± 10V       DIGITAL INPUTS       ADC Convert Command*       ITTL Load, Positive Pulse       Negative Edge Triggered       SHA Control     HOLD = Logic 0       SAMPLE = Logic 1       Low Enable, High Enable     ENABLE = Logic 1       DIGITAL OUTPUTS       Parallel Data Outputs     Tri-State       Unipolar     Binary       Bipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     ± 100, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     # 15V ± 5%, + 5V ± 5%       Operating Voltages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages     ± 15V ± 5%, - 525V       Supply Current Drini ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     50ct + 85°C       Storage     - 25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RTI) 6 sides, Electrostatic (RTI) 5 sides       SIZE     2" × 4" × 0.44" metal package	CMR (up to 500Hz)	- 80dB	*
DIGITAL INPUTS     ITTL Load, Positive Pulse       Negative Edge Triggered     Negative Edge Triggered       SHA Control     HOLD = Logic 0       SAMPLE = Logic 1     ENABLE = Logic 0       DIGITAL OUTPUTS     Tri-State       Unipolar     Binary       Bipolar     Offset Binary, 2's Complement       Output Drive     ZTTL Loads       Status     Logic ''1' During Conversion       Output Drive     ZTTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Retad Performance)     ZnA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     at 21V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     Socified       Ot to + 70°C     Operating       Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI)6 sides, Electrostatic (RFI)5 sides       SIZE     2″ × 4″ × 0.44″ metal package	CMV	±10V	*
ADC Convert Command <sup>4</sup> ITTL Load, Positive Pulse Negative Edge Triggered HOLD = Logic 0 SAMPLE = Logic 0       SHA Control     HOLD = Logic 0       SAMPLE = Logic 1     ENABLE = Logic 0       DIGITAL OUTPUTS     Finary       Parallel Data Outputs     Tri-State       Unipolar     Difary 2's Complement       Output Drive     ZTTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     Rated Voltages       Active to the system of the s	DIGITAL INPUTS		,
Negative Edge Triggered       HOLD = Logic 0       SAMPLE = Logic 1       Low Enable, High Enable     ENABLE = Logic 0       DIGITAL OUTPUTS       Parallel Data Outputs     Tri-State       Unipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       Status     Logic "1" During Conversion       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       POWER REQUIREMENTS     ± 3.5pm/°C (max)       POWER REQUIREMENTS     ± 15V ± 5%, + 5V ± 5%       Operating Voltages     ± 15V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       + 5V     80mA       TEMPERATURE RANGE     Specified       Oto + 70°C     Storage       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electromagnet (EMI) 5 sides       SHZE     2" × 4" × 0.44" metal package	ADC Convert Command <sup>4</sup>	ITTL Load, Positive Pulse	
SHA Control     HOLD = Logic 0 SAMPLE = Logic 1       Low Enable, High Enable     ENABLE = Logic 1       DIGITAL OUTPUTS     Finany       Parallel Data Outputs     Tri-State       Unipolar     Binary       Bipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       Status     Logic '1'' During Conversion       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     Rated Volages       Atot Volages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages'     ± 12V to ± 17V, + 4.75V to + 5.25V       Supply Current Drin ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     Storage       Specified     0 to + 70°C       Operating     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RTI) 6 sides, Electrostatic (RTI) 5 sides       SIZE     2" × 4" × 0.44" metal package		Negative Edge Triggered	
SAMPLE     = Logic 1       Low Enable, High Enable     ENABLE     = Logic 0       DIGITAL OUTPUTS     Tri-State     Unipoloa       Parallel Data Outputs     Tri-State       Unipolar     Binary       Bipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       Status     Logic*'1'During Conversion       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     Rated Voltages       Att Voltages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages <sup>3</sup> ± 12V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     Specified       Otro + 70°C     Operating       Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides       SIZE     2″ * 4″ × 0.44″ netal package	SHA Control	HOLD = Logic 0	
DIGITAL OUTPUTS       Parallel Data Outputs       Tri-State       Unipolar       Bipolar       Output Drive       ZTTL Loads       Status     Logie "I" During Conversion       Output Drive     ZTTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     Rated Voltages       Appendix Voltages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages     ± 12V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       + 5V     80mA       TEMPERATURE RANGE     Specified       Operating     - 25°C to + 85°C       Storage     - 25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electromagnet (EMI) 5 sides       SIZE     2″ × 4″ × 0.44″ metal package	Low Enable, High Enable	SAMPLE = Logic I ENABLE = Logic 0	
DIGIAL OUTPUTS         Parallel Data Outputs       Tri-State         Unipolar       Binary         Bipolar       Offset Binary, 2's Complement         Output Drive       2TTL Loads         Status       Logic "1" During Conversion         Output Drive       2TTL Loads         INTERNAL REFERENCE VOLTAGE       +10V, ± 0.3%         External Load Current (Rated Performance)       2mA (max)         Temperature Stability       ± 8.5ppm/°C(max)         POWER REQUIREMENTS       Rated Voltages         Rated Voltages       ± 15V ± 5%, + 5V ± 5%         Operating Voltages <sup>2</sup> ± 12V to ± 17V, + 4.75V to + 5.25V         Supply Current Drain ± 15V       ± 40mA         +5V       80mA         TEMPERATURE RANGE       Specified         Storage       -25°C to + 85°C         Relative Humidity       (Meets MIL-STD-202E, Method 103B)         SHIELDING       Electrostatic (RFI) 6 sides, Electrostatic (RFI) 6 sides,         Electrostatic (RFI) 6 sides,       Electrostatic (RI) 5 sides         SIZE       2" × 4" × 0.44" metal package			÷
Paramer Data Outputs     Inividue       Unipolar     Binary       Bipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       Status     Logic "1" During Conversion       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     Rated Volages       Attages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages <sup>3</sup> ± 12V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     Specified       Oto + 70°C     Operating       -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RTI) 6 sides, Electrostatic (RTI) 5 sides       SIZE     2" × 4" × 0.44" metal package	DIGITAL OUTPUTS Parallal Data Outputs	Tei Stata	
Bipolar     Offset Binary, 2's Complement       Output Drive     2TTL Loads       Status     Logic "1" During Conversion       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2nA (max)       Temperature Stability     ± 8.5ppm/°C(max)       POWER REQUIREMENTS     Rated Voltages       Action Voltages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages     ± 12V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     Specified       Oto + 70°C     Operating       Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electromagnet (EMI) 5 sides       Electromagnet (EMI) 5 sides     Electrostatic RTJ 6 sides,       Electrostatic RTJ 6 sides,     Electrostatic RTJ 6 sides,       Electrostatic RTJ 6 sides,     Electrostatic RTJ 6 sides,       Electrostatic RTJ 6 sides,     Electrostatic RTJ 6 sides,	Unipolar	Binary	
Output Drive     2TTL Loads       Status     Logic "1" During Conversion       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       POWER REQUIREMENTS     # 8.5ppm/°C (max)       POWER REQUIREMENTS     ± 15V ± 5%, + 5V ± 5%       Operating Voltages     ± 15V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       + 5V     80mA       TEMPERATURE RANGE     Specified       Specified     0 to + 70°C       Operating     - 25°C to + 85°C       Storage     - 25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides       SIZE     2" × 4" × 0.44" metal package	Bipolar	Offset Binary, 2's Complement	
Status     Logic "1" During Conversion       Output Drive     2TTL Loads       INTERNAL REFERENCE VOLTAGE     + 10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     Rated Voltages       Rated Voltages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages <sup>2</sup> ± 12V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     Specified       Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI)6 sides, Electrostaget       SIZE     2" × 4" × 0.44" metal package	Output Drive	2TTL Loads	
Output Drive     2111 Loads       INTERNAL REFERENCE VOLTAGE     +10V, ± 0.3%       External Load Current (Rated Performance)     2mA (max)       Temperature Stability     ± 8.5ppm/°C (max)       POWER REQUIREMENTS     Rated Volages       Rated Volages     ± 15V ± 5%, + 5V ± 5%       Operating Voltages <sup>5</sup> ± 12V to ± 17V, + 4.75V to + 5.25V       Supply Current Drain ± 15V     ± 40mA       +5V     80mA       TEMPERATURE RANGE     Specified       Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RTI) 6 sides, Electrostatic (RTI) 5 sides       SIZE     2″ × 4″ × 0.44″ metal package	Status	Logic "1" During Conversion	
INTERNAL REFERENCE VOLTAGE         + 10V, ± 0.3%           External Load Current (Rated Performance)         2mA (max)           Temperature Stability         ± 8.5ppm/°C(max)           POWER REQUIREMENTS         Rated Volages           Rated Volages         ± 15V ± 5%, + 5V ± 5%           Operating Voltages <sup>2</sup> ± 12V to ± 17V, + 4.75V to + 5.25V           Supply Current Drain ± 15V         ± 40mA           + 5V         80mA           TEMPERATURE RANGE         Specified           Operating         - 25°C to + 85°C           Storage         - 25°C to + 85°C           Relative Humidity         (Meets MIL-STD-202E, Method 103B)           SHIELDING         Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides           SIZE         2″ × 4″ × 0.44″ metal package	Output Drive	ZTTL Loads	
External Load Current (Rated Performance)       ZmA (max)         Temperature Stability       ± 8.5ppm/°C (max)         POWER REQUIREMENTS       Rated Voltages         Parating Voltages'       ± 15V ± 5%, + 5V ± 5%         Operating Voltages'       ± 12V to ± 17V, + 4.75V to + 5.25V         Supply Current Drain ± 15V       ± 40mA         + 5V       80mA         TEMPERATURE RANGE       0 to + 70°C         Operating       - 25°C to + 85°C         Storage       - 25°C to + 85°C         Relative Humidity       (Meets MIL-STD-202E, Method 103B)         SHIELDING       Electrostatic (RFI) 6 sides, Electrostaget (EHI) 5 sides         SIZE       2″ × 4″ × 0.44″ metal package	INTERNAL REFERENCE VOLTAGE	$+10V, \pm 0.3\%$	
Temperature Stability         ± 8.3ppm/ <sup>1</sup> /c (max)           POWER REQUIREMENTS         # 3.3ppm/ <sup>1</sup> /c (max)           Rated Voltages         ± 15V ± 5%, + 5V ± 5%           Operating Voltages <sup>3</sup> ± 12V to ± 17V, + 4.75V to + 5.25V           Supply Current Drain ± 15V         ± 40mA           +5V         80mA           TEMPERATURE RANGE         Specified           Operating         -25°C to + 85°C           Operating         -25°C to + 85°C           Relative Humidity         (Meets MIL-STD-202E, Method 103B)           SHIELDING         Electrostatic (RFI) 6 sides, Electrostaget (EII) 5 sides           SIZE         2″ × 4″ × 0.44″ metal package	External Load Current (Rated Performance)	2mA (max)	
POWER REQUIREMENTS           Rated Voltages         ± 15V ± 5%, + 5V ± 5%           Operating Voltages <sup>5</sup> ± 12V to ± 17V, + 4.75V to + 5.25V           Supply Current Drain ± 15V         ± 40mA           +5V         80mA           TEMPERATURE RANGE         50mA           Specified         0 to + 70°C           Operating         -25°C to + 85°C           Storage         - 25°C to + 85°C           Relative Humidity         (Meets MIL-STD-202E, Method 103B)           SHIELDING         Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides           SIZE         2″ × 4″ × 0.44″ metal package	I emperature Stability	± 8.5ppm/°C(max)	
Rated Voltages         ± 15V ± 5%, +5V ± 5%           Operating Voltages <sup>2</sup> ± 12V to ± 17V, +4.75V to +5.25V           Supply Current Drain ± 15V         ± 40mA           + 5V         80mA           TEMPERATURE RANGE         50mA           Specified         0 to + 70°C           Operating         - 25°C to + 85°C           Storage         - 25°C to + 85°C           Relative Humidity         (Meets MIL-STD-202E, Method 103B)           SHIELDING         Electromagnet (EMI) 5 sides, Electromagnet (EMI) 5 sides           SIZE         2″ × 4″ × 0.44″ metal package	POWER REQUIREMENTS	· · · · · · · · · · · · · · · · · · ·	
Operating voltages*     ±12V to ±1/Y, +4.75V to ±3.25V       Supply Current Drain ±15V     ±40mA       +5V     80mA       TEMPERATURE RANGE     0 to + 70°C       Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electrostatic (RFI) 5 sides       SIZE     2″ × 4″ × 0.44″ metal package	Rated Voltages	$\pm 15V \pm 5\%, \pm 5V \pm 5\%$	
Supply Culture 13V     2-totini       +5V     80mA       TEMPERATURE RANGE     0 to + 70°C       Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electrostatic (RFI) 5 sides       SIZE     2" × 4" × 0.44" metal package	Operating Voltages <sup>2</sup> Supply Current Drain + 15V	$\pm 120$ to $\pm 1/0$ , $\pm 4.750$ to $\pm 5.250$	
TEMPERATURE RANGE     0 to + 70°C       Operating     - 25°C to + 85°C       Storage     - 25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electrostatic (RFI) 6 sides       SIZE     2" × 4" × 0.44" metal package	+ SV	80mA	
Non-Excit Contention     0 to + 70°C       Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides       SIZE     2" × 4" × 0.44" metal package	TEMPEDATURE DANGE		
Operating     -25°C to + 85°C       Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electrostatic (RFI) 5 sides       SIZE     2" × 4" × 0.44" metal package	Specified	$0$ to $\pm 70^{\circ}$ C	
Storage     -25°C to + 85°C       Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electrostatic (RFI) 6 sides       SIZE     2" × 4" × 0.44" metal package	Operating	- 25°C to + 85°C	
Relative Humidity     (Meets MIL-STD-202E, Method 103B)       SHIELDING     Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides       SIZE     2" × 4" × 0.44" metal package	Storage	- 25°C to + 85°C	
SHIELDING     Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides       SIZE     2" × 4" × 0.44" metal package	Relative Humidity	(Meets MIL-STD-202E, Method 103E	i)
Electromagnet (EMI) 5 sides           SIZE         2" × 4" × 0.44" metal package	SHIELDING	Electrostatic (RFI) 6 sides,	<b>_</b>
SIZE 2" × 4" × 0.44" metal package		Electromagnet (EMI) 5 sides	
	SIZE	$2'' \times 4'' \times 0.44''$ metal package	,

NOTES

NOTES Messured in hold mode, input 20V pk-pk @ 10kHz. FSR means Full Scale Range. Worst-case summation of IA, S/I and A/D nonlinearity errors. When connecting the Convert Command the S/I control terminals together, the puke width must be long enough for the S/I amplifier to acquire the input signal to the required accuracy  $4\mu_S$  (min, DAS1155)  $5\mu_s$  (min, DAS1156). M = 12V operating power supply is used, the analog input must be limited to  $\pm 7V$ . Recommended Power Supply: Analog Devices Model 923. Same specifications as for DAS1155. Specifications subject to change without notice.

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



#### INTERCONNECTION AND SHIELDING TECHNIQUES

To preserve the high CMR characteristics of the DAS1155/DAS1156, care must be taken to minimize noise wherever possible. For best performance use twisted shielded cable, for the sensitive input signal, to reduce inductive and capacitive pickup. The cable should be connected as close as possible to the input common mode signal source. Place the gain setting resistor as close as possible to its respective terminal connections to avoid pickup.



Figure 2. Analog Input Block Diagram

The gain T.C., of the DAS1155/DAS1156, will be directly affected by the resistor used for  $R_G$ . Using a high quality metal film resistor is recommended. Bipolar operation is obtained by connecting the REF OUT and the BIPOLAR OFFSET terminals together.

The output of the instrumentation amplifier drives the sample/hold amplifier which has a gain of 1V/V. The sample/hold amplifier holds the input signal at a constant level during the A/D conversion. Acquisition times of 4 $\mu$ s and 5 $\mu$ s maximum are provided respectively by the DAS1155 and DAS1156. Full scale A/D converter input range is programmed for + 10V (unipolar) or ± 5V (bipolar). Therefore, the instrumentation amplifier gain must be set accordingly to obtain maximum usable resolution.

#### COMMON MODE REJECTION

CMR is dependent on source impedance imbalance, signal frequency, and amplifier gain. CMR is specified having a  $\pm 10V$  CMV and  $1k\Omega$  source imbalance over a frequency range of dc to 500Hz. Figure 3 illustrates the typical CMR vs. source impedance



Figure 3. CMR vs Gain and Source Imbalance DAS1155/ DAS1156



Figure 4. CMR vs Frequency DAS1155/DAS1156

### Applying the DAS1155/DAS1156

imbalance for the DAS1155/DAS1156. Increasing the input gain of the instrumentation amplifier increases the CMR. At Gain = 1V/V, CMR is maintained greater than 80dB for source impedance imbalance up to  $10k\Omega$ . Figure 4 illustrates the CMR vs. gain and frequency.

#### SETTLING TIME VS. GAIN

Illustrated in Figure 5 is the typical settling time vs. gain of the instrumentation amplifier in the DAS1155/DAS1156. Settling times are specified to 0.003% FSR for gains 1 and 10, and to 0.01% FSR for gain to 1000 having an output step voltage of 10 volts. Settling time to 0.003% FSR for gains greater than 10 are not shown because of the effects of voltage noise at the higher gains.



Figure 5. Typical Settling Time vs Gain

#### TIMING DIAGRAM

The timing diagram for the DAS1155/DAS1156 is illustrated in Figure 6. This figure includes the sample/hold amplifier characteristics and assumes that the instrumentation amplifier is allowed to settle during the previous conversion.



NOTES

///// 1. Output Data Valid.

 This Diagram assumes that the Instrumentation Amplifier is allowed sufficient time to settle before the Sample/Hold Amplifier is placed in the Sample Mode. Instrumentation Amplifier settling can take place during the A/D Conversion process for the next conversion (see throughput rate).

 The S/H Control and Trigger are tied together, Pulse Width must be 4µs (min)/5µs (min) to allow the S/H Amplifier to acquire the Input Signal.

#### Figure 6. DAS1155/DAS1156 Timing Diagram

The TRIGGER input and S/H CONTROL terminal can be tied together requiring only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of  $4\mu$ s/5 $\mu$ s, for the DAS1155/DAS1156 respectively, to insure accuracy is attained. At the falling edge of the TRIGGER pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion

#### DATA ACQUISITION SUBSYSTEMS VOL. II, 15-19

begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The internal DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking 35µs/ 44µs maximum respectively for the DAS1155/DAS1156.

At this time, the STATUS line goes low signifying that the conversion is complete. For bus applications, the digital output can now be applied to the selected data bus by enabling the tri-state buffers with the HI-ENABLE and LO-ENABLE terminals.

#### GAIN AND OFFSET ADJUSTMENTS

The DAS1155/DAS1156 each are provided with internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed first. Proper gain and offset calibration require great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within  $\pm 1/10$ LSB of the desired value at any point within its range.

The analog input values given in Tables I, II, III and in the following Offset & Gain Calibration Section, are values that should be present at the input to the internal ADC. The value of the analog input will be affected by the gain of the input instrumentation amplifier.(Example: For a full scale input of 0 to +5V, divide the 0 to +10V range input values by 2 and set input gain to 2.)

Analog 0 to + 10	Input V Range	Digital Output Binary Code		
DAS1155	DAS1156	DAS1155	DAS1156	
+9.99939V	+ 9.99969V	11 111 111 111 111	111 111 111 111 111	
+ 5.00000V	+ 5.00000V	10 000 000 000 000	100 000 000 000 000	
+1.25000V	+1.25000V	00 100 000 000 000	001 000 000 000 000	
+0.0006V	+0.0003V	00 000 000 000 001	000 000 000 000 001	
+0.0000V	+0.0000V	00 000 000 000 000	000 000 000 000 000	

Table I. Nominal Unipolar/Output Relationships

Analog Input	Digital Output					
±5V Range	Offset Binary Code	Two's Complement Code				
+4.99939V	11 111 111 111 111	01 111 111 111 111				
+2.50000V	11 000 000 000 000	01 000 000 000 000				
+0.00061V	10 000 000 000 001	00 000 000 000 001				
+0.00000V	10 000 000 000 000	00 000 000 000 000				
-5.00000V	00 000 000 000 000	10 000 000 000 000				

Table II. DAS1155 Bipolar Input/Output Relationships

Analog Input	Digital Output					
±5V Range	Offset Binary Code	Two's Complement Code				
+4.99969V	111 111 111 111 111	011 111 111 111 111				
+2.50000V	110 000 000 000 000	010 000 000 000 000				
+0.00030V	100 000 000 000 001	000 000 000 000 001				
+0.00000V	100 000 000 000 000	000 000 000 000 000				
-5.00000V	000 000 000 000 000	100 000 000 000 000				

Table III. DAS1156 Bipolar Input/Output Relationships

For 0 to +10V unipolar range set the input voltage precisely to  $+305\mu$ V for the DAS1155 and  $+153\mu$ V for the DAS1156. Then adjust the zero potentiometer until the converter is just on the verge of switching from 00-----00 to 00-----01.

For the  $\pm 5V$  bipolar range set the input voltage precisely to  $+305\mu$ V for the DAS1155 and  $+153\mu$ V for the DAS1156. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 00-----00 to 00-----01 and the two's complement coded units are just on the verge of switching from 10-----01 to 10-----01.

#### GAIN CALIBRATION

**OFFSET CALIBRATION** 

Set the input voltage precisely to +9.99909 (DAS1155)/ +9.99954V (DAS1156) for the 0 to +10V units, or +4.99909V(DAS1155)/+4.99954V (DAS1156) for ±5V units. Note that these values are 1 1/2LSB less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11-----10 to 11-----11 and two's complement coded units are just on the verge of switching from 011-----10 to 011-----11.

#### THROUGHPUT RATE

Throughput rates for the DAS1155/DAS1156 can be increased by the use of the OVERLAP MODE, i.e. updating the input while the ADC is making a conversion.

The guaranteed throughput rates are  $25 \text{kHz} \oplus \text{G} = 1$ , 20 kHz $(\widehat{a} G = 1000 \text{ for the DAS1155 and } 20 \text{kHz} (\widehat{a} G = 1 \text{ and } 1000 \text{ s})$ for the DAS1156. When the IA settling time is less than or equal to the sum of SHA acquisition time and ADC conversion time, 39µs, the DAS throughput rate equals 1/39µs or 25.6kHz. When IA settling time is greater than 39µs (see Figure 5), the DAS throughput rate becomes dependent upon the IA settling time and equals its reciprocal.

#### DAS1155/DAS1156 INPUT/OUTPUT RELATIONSHIPS

The DAS1155/DAS1156 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary code while the  $(\overline{MSB})$  is used to obtain the two's complement code. Table I shows the unipolar analog input/digital output DAS1155/DAS1156 relationships. Tables II and III show the DAS1155/DAS1156 bipolar analog input/digital output relationships respectively.

#### TRI-STATE DIGITAL OUTPUT

The digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data buss in either a one-byte or a two-byte format by using the HI-ENABLE and LO-ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

#### POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1155/DAS1156, care must still be taken to provide proper grounding due to the high accuracy nature of the devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1155/ DAS1156 terminals.

No power supply decoupling is required since, both the DAS1155 and DAS1156, contain high quality tantalum capacitors on each of the power supply inputs to ground.

# **Digital Panel Instruments**

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•New product since publication of 1982-1983 Databook Update.

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# **Selection Guide Digital Panel Instruments**

For the purpose of selection, the instruments in this section are divided into three classes, each having its own Selection Guide:

- 1. 3- to 4 3/4-digit panel meters for general applications, powered by dc voltage furnished by the user's instrumentation-system +5V logic supply
- 2. 3- to 4 3/4-digit panel meters for general applications, powered by ac line voltage, and including multi-channel scanning and true-rms types
- 3. Single- and scanning multi-channel digital temperature meters for measurements with thermocouples, RTDs, thermistors, and AD590 semiconductor temperature sensors

The Selection Guides permit all the devices in each class to be compared in terms of their salient features, to narrow the field of choice to one or two devices, for which page locations are given. The data sheets in this Volume have technical

		LOGIC (+5V) POWERED DIGITAL PANEL METERS							
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Digits; F.S. Range	3;-99 to +999mV	•							
	3½;±199.9mV ±1.999V ±19.99V		•	•	•				
	4½;±1.9999V ±19.999V	•				•	•		
	4¾;±3.9999V ±39.999V							•	
Іприт Туре	Ltd. Differential Differential	•	•	•	•		•	•	
	Floating	-				•			1
Data Outputs	Character Serial Parallel BCD Parallel BCD Latched		•		•		•	•	
Display Type	LED Gas Discharge	•	•	•	•	•	•	•	
Display Size in/mn	1	0.5/13	0.55/14	0.27/7	0.5/13	0.27/7	0.43/11	0.43/11	1
Max Case Depth <sup>1</sup> i	n/mm	0.65/17	4.8/122	1.4/36	1.9/48	3.3/84	4.8/122	4.8/122	<b>.</b> .
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NOTE

<sup>1</sup> Case depth includes mating connector. All logic powered DPMs use industry standard case with 3.175" × 1.810" (80.65 × 45.97mm) cutout. All ac-powered DPMs except AD2006 use industry standard case with 3.930" × 1.682"

(99.82 × 42.72mm) cutout. AD2006 uses same case as logic powered DPMs.

descriptions, specifications, and in many cases, applications information. Complete data sheets for most of these instruments, with further information on application and use of the products, are available upon request. General information on digital panel instruments can be found in the pages that follow the Selection Guides.

For temperature instrumentation, there are a number of other products dedicated to temperature measurement, included in this Databook, that may be of interest. They are to be found in these sections: Transducers & Signal Conditioners,  $\mu$ MAC-4000 Intelligent Measurement-and-Control Subsystems, and MACSYM. Power supplies for excitation of systempowered panel instruments may be found in the Power Supply section.

Finally, in the Synchro & Resolver Conversion section, there are the benchtop API1620 and API1718 Angle Position Indicators, which accept synchro or resolver input, convert to digital, and provide a 5-digit numerical LED display of the angle, and a 5-decade BCD or 16-bit binary data output.

		AC-POWERED DIGITAL PANEL METERS						
		40,00	40,000 × 20,000	40.00 total	Porton Porton	. Alerra and a second	C C C C C C C C C C C C C C C C C C C	7
6-Channel Scanning							•	
Digits; F.S. Range	3; -99 to +999mV	•						
•	3½;±199.9mV ±1.999¥ ±19.99V 199.9V 600V		•	•			•	
	4½; ±1.9999V ±19.999V				•			
	4¾; ±3.9999V ±39.999V					•		
Input Type	Single Ended Ltd. Differential Differential		•	•	•	•	•	
	Floating True RMS	• /					•	
Data Outputs	Character Serial Parallel BCD Parallel BCD Latched		•	•	•	•-	•	
Display Type	LED Gas Discharge	•	•	•	•	•		
Display Size in/mm		0.5/13	0.55/14	0.5/13	0.43/11	0.43/11	0.5/13	
Max Case Depth <sup>2</sup> in/mm		2.44/63	4.95/126	4.77/121	5.3/135	5.3/135	6.03/153	
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NOTES

<sup>1</sup> Full scale inputs when reading out in dB are 500mV, 5V, 50V, 500V and 625V rms.

<sup>2</sup>Case depth includes mating connector. All logic powered DPMs use industry standard case with 3.175" × 1.810"

(80.65 × 45.97mm) cutout. All ac-powered DPMs except AD2006 use industry standard case with 3.930" × 1.682"

(99.82 × 42.72mm) cutout. AD2006 uses same case as logic powered DPMs.

# **Selection Guide** Digital Panel Instruments

				<u> </u>		DIGI TRA	TAL TEN	NPERAT ER METI	URE/ ERS		
	,		- Ţ	<sup>4</sup> D <sub>2</sub> n,	50° - 60°	873, <sup>2</sup> 07	040 1030	000 400 V	15 20	000 (00 100 100 100 100 100 100 100 100	
Input	Number of Channels	1 6	•		•	•	•	•	•	•	
Sensor (Determines Temperature Range)	Thermocouple Type	Switch Selected User Specified J, K, T E, R, S	•	-			•	•	•	•	
	AD590 (-55°C t RTD Thermistor	o +150°C)		•	•	•			•	•	
Features	Self-Calibration Cold-Junction C Linearization	ompensation	:				•	•	•	•	
	Isolation		•	•	•		•1	•1		● <sup>1</sup>	
Readout	Digits	3+, 2- 3 <sup>1</sup> / <sub>2</sub>	•	•	•	•	•	•			
	LED Display Height	0.5", 13mm 0.56", 14.3mm	•	•	•	•		•			
Digital Data Output	Isolated Parallel 7-Bit Character-S Isolated, 20mA c	BCD, Latched erial ASCII current loop	•	•	•		•		•	•	
Analog Output	Voltage		•	•	•		•	•		•	
Power Supply	AC Line DC +7.5V to +2 +5V +12V	8V	•	•	•	•	:	•	•	•	
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NOTE

<sup>1</sup> AC line-operated versions.

Shading indicates new product since publication of 1982–1983 Databook Update.

# **Orientation** Digital Panel Instruments

#### UNDERSTANDING DPMS

#### Introduction

A DPM is basically an analog to digital converter with a visual readout. The DPM samples the input voltage periodically, converts that voltage to digital outputs, and displays the corresponding reading visually. A digital panel meter, then, consists of four basic functional sections: the input section, including signal conditioning and analog to digital conversion circuitry; the display; the data outputs; and the power supply.

#### Processing The Input Signal

The primary function of the input section is to convert an analog voltage input into a digital signal for display. Besides this basic function, the input section also buffers the input to provide a high input impedance, prevent circuit damage in overvoltage conditions, reject both normal mode and common mode noise on the input signal, compensate for large variations in operating temperature, and sometimes even measure the ratio of two separate input voltages.

The analog to digital conversion scheme used on most DPMs is the dual-slope type, due to its inherent stability and normal mode noise rejection. The dual slope converter can also be used to measure the ratio of two input voltages, in some DPM designs. Lower-resolution DPMs sometimes use staircase or single slope converters, which require RC filtering of the input signal for normal mode noise rejection.

The input of the DPM may be single-ended, differential or floating. Single-ended inputs measure the input voltage with respect to input common and may require some care in application to avoid ground loop problems. To prevent ground loops, some of Analog Devices' DPMs use a "limited differential input", where a resistor separates analog and digital grounds, allowing up to 200mV of common mode voltage and providing up to 60dB of common-mode rejection.

True differential input DPMs accommodate common mode voltages of up to  $\pm 5V$ , adequate for most bridge transducer type applications. For very high common mode voltages, the opto-isolation technique, used in several Analog Devices' DPMs, allows common mode voltages of up to  $\pm 300V$  and provides 100 to 120dB of common mode rejection, even when BCD data outputs are being used. Any ac powered DPM can be floated on the power supply transformer to provide isolation and CMR, similarly to the opto-isolated DPM, if no BCD outputs or control signals are being used (i.e., in readout-only operation). Further information on DPM input configurations can be found in the section, "DPM Input Types and Their Applications."

#### **Displaying the Data**

Once the input signal is digitized, it is decoded and displayed on a digital readout. Numerous types of displays are available today, but Analog Devices' DPMs use large LED (light emitting diode) displays on all of the latest models. Seven-segment LED displays as large as 0.56 (14.3mm) offer the ultimate in ruggedness, reliability and aesthetic appeal, and challenge Beckman gas discharge displays for size.

Beckman displays and smaller 0.27''(6mm) solid state LEDs are also used by Analog Devices. The large shaped characters of the Beckman display easily read at up to 30 feet (9 meters) away. The neon orange digits can be filtered to provide either an amber or a red display. The smaller LEDs, packaged with counting and decoding logic circuitry, permit the extremely small packaging of the AD2010 and the AD2004.

#### **Producing Digital Outputs**

Since the visual display of a DPM must be in a decimal format, the counters used in DPM conversion circuitry are always binary-coded decimal (BCD) counters. The data-output format depends on the circuit design of the meter: most designs using TTL integrated circuits have parallel BCD data outputs, with all BCD bits available simultaneously. Parallel data is easiest to interface to, since most data peripherals, such as printers and comparators, require parallel data. Parallel data can be latched, and therefore valid, except for the period of several microseconds after each conversion, when it is updated, or unlatched, where the data is valid only between conversions. In either case, a STATUS or DATA READY signal is available to indicate when the data outputs are valid.

DPMs using MOS-LSI (metal-oxide semiconductor, large scale integrated circuits) usually have character serial outputs, where each BCD digit is gated onto a single set of parallel output lines in sequence. This technique is used to reduce the number of pins used on the LSI chip and to simplify data interfacing to the display. Although some data peripherals, such as microprocessors, require character-serial data inputs, for many applications it is necessary to use latches or shift registers to convert the data into a parallel format for interfacing. Most DPMs using LSI have an extra cost option available that provides parallel data outputs.

Digital data outputs from DPMs are generally compatible with DTL or TTL logic systems, but some of the newer DPMs using LSI are only compatible with CMOS logic. The parallel output option with these LSI DPM designs, however, is generally TTL compatible for ease in interfacing.

#### Understanding Performance Specifications

*Resolution, Accuracy, and Stability*—these three specs are very important in the selection of a DPM. Although more digits may mean more resolution, the digits themselves are useless unless the accuracy is sufficient for the digits to have real meaning. Therefore, accuracy and resolution should be comparable.

Besides temperature variations, there are three components of DPM inaccuracy: zero offset error, gain error, and quantization error. In any device using a counter and clock to determine a digital output, there is always a potential  $\pm 1$  count error in the output. This is caused by the timing of the input gate of the counter; when the gate closes asynchronously with the clock, a clock pulse that occurs just as the gate closes may or may not be counted, hence the fixed  $\pm 1$  digit inaccuracy.

Zero level offsets in the analog circuitry cause errors specified as a percentage of full scale reading. These errors can be corrected by a zero calibration potentiometer requiring periodic resetting, or by internal calibration circuits that set the zero level automatically between each reading, assuring no zero level contribution to the error.

Gain variations occur as a function of signal level in the analog circuitry and produce errors which are specified as a percentage of the reading. These are the hardest errors to design out of a DPM circuit, but they can be minimized by component specification and selection. A range potentiometer is used for periodic adjustment of the gain. Gain errors may also be calibrated out in "smart" instruments having an automatic internal calibration facility (e.g. AD2050).

Since all the electronic components used in the design of a DPM have some temperature dependence, one can expect the accuracy of the DPM to be affected by changes in operating temperature. If automatic zero correction circuitry is not used, the zero level may drift with temperature. Variations in the reference voltage circuitry and its associated switches will cause changes in the gain of the DPM, but careful selection and matching of components can minimize this error.

To illustrate these specifications, consider a 3½ digit DPM (1999 counts full scale). The resolution of the unit is the value of one digit, 1 part in 2000 or 0.05% of full scale. If the accuracy is comparable to the resolution (exclusive of digital indecision), the DPM should have a maximum error of  $\pm 0.05\%$   $\pm 1$  digit.

Temperature coefficient specifications for a DPM should be very good to maintain the accuracy. A tempco of only  $50ppm/^{\circ}C (0.005\%/^{\circ}C)$  will produce an additional error of  $\pm 0.05\%$  over a range of only  $\pm 10^{\circ}C$ .

Since each manufacturer tends to use a different method of specifying accuracy and temperature coefficients, specifications must be expressed in common terms to be comparable. For example, one may find specifications for 3½ digit DPMs in the formats shown below ("R" = "of reading"):

Unit 1: max error: ±0.05% R ±1 digit, tempco: ±50ppm(R)/°C

- Unit 2: max error: ±0.02% R ±0.03% F.S. ±1 digit, tempco: ±0.004%R ±0.001% F.S./°C
- Unit 3: max error: ±0.05% R ±0.05% F.S. ±1 digit, for temperature +15°C to +35°C

To compare the three units, one must establish a common ground: full scale reading, temp range  $+15^{\circ}$ C to  $+35^{\circ}$ C ( $\pm 10^{\circ}$ C). The specification then becomes:

Unit 1:  $\pm 0.05\%$  F.S.  $\pm 1$  digit  $\pm (50$ ppm(F.S.)/<sup>°</sup>C x $\pm 10$ <sup>°</sup>C) =  $\pm 0.05\%$  F.S.  $\pm 1$  digit  $\pm 0.05\%$  F.S. = 0.1% F.S.  $\pm 1$  digit

Unit 2: ±(0.02% F.S. ±0.03% F.S.) ±1 digit (0.004% F.S. ±0.001% F.S.)/°C x ±10°C = 0.05% F.S. ±1 digit ±0.05% F.S. = 0.1% F.S. ±1 digit Unit 3: ±0.05% F.S. ±0.05% F.S. ±1 digit

Unit 3:  $\pm 0.05\%$  F.S.  $\pm 0.05\%$  F.S.  $\pm 1$  digit = 0.1% F.S.  $\pm 1$  digit

Even though all units are specified differently, they have equivalent performance.

#### **DEFINITIONS – TERMS & SPECIFICATIONS**

Accuracy (absolute): DPMs are calibrated with respect to a reference voltage which is in turn calibrated to a recognized voltage standard. The absolute accuracy error of the DPM is the tolerance of the full-scale set point referred to the absolute voltage standard.

Accuracy (relative): Relative accuracy error is the difference between the nominal and actual ratios to full scale of the digital output corresponding to a given analog input. See also: linearity.

Automatic Zero: To achieve zero stability, a time interval during each conversion is provided to allow the circuitry to compensate for drift errors, thereby, providing virtually no zero drift error.

Bias Current: The current required from the source at zero signal input by the input circuit of the DPM. Bias current is normally specified at typical and maximum values. Analog Devices' DPMs using transistor input circuitry are bias current sinks.

Binary Coded Decimal (BCD): Data coding where each decimal digit is represented by a group of 4 binary coded digits (called "quads"). Each quad has bits corresponding to 8, 4, 2 and 1 and 10 permissible levels with weights 0-9. BCD is normally used where a decimal display is needed.

Bipolar: A bipolar DPM measures inputs which may be of either positive or negative polarity and automatically displays the polarity as well as the magnitude of the input voltage on the readout.

Character Serial BCD: Multiplexed BCD data outputs, where each digit is gated sequentially onto four common output lines.

Common-Mode Rejection: A differential-input DPM will reject any input signals present at both input terminals simultaneously if they are within the common mode voltage range. Common mode rejection is expressed as a ratio and usually given in dB. (CMR = 20 log CMRR). 120dB of common-mode rejection (CMRR =  $10^6$ ) means that a 10V common-mode voltage is processed as though it were an additive-differential input signal of  $10\mu$ V magnitude.

Common Mode Voltage: A voltage that appears in common at both input terminals of a device, with respect to its ground.

Conversion Rate: The frequency at which readings may be processed by the DPM. Specifications are typically given for internally clocked rates and maximum permissible externallytriggered rates.

Conversion Time: The maximum time required for a DPM to complete a reading cycle, specified for the full scale reading.

Dual-Slope Conversion: An integrating A/D conversion technique in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time.

Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown, until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period.

Input Impedance: The complex ratio of signal voltage to signal current at the input terminals. For dc measuring DPMs, the input is measured at dc. For ac measuring DPMs, it is expressed as a dc resistance shunted by a specified capacitance.

Linearity: The conventional definition for nonlinearity of a DPM is the deviation from a "best" straight line which has been fitted to a calibration curve. Analog Devices defines nonlinearity as the deviation from a straight line drawn between the zero and full scale end points. Not only is this an easier method for customer calibration, it is also a more conservative method of specifying nonlinearity.



Normal Mode Rejection: Filtering or integrating the input signal improves noise rejection of undesired signals present at the analog *higb* input. Normal mode rejection is expressed as the ratio of the actual value of the undesired signal to its measured value over a specified frequency range. (NMR (dB) = 20 log NMRR, e.g. NMR = 40dB means an attenuation of 100:1). Overload: An input voltage exceeding the full scale range of the DPM produces an overload condition. An overload condition is usually indicated by conspicuous manipulation of the display such as all dashes, flashing zeros, etc. On a 3½ digit DPM with a range of 199.9mV, a  $\geq$ 200mV signal will produce an overload condition.

Overrange: An input signal that exceeds all nines on a DPM, but is less than an overload. On a 3½ digit DPM with a full scale range of 199.9mV, the all-nines range is 0-99.9mV, and signals from 100-199.9mV are said to fall in the 100% overrange region. Some DPMs have higher overrange capability. A 3¼ digit DPM has a full scale range of 3.999 or 300% overrange.

Overvoltage Protection: The input section of the DPM must provide protection from large overloads. Specifications are given for sustained dc voltages that can be tolerated.

Parallel BCD: A data output format where all digital outputs are present simultaneously.

Range (Temperature Operating): The range of temperatures over which the DPM will meet or exceed its performance specifications.

Range (Full Scale): The range of input signals that can be measured by a DPM before reaching an overload condition. A 3<sup>1</sup>/<sub>2</sub> digit DPM's full-scale range consists of three digits (allnines range) and 100 percent overrange capability.

Ratiometric: Dual Slope DPMs compare voltage inputs to a stable internal reference voltage. In some systems, the voltage being measured is a function of another voltage, and accurate measurements should be made as the ratio of the two voltages. Some DPMs provide inputs for external reference voltages for ratiometric measurements.

Resolution: The smallest voltage increment that can be measured by a DPM. It is a function of the full scale range and number of digits of a DPM. For example, if a  $3\frac{1}{2}$  digit DPM has a resolution of 1 part in 2000 (0.05%) over a full scale range of 199.9mV, the DPM can resolve 0.1mV.

Digits	Counts (F.S.)	Resolution (% F.S.)
21/2	199	0.5%
3	999	0.1%
31/2	1999	0.05%
33/4	3999	0.025%
4	9999	0.01%
41⁄2	19999	0.005%
4¾	39999	0.0025%

Single Slope Conversion: In the single slope converter, a reference voltage is integrated until the output of the integrator is equal to the input voltage. The time period required for the integrator to go from zero to the level of the input is proportional to the magnitude of the input voltage and is measured by an internal clock. 16



Staircase Conversion: A simple analog-to-digital conversion technique in which a clock and counter drives a digital-toanalog converter which produces an output voltage waveform resembling a staircase. A comparator stops the counter when the voltage exceeds the input voltage; the count achieved by the counter is the digitized output.



Staircase Converter

Temperature Coefficient: The additive error term (ppm/°C or % Reading/°C) caused by effects of variations in operating temperature on the electronic characteristics of the DPM.

Unipolar Input DPM: A DPM designed to measure input voltages of only one polarity.

#### **DPM Input Types And Their Applications**

The four different input configurations used on DPMs (singleended, limited differential, differential, and floating) are made available to solve various applications problems. In OEM applications where the DPM is a dedicated readout for an instrument or system, a single-ended DPM is usually desired for its low cost. But single-ended DPMs require care in application to prevent ground loops from interfering with measurements. The "limited differential" input pioneered by Analog Devices, however, uses a single resistor to isolate analog and digital (and, in logic powered DPMs, the power supply) grounds to effectively eliminate ground loops. This limited differential input allows up to approximately 200 millivolts of common mode voltage and 60dB of common mode rejection without imposing the cost penalties of a true differential or floating input. Thus the majority of DPM applications require only a single-ended or limited differential input DPM.

But if the DPM is measuring the output of a bridge transducer, higher common mode voltages must be accommodated, and differential input DPMs which allow a CMV up to  $\pm 5V$  are usually necessary. Where extremely high common mode voltages are required, such as current measurements, a floating (usually opto-isolated) input DPM can provide for up to  $\pm 300V$ CMV. Either the differential or floating input DPM will also provide greater common mode noise rejection, if necessary.

If digital control signals and BCD data outputs are not needed, any ac line powered DPM can be floated on the power supply transformer to provide high CMV and CMR. But care must be exercised when applied in this fashion at high CMV, since all connections may be floating at dangerously high voltages. All line powered DPMs have a connection for "earth ground" which may be connected to a transformer shield or guard track on the printed circuit board, but this earth ground is usually capacitively coupled to the digital ground for noise rejection. Always insure that the earth ground is not directly connected to digital ground when "floating" a line powered DPM in this manner.



Grounding Configurations of DPMs



# High Performance $4\frac{1}{2}$ Digit DPM For System Applications

# AD2004

#### FEATURES

Floating Optically Isolated Analog Section Excellent Common Mode Rejection: 120dB at ±300V High Normal Mode Rejection: 60dB 5V dc Powered Automatic Zero with Maximum Error: 0.01% ±1 Digit LED Display with Latched Digital Outputs

Small Size: 1.8"H x 3"W x 2.5"D

#### APPLICATIONS

Industrial Weighing Systems Process Control Monitoring Precision Differential Measurement Ground Loop Elimination Off Ground Signal Measurements Analytical and Scientific Instrumentation

#### **GENERAL DESCRIPTION**

Analog Devices' model AD2004 is a 4½ Digit, 5V dc powered digital panel meter offering 0.01%  $\pm 1$  digit accuracy, resolution of 0.1mV, common mode voltage (CMV) of  $\pm 300V$  with a common mode rejection ratio (CMRR) of 120dB.

Using optically coupled isolation techniques for the signal channel, this new design is capable of performing precision measurements of floating differential voltages in noisy environments or under widely varying common mode voltage levels of up to  $\pm 300$ V. The optically isolated design assures ground loop elimination and permits critical measurement of off ground signals such as those found in the nuclear and process control industries.

The AD2004 features a 4½ digit light-emitting-diode (LED) display with a full scale range of 0 to  $\pm 1.9999$  volts and latched digital data outputs and control interface signals. Automatic-zero correction circuitry measures and compensates for offset and offset drift errors thereby providing virtually no zero error.

The conversion rate of the AD2004 is normally 4 readings per second. However, an external trigger may be applied to vary the sampling rates from a maximum of 8 readings per second down to an indefinite hold rate. During conversion, the previous reading is held by the latched logic. The numeric readout is available as BCD data. Application of the metering system in a computer or data logging system is made easy with the availability of the "overrange," "polarity," "overload," and "status" signals.

The AD2004 can operate from the users 5V dc system supply, thereby, eliminating the shielding and decoupling needed for



line powered units when the ac line must be routed near signal leads.

#### TYPICAL APPLICATIONS INCLUDE:

- Ground loop elimination between input transducer and output circuit functions.
- High resolution monitoring of small signals impressed on high off-ground voltages of up to ±300V.
- Electronic indicating weighing systems for industrial applications. Numerical output may be interfaced with a digital computer or data logging system.
- Digitally controlled industrial process where analog and digital signal isolation is required.
- Balanced strain gage bridge output measurement for industrial requirements.
- Digital indicating micrometer using a linear variable differential transformer (LVDT). Due to the high normal mode rejection ratio of the AD2004, the ac excitation of the LVDT does not induce errors into the system.
- Analytic and Scientific Instrument displays with isolated numeric readout.

#### FLOATING DIFFERENTIAL INPUT OFFERS HIGH CMV AND CMR

Figure 1 illustrates the isolation technique used to achieve high CMV and CMR.



Figure 1. Simplified Block Diagram

For detailed information, contact factory.

# SPECIFICATIONS (typical @ +25°C and +5V dc unless otherwise noted)

DISPLAY OUTPUT

- Display consists of five LEDs for data digits plus 100% overrange.
- Overload Four data digits display zeros and flashes when reading exceeds the input range (>1.9999 volts).
- Decimal Points Selectable at input connector.

INPUT

- Full Scale Range 0 to ±1.9999 volts
- Automatic Zero
- Automatic Polarity
- Floating
- Bias Current <1nA max</li>
- Impedance  $> 100 M\Omega$
- Overvoltage Protection ±50V sustained without damage.
- Decimal Points (4) Selectable by Logic "1" or by leaving open. Grounding the input turns decimal points off.

#### ACCURACY (30 Minute Warm-Up)

- 0.01% of Reading ±1 Digit
- Resolution 0.1mV
- Temperature Range 0 to +50°C operating
- Temperature Coefficient  $-\pm 15$  ppm/°C max

#### NORMAL MODE REJECTION

• 60dB without filter @ 50-60Hz minimum

#### COMMON MODE REJECTION

120dB typical dc-1kHz with 1kΩ unbalance

COMMON MODE VOLTAGE (with digital interface signals connected)

• ±300V dc (600V peak to peak)

#### DATA PROCESSING SIGNALS

		114	001
•	DTL/TTL Compatible Logic "0"	<0.8V	<0.4V
	Logic "1"	>2.0V	>2.4V

OUT

IN

Inputs

External Trigger – Operation in the External Trigger mode requires the External Hold input be held at Logic "0" or grounded. A negative going external trigger pulse (Logic "1" or Logic "0" and return) is required to start each conversion. The DPM is reset on the negative transition and a new conversion is triggered on the positive transition. The pulse width must be greater than 100ns. The STATUS signal is set at the negative transition and the actual conversion begins  $0-3.3\mu$ s (maximum of 1 clock pulse) after the positive transition to allow synchronizing conversion with the internal clock.

External Hold – When this input is grounded or held at 0.8V max, the last conversion is held and displayed. For a new conversion under internal control, this input must be open or at Logic "1".

- Output
  - 4BCD Digits (8421 Positive True) Latched 3TTL loads Overrange – Logic "1" indicates an overrange – Latched – 9TTL loads
  - Overload Logic "1" indicates the input has exceeded the input range – Latched – 9TTL loads
  - Status Signal Logic "0" indicates conversion is complete – 9TTL loads

Polarity – Logic "1" with positive polarity input – Latched – 7TTL loads

#### CONVERSION TIME

• 125ms for Full Scale Input (145ms for AD2004/E)

#### SPEED

- External Trigger 8 conversions per second (6 conversions per second for AD2004/E)
- Internal Conversion 4 conversions per second
- Hold and Read on Command

#### SIZE AND WEIGHT

3"W x 1.8"H x 2.5"D (7.62 x 4.57 x 6.35cm) (overall depth for case and connector is 3.3" (8.38cm)). Weight, 8 oz. (227 gm).

#### POWER

5V dc ±5% @ 800mA typ, 900mA max

#### ORDERING GUIDE

- AD2004 Standard AD2004 as described above tuned for peak normal mode rejection at 60Hz and its harmonics.
- AD2004/E Standard AD2004 as described above – tuned for peak normal mode rejection at 50Hz and its harmonics.

#### CONNECTOR

 AC1600 6 feet of decade coded wire mated with "3M" Connector (Part No. 3414)

AC1601 "3M" mating connector (Part No. 3414) only NOTE

Specifications subject to change without notice.

NOTE:



1. Maximum Delay of One

to Synchronize with

2. AD2004E (50Hz Model) Timing.

Ramp up 40ms

Ramp down 80ms

Zero correct 25ms

6ms

Figure 2. AD2004 Timing Diagram

Maximum Trigger Rate

Clock Pulse 3.3µs

Clock



# AC Powered 3½ Digit DPM with Sperry Display AD2006

#### FEATURES

AC Line Powered (+5V dc Powered Optional) 0.55" Sperry Display Differential Input Maximum Error: ±0.05%±1 Digit AC Terminal Strip for Safety Ratiometric Operation Power Outputs for External Circuitry

#### APPLICATIONS

Analytical, Medical and Scientific Instrumentation Industrial Test Equipment Process Control Instrumentation



In addition to ac line powered versions, the AD2006/D is available for operation from +5V dc power supplies commonly used for digital logic circuitry. The AD2006/D has identical performance specifications to all other AD2006 versions, except that it cannot be floated on the power supply for measurements at high common mode voltages and, of course, the +5V dc output is not available.

#### LARGE CLEAR DISPLAY ENHANCES READABILITY

The AD2006 uses large (0.55'') Sperry, seven-segment, planar gas-discharge displays which appear as continuous solid digits. The display size, brightness and contrast ratio makes the AD2006 readable at distances up to 40 feet or more and in any ambient lighting condition including bright sunlight. The display is filtered to provide bright red digits and is readable without distortion over a 130° viewing angle. Overload conditions are indicated by displaying all dashes with the polarity sign remaining valid. The polarity sign can be blanked for display in engineering units where polarity indication is unnecessary.

#### **GENERAL DESCRIPTION**

Analog Devices' model AD2006 is an ac line-powered, 3<sup>1</sup>/<sub>2</sub> digit panel meter with Sperry displays for high visibility. The design of the AD2006 includes ratiometric operation and external power outputs to increase its application versatility.

The AD2006 provides high accuracy measurements of bipolar, differential input signals over a full scale range of  $\pm 1.999V$ , with a maximum error of  $\pm 0.05\%$  (reading)  $\pm 1$  digit. For most applications, the differential input section provides greater than 70dB of common mode rejection (CMRR) at common mode voltages (CMV) up to  $\pm 5V$ . In addition, the AD2006 can be floated on the ac power supply in the singleended mode, allowing common mode rejection exceeding 100dB. To insure the safety of operational personnel and interconnected equipment, especially at high CMV, a terminal strip is provided for connection of ac power.

For best visual readout, the AD2006 is internally programmed to make 5 readings per second. For data acquisition applications, up to 90 conversions per second can be externally triggered. DTL/TTL compatible parallel BCD data outputs and control signals are provided for interfacing to other digital data systems. To extend its versatility, external power outputs suitable for powering op amps and IC circuits are available to facilitate scaling or buffering inputs and driving external logic. Standard ratiometric operation allows normalizing inputs to an external reference voltage for making compensated measurements with bridge and potentiometric transducers.

# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

#### DISPLAY OUTPUT

- Sperry Gas Discharge displays (seven segment, 0.55" (1.4cm)H), for 3 data digits, 100% overrange and polarity indication.
- Overload: Center segment dashes, polarity remains valid.
- Decimal Points: Selectable at input connector (contact closure).
- Polarity Sign may be blanked for display in engineering units.

#### INPUT

- Full Scale Range: 0 ±1.999V
- Automatic Polarity
- Differential
- Bias Current: High Input 3nA typ. (7nA maximum)
- Low Input 200nA typ. (500nA maximum) Impedance: >100MΩ
- Overvoltage Protection: Analog Hi = ±50V sustained Analog Low = ±30V sustained

#### EXTERNAL REFERENCE INPUT

- Range: +5.8 to +6.8 Volts
- Input Impedance: >0.5MΩ
- Not protected against overvoltage
- Absolute Value Measurements: Internal +6.4V reference must be externally connected to the reference input.

#### ACCURACY

- Maximum Error: 0.05% of reading ±1 digit
- Resolution: 1mV
- Temperature Range: 0 to +50°C operating, -55°C to +85°C storage.
   Temperature Coefficient: Gain: <50ppm/°C</li>
  - Zero: <±50µV/°C
- COMMON MODE REJECTION
  - Differential Mode: 70dB, dc to 1kHz, with 1kΩ unbalance Floated on power supply transformer: >100dB<sup>1</sup>

COMMON MODE VOLTAGE

- Differential Mode: ±5V
- Floating Mode: ±300V dc (600V p-p ac)<sup>1</sup>

#### SPEED

- External Trigger: Up to 90 conversions per second (without display)
- Internal Trigger: 5 conversions per second
- Hold and Read on Command

#### CONVERSION TIME

- Normal Conversion: 9ms maximum
- Overload Conversion: 11ms maximum

#### INTERFACE SIGNALS

DTL/TTL Compatible

	IN	OUT
logic "0"	<0.8V	<0.4V
logic "1"	>2.0V	>2.4V

Inputs

Polarity Sign Blanking: Logic "0" or grounding blanks the polarity sign being displayed.

External Hold: Logic "0" or grounding this input disables the internal trigger, and the last conversion is held and displayed. External triggering can only be done when the AD2006 is in "HOLD".

External Trigger: A negative trigger pulse applied to the external trigger input will initiate conversion.

Outputs

Status: All digital outputs are valid when status is low (logic "0"), logic "1" indicates conversion is in process. 3BCD Digits (8421 positive true), unlatched, 6TTL loads. Overrange: Logic "1", unlatched, 6TTL loads, indicates overrange (>1.000V).

Overload: Logic "1" unlatched, 6TTL loads, indicates overload (>1.999V), logic "0" indicates data is valid. Polarity: Logic "1", latched, 6TTL loads, indicates postive polarity.

Polarity: Logic "1", latched, 6TTL loads indicates negative polarity.

#### POWER

- AC line power (see option table), 7 Watts at nominal line voltage.
- AD2006/D: +5V dc @ 850mA
- WARMUP
  - 20 minutes to specified accuracy.
- ADJUSTMENTS
  - (recommended calibration period: 6 months)
  - Gain Zero Offset
- EXTERNALLY AVAILABLE POWER OUTPUTS
  - +5V ±5% 
     50mA (continuous short circuit protection)<sup>1</sup>
  - ±15V ±10% @ 10mA (No short circuit protection; may require filtering for power supply-sensitive components)

SIZE

3"W x 1.8"H x 4"D (7.62 x 4.57 x 10.16cm) (4.95" (12.57cm) max to rear of mating connector, 4.80(12.19cm) max on AD2006/C)

WEIGHT

• P

- 19 oz. (540gm) with ac power
- 10½ oz. (300gm) on AD2006/D

**OPTIONAL FEATURES & ORDERING GUIDE** (All options on any AD2006 are listed on the label affixed to the bottom of the unit.)

ower Supply Inputs (	only one may be spec	cified)
AD2006	115V ac ±10%	)
AD2006/E	220V ac ±10%	(50 - 604-)
AD2006/H	240V ac ±10%	( (30 - 00H2)
AD2006/F	100V ac ±10%	,
AD2006/D	+5V dc ±5%	

- Card Edge Connector: AD2006/C
- Any combination of the above options excluding power inputs -- can be specified. When ordering, specify power supply option first, then the other option desired. For example, an AD2006/E/C operates on 220V ac, and has the connector card edge.
- Display Lenses (only one may be specified):
  - Lens-5 will be supplied if none is specified)
    - Lens-5 Red w/ADI Logo
    - Lens-6 Red no ADI Logo
    - Lens-9 Amber w/ADI Logo
    - Lens-10 Amber no ADI Logo

CONNECTOR

- M connector #3414, (optional) AC1600-34 pin connector and 6 ft. (1.83m) of color-coded, 34 way, 28 AWG flat woven cable.
- AC1601-connector only.
- AD2006/C requires 30 pin, 0.156 spacing, Viking No. 2VK 15D/1-2 or Cinch type 251 No. 5030A30.
- AD2006/C optional Order AC1501.
- AC Power Line Cords are not supplied by ADI.

#### NOTES

<sup>1</sup>Not applicable to AD2006/D,

<sup>a</sup>Not applicable to AD2006/C.

Specifications subject to change without notice.

### Applying the AD2006

#### **RATIOMETRIC OPERATION EXTENDS APPLICATIONS**

The AD2006 has provision for making measurements normalized to an external reference voltage. This feature allows compensation for transducer outputs sensitive to excitation voltage variations, by making all measurements with reference to the excitation voltage. Figure 1 shows the AD2006 used with a bridge transducer which may be measuring temperature, pressure or any other physical parameter. The excitation voltage of the transducer is used as the reference input of the DPM. When used in the ratiometric mode, reference inputs in the range of +5.8 to 6.8 volts must be presented to the REFERENCE INPUT. The reference input must be relatively stable since the

DPM measures	$\int_{t} E_{in} dt$	not	ſ	$\frac{E_{in}}{E_{in}}$ dt, and any variations
	∫ <sub>t</sub> E <sub>ref</sub> dt →		$J_{t}$	<sup>L</sup> ref

in the reference voltage during conversion may produce erroneous readings.



### Figure 1. Bridge Transducer Measurements Using the AD2006's Ratiometric Input

The REFERENCE OUTPUT can be used for driving transducers if it is properly buffered using an external op amp. Figure 2 shows a thermistor temperature measuring circuit using the AD2006 to power the entire measurement system. The REFERENCE INPUT is a high impedence input which will not load any reference source, but this input is not protected from overload damage. If normal operation of a AD2006 is required, connection of the Reference Output to the Reference Input will allow operation using the internal +6.4V reference source.



Figure 2. AD2006 Thermistor Temperature Measurement System

DC OUTPUTS CAN POWER EXTERNAL CIRCUITRY

Since the circuitry of the AD2006 requires  $\pm 15V$  and  $\pm 5V$  to be generated internally, these voltages are made available to allow operation of external circuitry used in conjunction with the DPM. Sufficient power is available to drive op amps to scale inputs or even buffer the reference output to drive transducers such as in the thermistor application shown in Figure 2. The  $\pm 5V$  output (not available on AD2006/D models) can be used for external logic. In many measurement systems, these power outputs will be sufficient to power all the circuitry external to the DPM. Although the regulation and ripple are adequate for the sensitive analog and digital circuitry of the AD2006, further filtering may be necessary for components that are extremely power supply sensitive.

#### **AD2006 THEORY OF OPERATION**

Figures 3 and 4 are the block diagram and timing diagram for the AD2006. The AD2006 uses a standard dual slope conversion technique with an absolute value voltage to current converter on the input. The absolute value of the analog input voltage produces a proportional current. When the convert command pulse initiates conversion, this current is integrated "up" for a fixed time period (1000 clock periods). The con-

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Figure 3. AD2006 Block Diagram

verter then integrates "down" using a reference current of opposite polarity until the comparator senses that the integrator output voltage has returned to the original baseline. During the ramp-down period, the counters count clock pulses, and the number stored at the end of ramp-down is proportional to the analog input voltage.



Figure 4. AD2006 Timing Diagram

#### **INTERFACING THE AD2006**

<u>AC POWER CONNECTIONS</u>: Connect ac power lines to the terminal strip on the rear of the AD2006. The ground line is internally connected to the case of the DPM. To assure safe operation, always use three-wire ac only, and cover the terminal strip with the protective cover provided. AD2006/D versions use the +5V dc Output and the Digital Ground as power supply <u>INPUTS</u>.

INPUT CONNECTIONS: Differential input signals should be connected between the ANALOG HI and the ANALOG LOW. The ANALOG GROUND must be connected to the system ground. For single-ended operation, connect the ANALOG LOW to the ANALOG GROUND. To allow operation at high common mode voltage, the AD2006 may be floated on the ac power supply transformer in the single-ended mode, without the digital interface signals connected. (See note on decimal points. AD2006/D versions can only be operated in the differential mode.) For absolute value measurements, the REFERENCE OUTPUT must be connected to the REFER-ENCE INPUT.

**DECIMAL POINTS:** Grounding the appropriate pin will illuminate the desired decimal point. (Note: Decimal points can be used in the "floating" mode if and only if the appropriate pin is grounded only to the AD2006 digital ground.

DIGITAL DATA OUTPUTS: The digital data outputs are unlatched, positive true, parallel BCD, at DTL/TTL logic levels. All data outputs are valid when the STATUS line is low (logic "0"). Erroneous data will be present when the conversion is in process and the STATUS line is high.

#### EXTERNAL CONTROL SIGNALS:

EXTERNAL HOLD: Logic "0" or grounding the HOLD input disables the internal trigger, and the last conversion is held and displayed. If a HOLD input is applied during conversion, the conversion will be completed and displayed. No further conversions will be made unless the HOLD input is removed or an EXTERNAL TRIGGER pulse is applied.

EXTERNAL TRIGGER: Operating in the EXTERNAL TRIGGER mode requires that the HOLD line be held at logic "0" or grounded. A negative going trigger pulse (logic "1" to logic "0" and return) of 1 $\mu$ s minimum and 1ms maximum width applied to the trigger input will initiate a conversion. The external trigger input must be a pulse since the STATUS is set on the negative-going edge of the pulse and the conversion is initiated on the positive-going edge of the pulse. Triggering at high rates asynchronously with line frequency may cause modulation of the display brightness, since the display is blanked both during conversion and during the negative half of the line cycle. Care should be taken to insure that triggering does not occur during conversion, as this will cause an erromeous conversion.

**POLARITY SIGN:** A logic "0" or ground blanks the polarity sign being displayed.

#### CALIBRATION PROCEDURES

WARNING: For the safety of personnel and interconnected equipment, all calibration should be done using a PLASTIC TRIMMING TOOL ONLY.

The accuracy of the AD2006 should be checked approximately every six months. A precision voltage reference or a calibrated DVM or DMM and a stable voltage source are required. The location of the adjustment potentiometers are shown on the mechanical layout drawings. Under most circumstances, only the gain will need adjustment. Should zero adjustment be necessary, adjust the zero before adjusting the gain.

ZERO OFFSET: Apply an input of 0V or short the analog inputs. If the meter does not read zero, adjust the zero offset pot until the meter reads zero and the polarity sign periodically changes. (Turning the pot clockwise, viewed from the back, makes the reading more negative.)

GAIN: Set the input of the panel meter to 1.900V. The input can be from a precision reference source, or from a stable voltage source set using a calibrated DVM or DMM. If the meter does not read 1900, adjust the gain pot to set the proper reading. (Turning the pot clockwise will increase the reading.) This is a bipolar adjustment, when correctly adjusted, the meter will read correctly for both polarities.



# Low Cost 3½ Digit DPM For OEM Applications

AD2010

#### FEATURES

LED Display with Latched Digital Outputs Small Size, Lightweight Automatic Zero Correction; Max Error: 0.05% ±1 Digit High Normal Mode Rejection: 40dB @ 50 or 60Hz Optional Ratiometric Operation Leading "0" Display Blanking 5V dc Powered

#### APPLICATIONS

Medical/Scientific/Analytic Instruments Data Acquisition Systems Industrial Weighing Systems Readouts in Engineering Units Digital Thermometers

#### GENERAL DESCRIPTION

Analog Devices' model AD2010 represents an advance in price/ performance capabilities of  $3\frac{1}{2}$  digit digital panel meters. The AD2010 offers  $0.05\% \pm 1$  digit maximum error with bipolar, single ended input, resolution of  $100\mu$ V, and a common mode rejection ratio of 60dB (CMRR) at  $\pm 200$ mV (CMV).

The AD2010 features a light-emitting-diode (LED) display with a full scale range of 0 to  $\pm 199.9$  millivolts, latched digital data outputs and control interface signals, and leading zero display blanking. Automatic-zero correction circuitry measures and compensates for offset and offset drift errors, thereby providing virtually no error. Another useful feature of the AD2010 is its 5V dc operation. The AD2010 can operate from the users' 5V dc system supply, thereby eliminating the shielding and decoupling needed for line powered units when the ac line must be routed near signal leads.

To satisfy most application requirements, the conversion rate of the AD2010 is normally 4 readings per second. However, an external trigger may be applied to vary the sampling rates from a maximum of 24 readings per second down to an indefinite hold time. The AD2010 can also be connected for automatic conversion at its maximum conversion rate. During conversion, the previous reading is held by the latched logic. The numeric readout is available as BCD data. Application of the metering system in a computer or data logging system is made easy with the availability of the "overrange," "polarity," "overload," and "status" signals.

The AD2010/R option for ratiometric operation allows readings to be made of the ratio of two input voltages as well as the absolute value of the input. AD2010/R operation is described in a later section.



A simplified block diagram of the AD2010, illustrating the features described above is shown in Figure 1.



#### Figure 1. Simplified Block Diagram

### IMPROVED NOISE IMMUNITY, ACCURACY AND ZERO STABILITY

Dual-slope integration, as used in the AD2010 and as described in the theory of operation section, offers several design benefits.

- Conversion accuracy, for example, is independent of both the timing capacitor value and the clock frequency, since they affect both the up ramp and down ramp integration in the same ratio.
- Normal mode noise at line frequencies or its harmonics is rejected since the average value of this noise is zero over the integration period.
- To achieve zero stability, a time interval during each conversion is provided to allow the automatic-zero correction circuitry to measure and compensate for offset and offset drift errors, thereby, providing virtually no zero error.

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# SPECIFICATIONS (typical @ +25°C and +5VDC unless otherwise noted)

#### DISPLAY OUTPUT

- Display consists of four LED's (7 segment 0.27" (6.9mm) high). for data digits plus 100% overrange and polarity indication.
- Overload three data digits display zeros and flashes.
- Decimal Points selectable at input connector.
- Leading "0" Display Blanking controlled externally.

#### INPUT

- Full Scale Range 0 to ±199.9 millivolts
- Automatic Zero
- Automatic Polarity
- Bias Current 3nA
- DC Impedance 100MΩ
- Overvoltage Protection 20V sustained, 50V momentary without damage.
- Decimal Points (3) illuminate with logic "1", extinguish with logic "0".

#### ACCURACY

- Maximum Error 0.05% of reading ±1 digit
- Resolution 0.1 millivolt
- Temperature Range 0 to +50°C operating -30°C to +85°C storage
- Temperature Coefficient ±50ppm/°C
- NORMAL MODE REJECTION

• 40dB @ 60Hz (50Hz on AD2010/E)

#### COMMON MODE REJECTION • 60dB @ ±200mV

#### CONVERSION RATE

- External Trigger up to 24 conversions per second
- Internal Trigger 4 conversions per second
- Automatic A new conversion is initiated automatically upon completion of conversion in process; conversion rate will vary from 24/sec to 40/sec depending on input magnitude.
- Hold and Read upon command.

#### CONVERSION TIME

- Normal Conversion 42ms max (full scale input) 50ms max Model AD2010/E
- Overload Conversion 62ms max
- INTERFACE SIGNALS

٠	DTL/TTL Compatible		IN	OUT
	-	logic "0"	<0.8V	<0.4V
		logic "1"	>2.0V	>2.4V

Inputs

External Trigger – Operation in the "External Trigger" mode requires that the "External Hold" input be a logic "0" or ground.

Negative Trigger Pulses – Applying a logical "low" to the "HOLD" input disables the internal trigger. A negative trigger pulse (logic "1" to logic "0") of 1.0µs minimum applied to the "EXT TRIGGER" input will initiate conversion in the same manner as the internal oscillator. The external trigger should not be repeated, however, until the "status" indicates completion of the conversion in process.

Positive Trigger Pulses – The "HOLD" input can be used to trigger the AD2010 from a "normally low" signal with the "EXT TRIGGER" input open or logic "1". Following a "hold" a new reading will be initiated on the leading edge of the "hold" signal. Thus, a momentary positive pulse on the "HOLD" input can be used to trigger the AD2010. The drift correct interval, however, begins on the trailing edge of the positive pulse, so if the pulse width exceeds 1 ms, the conversion will actually be initiated by the internal trigger.

Specifications subject to change without notice.

Maximum Conversion Rate - Automatic – The AD2010 can also be connected for automatic conversion at its maximum conversion rate by connecting the "status" output back into the "hold" input. In this manner the status signal going high at the end of one conversion immediately initiates a new conversion. The pulses appearing on the status line can be used to step a multiplexer directly, since the built-in drift-correct delay of 8.33ms will allow settling of the input prior to conversion. A logic "O" applied to the "EXT TRIGGER" will inhibit the automatic trigger mode.

External Hold – Logic "0" or ground applied to this input disables the internal trigger and the last conversion is held and displayed. For a new conversion under internal control the input must be opened or at logic "1". For a new conversion under external control, a positive pulse of less than 1.0ms can be applied (as previously explained).

#### OUTPUTS

- 3 BCD Digits (8421 Positive True) latched 3TTL loads
- Overrange logic "1" latched 6TTL loads, indicates overrange.
- Overload logic "0" indicates overload (>199.9mV) logic "1" - latched - 6TTL loads, indicates data valid.
- Polarity logic "1" latched 6TTL loads, indicates positive polarity input.
- Status logic "0" conversion in process logic "1" - latched - 6TTL loads, indicates conversion complete.

#### POWER

• +5V dc ±5%, 500mA

#### WARM UP

• Essentially none to specified accuracy

#### ADJUSTMENTS

- Range potentiometer for full scale calibration. Calibration recommended every six months.
- Normal Mode Rejection potentiometer (AD2010R only) SIZE
  - 3"W x 1.8"H x 0.84"D (76.2 x 45.7 x 21.3mm) (overall depth for case and printed circuit board extension is 1.40" (35.6mm)).

#### ORDERING GUIDE

- AD2010 Standard AD2010 as described above tuned for peak normal mode rejection at 60Hz and its harmonics.
- AD2010/E Standard AD2010 as described above tuned for peak normal mode rejection at 50Hz and its harmonics.
- AD2010/R Standard AD2010 as described above with Ratiometric option.
- AD2010/E/R Standard AD2010/E as described above with Ratiometric option.

#### WEIGHT

• 4 oz. (113.5gm)

CONNECTOR RECOMMENDATION

- 30 Pin 0.156 spacing, Viking No. 2Vk 15D/1-2 or Cinch type 251 No. 5030A30.
- Optional Order AC1501.

### Applying the AD2010

#### 5V dc OPERATION PROVIDES REDUCED NOISE PICKUP, IMPROVES RELIABILITY

A DPM designed for 5V dc operation offers the user many advantages over ac line powered devices. These benefits include:

- <u>REDUCED NOISE PICKUP AND SUSCEPTIBILITY</u>. Since line voltages are not required for operation, signal leads and internal circuitry need not be exposed to this source of noise, thereby, reducing power-frequency interference. A separate 5V dc power supply also provides additional isolation from line transients. Shielding and decoupling of the DPM circuits can also be eliminated. The DPM may be used as a component without danger of shock hazards to operational personnel or nearby circuitry.
- <u>IMPROVED RELIABILITY</u>. DPMs without power supplies generally require less space and generate less heat. The result is improved reliability while achieving lower cost. The smaller package size provides greater packaging flexibility and requires less ventilation behind the panel.

#### LEDs GIVE LONG LIFE, SHARP DISPLAY

The numeric outputs are displayed using 0.27'' high, 7 segment, red LEDs. The LEDs provide the physical ruggedness typical of ICs, with a life expectancy in excess of 100,000 hours. The displayed numerals are sharp and easily readable at distances of up to 8 feet. The clean uncluttered look of the lens and case design further enhance the visual attractiveness of the display.

Optical features of the display include: a minimum photometric brightness of 200 foot-lamberts, and a 6300 angstrom, wavelength at peak emission (red). Other display features include programmable decimal points, automatic zero, 4 readings per second display rate, external trigger-and-hold rate of up to 24 readings per second, flashing-zeros overload indication, and leading "zero" display blanking.

### COMPACT DESIGN FEATURES EASY SNAP-IN INSTALLATION

The AD2010 is housed in an aluminum case providing light weight, structural strength, optimum heat dissipation and shielding against external noise. With overall dimensions as shown in Figure 6, minimum space is required both on the panel and behind it. No tools are required for installation. You simply snap in the case, then snap on the filter and lens. Its light weight makes AD2010 ideal for applications in hinged panel equipment.

#### THEORY OF OPERATION

The AD2010 (Timing Diagram Figure 7) uses a dual-slope integrating A/D conversion scheme. When an input signal is applied to the DPM, it is applied to an integrator at the same time a counter is activated, initiating the count of clock pulses. After a predetermined number of counts (a fixed interval of time, T), the polarity of the input signal is strobed and a reference voltage having opposite polarity is applied to the integrator. At this instant, the accumulated charge on the integrating capacitor, C, is proportional to the average value of the input over the interval T. The integral of the reference is an opposite-going ramp having the fixed slop V<sub>REF</sub>/RC. At the same time, the counter is again counting from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to  $V_{IN}T$ , and the equal amount of charge lost is proportional to  $V_{REF}/\Delta t$ , then the number of counts relative to the full count is proportional to  $\Delta t/T$ , or  $V_{IN}/V_{REF}$ . The output of the counter is a BCD number, which is decoded and displayed as the digital representation of the input.

#### AD2010/R OPTION EXPANDS APPLICATION

RATIOMETRIC OPERATION WITH EXTERNAL REFER-ENCE: The ratiometric option (AD2010/R) allows readings to be normalized to an external reference. This option can be useful where the analog voltage to be measured is accurate relative to an external reference which in itself is not accurate. A ratiometric application is illustrated in Figure 2. In this example, a position readout potentiometer operates with an external excitation supply which itself may not be very accurate. However, the potentiometer output relative to the reference supply, will be accurate due to the potentiometric configuration.



#### Figure 2. Ratiometric Operation

In the AD2010 the normal reference voltage is 200mV and is internally connected. The AD2010/R, however, has a "Reference Input" where an external reference voltage in the range of 100-300mV can be applied. The displayed output is given by:

Display = 
$$2000 \left( \frac{E_{IN}}{E_{REF}} \right)$$

The AD2010 also has a "Reference Output" where the normal 200mV reference is available. Absolute measurements using the AD2010/R can be made by externally connecting "Reference Output" to "Reference Input." The "Reference Output" is provided for this purpose only. It should be noted that the ratiometric option is intended only for normalization, and that the external reference must be a steady dc voltage.

#### INTERFACING THE DPM

The AD2010 can also be connected for automatic conversion at its maximum conversion rate by connecting the "status" output (Pin K) back into the "hold" input (Pin D). The 70ns pulses appearing on the status output line may be used to step a multiplexer. The status pulse width may be increased (if desired) as shown in Figure 3.



Figure 3. Increasing Pulse Width for Multiplexer Control in the Automatic Mode

To maximize the common mode rejection, an external 100µF @ 3V capacitor, C, is recommended as illustrated in Figure 4. The capacitor will reduce ground noise and ripple where the interconnection wires are 12 inches or longer. The polarization of C will depend on actual configuration.



Figure 4. Insuring Maximum Common Mode Voltage Rejection

The latched digital data outputs and control interface signals are available at the rear of the AD2010. The signals may be interfaced with the system using a Cinch or Viking PC edge connector with 0.156" spacing or the AC1501 connector option. Signal and pin designations are shown in Figure 5.

PIN REF	PIN FUNCTION	PIN REF	PIN FUNCTION
1	EXTERNAL TRIGGER	А	1000's DIGIT (OVERRANGE)
2	800's DIGIT	В	100's DIGIT
= KEY - 3	400's DIGIT	с	200's DIGIT
4	DP 1XX.X	D	HOLD
5	OVERLOAD	E	POLARITY
6	40's DIGIT	F	80's DIGIT
7	20's DIGIT	н	10's DIGIT
8	DIGITAL GRD	J	POWER SUPPLY GND
9*	REF IN (2010/R ONLY)	к	STATUS
10	REF OUT	L	8's DIGIT
11	CLOCK OUT	м	1's DIGIT
12	4's DIGIT	N	+5V POWER INPUT
13	ANALOG IN	Р	2's DIGIT
14	ANALOG GRD	R	LEADING ZERO SUPPRESSION
15	DP 1X.XX	s	DP 1.XXX

\*WHEN IT IS DESIRED TO USE THE AD2010/R INTERNAL 200mV REFERENCE, EXTERNALLY CONNECT PIN "9" TO PIN "10". "REF IN" NOT PROTECTED AGAINST OVERLOAD.





Figure 6. Overall Dimensions All dimensions are given in inches and (mm).

#### NORMAL CONVERSION



#### **OVERLOAD CYCLE**



(PREVIOUS READING IN RANGE - DATA VALID)

NOTES:

0

- 1.
- The internal trigger rate is 4 conversions/sec. A logic "0" applied to the "HOLD" input (pin D) 2. disables the internal trigger. A positive pulse of 1ms max will initiate conversion. The "status" output may be used in this way for automatic triggering.
- 3. With the internal trigger disabled a negative pulse applied to the "external trigger" (pin 1) will initiate conversion.
- 4. Total ramp down time dependent on extent of overload (additional 20ms max).

Figure 7. AD2010 Timing Diagram

### **ANALOG** DEVICES

# Low Cost, 3½ Digit, Line Powered DPM With LED Display

AD2016

#### FEATURES

"Second Generation" MOS/LSI Design Large 0.5" (13mm) LED Displays AC Line Powered, Universal Transformer ±199.9mV dc, ±1.999V dc or ±19.99V dc Full Scale Ranges Auto-Zero Correction Limited Differential Input Character Serial Data Output Standard, Parallel Data Optional Industry Standard Case Design — Second Sources Available

#### APPLICATIONS

**General Purpose ac Line Powered DPM Requirements** 



GENERAL DESCRIPTION

The AD2016 is a low cost, 3<sup>1</sup>/<sub>2</sub> digit, line powered Digital Panel Meter with large LED displays, designed for general purpose DPM applications. The AD2016 measures bipolar input voltages over full scale ranges of  $\pm 199.9$ mV dc,  $\pm 1.999$ V dc or  $\pm 19.99$ V dc with an accuracy of  $\pm 0.05\%$  reading  $\pm 0.025\%$  full scale,  $\pm 1$  digit. By using the "limited differential" input first used on Analog Devices' AD2010, the AD2016 input prevents ground loop problems and provides common mode noise rejection at common mode voltages up to  $\pm 200$ mV. Normal mode rejection is 40-45dB at 50 to 60Hz.

AD2016 models are available for operation at any line voltage and frequency required throughout the world. But, since the AD2016 uses a "universal" transformer, simple internal changes by bridging solder pads allow easy changing of the input power voltage for specific requirements. Thus, the OEM need not stock a variety of models for export requirements, but can easily change the voltage as required.

#### THE BENEFITS OF SECOND GENERATION DESIGN

The AD2016 is designed around MOS/LSI (Metal Oxide Semiconductor, Large Scale Integration) integrated circuits to reduce the number of components and power consumption, which greatly enhances reliability. However, these ICs provide the performance and features of earlier DPM design. The large 0.5 inch (13mm) LED displays provide the visual appeal of the gas discharge displays with the reliability of all solid state devices.

#### VERSATILE DATA INTERFACING

Since the AD2016 is designed around MOS/LSI circuits, the BCD output data is presented in a bit parallel, character serial format compatible to CMOS logic systems. Although some applications, such as interfacing with microprocessors are simplified with this data format, many applications involving line printers or comparators require parallel data outputs. For these applications, the AD2016/B provides parallel BCD data, TTL compatible. The conversion from a serial to a parallel format is done using shift registers, so the output data is fully latched. The AD2016/B also has two "Hold" inputs, one which stops DPM conversions and one which prevents data updating. Thus, the data outputs can be held for data transfer while the DPM continues to convert and update the display.

#### STANDARD PACKAGING/SECOND SOURCES

The AD2016 is packaged in Analog Devices' ac line powered DPM case, which requires the same panel cutout as cases used by most other manufacturers of ac line powered DPMs. In addition, the pin connections are the same as several other DPMs, including the Analog Devices' AD2009. (Even the BCD outputs of the AD2016/B are the same as the AD2009). With this commonality between DPMs, the user is assured of having second sources available or can update instrument or system designs to utilize the newer technology of the AD2016 without expensive mechanical or electrical changes to current products.

#### DESIGNED AND BUILT FOR RELIABILITY

Even beyond the reliability advantages of the LSI IC design and LED displays, the AD2016 has had extreme care taken in its design and manufacture to insure reliability. Manufacturing processes are monitored by continual quality assurance inspections to insure proper workmanship and testing. Automatic test equipment is used to test each DPM at board level and final assembly to assure thorough testing without error. And, each AD2016 gets one full week of failure-free burn-in at 50°C and with cycled power before shipment.

# SPECIFICATIONS (typical at +25°C and nominal power supply voltage)

#### DISPLAY OUTPUT

- Light-emitting diode (LED), planar seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and negative polarity indication. Overload indicated by flashing display, polarity remains valid.
- Decimal points (3) selectable at input connector.
- Display Blanking

ANALOG INPUT

- Configuration: bipolar, limited differential
- Full Scale Ranges: ±1.999V dc (standard), ±199mV dc ("S" option) or ±19.99V dc ("V" option)
- Automatic Polarity
- Auto Zero .
- Input Impedance:  $100M\Omega$  ( $1M\Omega "V"$  option)
- Bias Current: 50pA
- Overvoltage Protection: ±200V dc sustained

#### ACCURACY

- ±0.05% reading ±0.025% full scale ±1 digit<sup>1</sup>
- Resolution: 1mV (standard), 100µV ("S" option), 10mV ("V" option)
- Temperature Range<sup>2</sup>: 0 to +50°C operating, -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C Zero: Auto Zero
- · Warm Up Time to Rated Accuracy: less than one minute Settling Time to Rated Accuracy: 0.5 seconds (-full scale
- to +full scale)

#### NORMAL MODE REJECTION

45dB at 50-60Hz (40dB, "V" option)

#### COMMON MODE REJECTION

Input Range	Limited Differential (dc-10kHz, no imbalance)	Floating <sup>*</sup> (dc-100Hz, 1kΩ imbalance)
±199.9mV	50dB	120dB
±1.999V ±19.99V	35dB 15dB	120dB 100dB

COMMON MODE VOLTAGE

- Limited Differential Mode: ±200mV
- Floated On Power Supply Transformer When No BCD Outputs or Control Signals are Used: ±300V dc or 600V ac p-p

#### CONVERSION RATE

- 5 conversions per second
- · Hold and read on command

#### CONTROL INPUTS<sup>3</sup>

Display Blanking (TTL/DTL Compatible, 3 TTL Loads) Logic "0" or grounding blanks the entire display except for the decimal points at the tens and hundreds digits. Logic "1" or open circuit for normal operation. Display blanking has no effect on the output data and the display is valid immediately upon removal of a blanking input.

Converter Hold (CMOS, TTL/DTL Compatible, 1 LPTTL Load)

Logic "0" or grounding causes the DPM to cease conversions and display the data from the last conversion. Logic "1" or open circuit for normal operation. After a "Converter Hold" is removed, one or two conversions are needed before the reading or BCD data is valid.

#### Decimal Points (Not TTL Compatible)

Grounding or Logic "0" will illuminate the desired decimal point. External drive circuitry must sink 50mA at a 25% duty cycle when a decimal point is illuminated.

Data Hold (AD2016/B Only) (TTL/DTL Compatible, 1 TTL Load)

Logic "0" or grounding inhibits updating of the latched parallel output data of the AD2016/B. Logic "1" or open circuit allows the data to be updated after each DPM conversion. This input has no effect on the normal conversion of the DPM.

DATA OUTPUTS<sup>3</sup> (See applications section for details on the data outputs)

Bit Parallel, Character Serial BCD Data Outputs Standard. 4 BCD data bits, positive true logic (CMOS, LPTTL or LP Schottky compatible, 1 LP Schottky load); 4 digit strobes (CMOS, TTL compatible, 1 TTL load); Polarity (CMOS, TTL compatible, 1 TTL load), logic "1" indicates positive polarity; Clock Output (CMOS, LPTTL or LP Schottky compatible, 1 LP Schottky load); Status Output (CMOS or LPTTL, 1 LPTTL load) are available.

Parallel BCD (AD2016/B) Optional. 3 BCD digits, Overrange, Overload and Data Ready Outputs (TTL compatible, 4 TTL loads). BCD data outputs are latched, positive true logic. The Overload Output is at Logic "0" for inputs greater than full scale range, Logic "1" when other data outputs are valid. Polarity Output (TTL compatible, 4 TTL loads latched) indicates positive polarity when high (Logic "1").

#### POWER INPUT

AC line, 50-60Hz. Power Consumption: 3.3 watts at 60Hz; 3.8 watts at 50Hz (Parallel BCD: 3.9 watts at 60Hz; 4.4 watts at 50Hz).

CALIBRATION ADJUSTMENTS (See application section for calibration instructions)

- Gain
- Zero (capability for system zero adjustment, meter is auto zero)
- Recommended recalibration interval: six months

SIZE

- 4.22"W x 1.97"H x 4.15"L (107 x 50 x 105mm)
- 4.77" (121mm) to rear of card edge connector
- Panel Cutout Required: 1.682" x 3.924" (42.72 x 99.67mm)

WEIGHT

12 ounces (340 grams)

**ORDERING GUIDE**<sup>4</sup>



DISPLAY LENS OPTIONS<sup>5</sup>

- Lens 7 Red with ADI logo
- Lens 8 Red without ADI logo

CONNECTOR (OPTIONAL)

30 pin, 0.156 spacing card edge connector, Amphenol 225-21524-601 (117) or equivalent

Optional: Order AC2611

NOTES

<sup>1</sup>Guaranteed at +25°C.

Guaranteed

- <sup>3</sup>No control inputs or data outputs can be used when the AD2016 is
- A control in power supply transformer at high common mode voltages.
   Only one AC power supply input and input range may be specified. The 'B" option can be ordered with any combination of power and

range options. <sup>5</sup> Lens 7 is supplied if no lens option is specified.

Specifications subject to change without notice.
## Applying the AD2016

#### Wiring Connections

Figure 1 is a wiring diagram for AD2016 applications. The "limited differential" input uses a  $47\Omega$  resistor to isolate the analog input from the digital and power supply sections to prevent ground loop problems. The analog ground must be connected to Pin 10 only, since there may be up to 200mV voltage difference between the input and digital ground.



Figure 1. AD2016 Wiring Interconnections

#### **Decimal Points**

Grounding, or Logic "0", applied to the appropriate pin will illuminate the desired decimal point. External drive circuitry, if used, must sink 50mA at a 25% duty cycle when the decimal point is turned on.

#### Display Blanking

Grounding, or Logic "0", blanks the entire AD2016 display with the exception of the decimal points on the tens and hundreds digit. The display is valid immediately upon removal of a blanking signal.

#### **Converter Hold**

Grounding, or Logic "0", causes the DPM to cease conversions and display the data from the last conversion. After a "Converter Hold" input is removed, the auto zero circuitry requires one or two conversions before the display and data outputs are again valid.

#### Data Hold (AD2016/B only)

Grounding, or Logic "0", on this input inhibits updating of the parallel BCD outputs of the AD2016/B. If the parallel data is interfaced to a printer, comparators, or a computer, requiring the data to be held stable for proper operation, the Data Hold input should be used to prevent data updating, but the DPM itself will continue making conversions. After a Data Hold input is removed, the BCD data will be updated at the end of the conversion cycle.

#### Extended Range Measurements

Although the full scale range of the AD2016 is 2000 counts, and it flashes the display to indicate overrange beyond this point, it actually makes measurements up to approximately 3000 counts. Beyond this point, it will flash a constant number. Thus, one can use this extra measurement range as a guide to reducing the input to the normal range. Note that the display will flash only the three full digits, since it is impossible to flash a "2" on the overrange readout. Thus, a reading of 2.300V or 230.0mV on an AD2016 will read as "300" and will be flashing.

BCD outputs on the standard AD2016 also will be valid up through the 3000 count range, but the BCD parallel outputs of the AD2016/B will indicate overload beyond 1999 counts.



Figure 2. AD2016 Timing Diagram

#### Interfacing Data Outputs - Character Serial Data

The BCD data outputs standard on the AD2016 are in a bit parallel character serial format. There are four BCD bit outputs (1, 2, 4, 8) and four digit outputs  $(10^0, 10^1, 10^2, 10^3)$  called D1, D2, D3 and D4 respectively. The BCD bits are gated onto the output lines sequentially in the order D1, D3, D2, D4 and the BCD bits are valid for the digit whose digit line is high. The serial output data is valid except when it is being updated, which occurs within 2 milliseconds after the Status line goes low, indicating the end of a conversion.

#### Interfacing Data Outputs - Parallel Data

The AD2016/B has data outputs in a full parallel BCD format. The output data is latched and is valid except for a 2ms period at the end of conversion when the "Data Ready" output is high (Logic "1"). As described above, the "Data Hold" input can be used to inhibit updating of the parallel data outputs without affecting the conversion of the DPM.

#### **Calibration Procedures**

A precision voltage reference is needed for the calibration of the AD2016. The location of the calibration potentiometers is shown in Figure 5. Always adjust the zero offset before the gain if zero adjustment is necessary.

Zero Adjustment: Short the signal inputs (Pins 2 and 10) and adjust the zero offset potentiometer until the meter reads 000.

Gain Adjustment: Apply an input of +1.800V (+180.0mV on AD2016/S, or +18.00V on AD2016/V) and adjust the gain potentiometer until the meter reads 1800 exactly.

#### **PIN DESIGNATIONS**

#### **AD2016 CHARACTER SERIAL**



(NC = NO CONNECTION)











Figure 5. AD2016 Mechanical Outline (Dimensions shown in inches and (mm)) Figure 6. AD2016 Mounting Instructions (Dimensions shown in inches and (mm))

## Low Cost 3½ Digit DEVICES Logic Powered DPM With LED Displays

## AD2021

#### FEATURES

"Second Generation" MOS-LSI Design Large 0.5" (13mm) LED Displays +5VDC Logic Powered ±1.999V, ±199.9mV or ±19.99V Full Scale Ranges Limited Differential Input Low Power Consumption: 2.0 Watts Small Size, Industry Standard Case Design

#### APPLICATIONS

General Purpose Logic Powered DPM Applications Portable Applications Requiring Low Power Consumption

#### GENERAL DESCRIPTION

The AD2021 is a low cost, 3<sup>1</sup>/<sub>2</sub> digit, +5V dc logic powered digital panel meter with large LED displays. While designed for general purpose DPM applications, the small size, light weight and low power consumption of the AD2021 make it an ideal digital readout for modern, compact instrument designs.

#### THE BENEFITS OF "SECOND GENERATION" DESIGN

The AD2021 is designed around MOS-LSI (Metal-Oxide-Semiconductor, Large Scale Integration) integrated circuits, which greatly reduce the number of components, and thereby the size, and reduce power consumption to 2.0 watts. Both the lower power consumption and fewer interconnections between components promise greatly increased reliability, and the circuit design maintains the performance and features of earlier DPMs. Large 0.5 inch (13mm) LED displays offer the visual appeal of gas discharge displays with the ruggedness and lifetime of all solid state devices.

EXCELLENT PERFORMANCE AND EASY APPLICATION

The AD2021 measures input voltage over a full scale range of  $\pm 1.999V$  dc or  $\pm 199.9mV$  dc ("S" option) with an accuracy of  $\pm 0.05\%$  reading  $\pm 0.025\%$  full scale  $\pm 1$  digit. Using the "limited differential" input first used on Analog Devices' AD2010, the AD2021 prevents ground loop problems and provides 35 to 50dB of common mode rejection at common mode voltages up to  $\pm 200mV$ . Normal mode rejection is 40dB at 50Hz to 60Hz.

BCD data outputs are provided in a bit parallel, character serial format compatible to CMOS logic systems. For those applications requiring parallel BCD data, schemes for making the serial to parallel conversion are available. Controls to hold readings, select decimal points and blank the display are provided.

#### DESIGNED AND BUILT FOR RELIABILITY

The AD2021 is packaged in Analog Devices' logic powered DPM case size, only 1.25 inches (32mm) deep. The small size of this DPM makes it easy to accommodate in any instrument design, and since several other manufacturers now use the same panel cutout for logic powered DPMs, this industry standardization allows mechanical second sourcing. In addition, the AD2021 uses the same pin connections as the AD2010 (except in BCD outputs, of course) as a convenience to allow updating



designs to take advantage of the second generation design and larger display of the AD2021. Each AD2021 receives a full one week failure free burn-in before shipment.



Figure 1. AD2021 Bit Parallel Character Serial to Full Parallel Data Conversion. AD2021 Pin Connections are Shown in Parentheses.

## SPECIFICATIONS

#### DISPLAY OUTPUT

- Light emitting diode, planar seven segment display readouts, 0.5" (13mm) high for three data digits, 100% overrange and negative polarity indication. Overload indicated by flashing display, polarity remains valid.
- Decimal points selectable at input connector.
- Display blanking on three data digits (does not affect overrange digit, polarity sign of decimal points).

#### ANALOG INPUT

- Configuration: bipolar, limited differential
- Full Scale Range: ±1.999V or ±199.9mV ("S" option) ±19.99V ("V" option)
- Automatic Polarity
- Auto Zero
- Input Impedance:  $100M\Omega$  ( $1M\Omega "V"$  option)
- Bias Current: 50pA
- Overvoltage Protection: ±50V dc, sustained

#### ACCURACY

- ±0.05% reading ±0.025% full scale ±1 digit<sup>1</sup>
- Resolution: 1mV, 10mV ("V" option) or 100µV ("S" option)
- Temperature Range<sup>2</sup>: 0 to +50°C operating; -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C Zero: auto zero
- Warm-Up Time to Rated Accuracy: less than one minute
- Settling Time to Rated Accuracy: 0.4 second

#### NORMAL MODE REJECTION

• 40dB at 50-60Hz

COMMON MODE REJECTION

- AD2021: 35dB (dc -10kHz)
- AD2021/S: 50dB (dc -10kHz)
- AD2021/V: 15dB (dc -10kHz)

#### COMMON MODE VOLTAGE

• ±200mV

#### CONVERSION RATE

- 5 conversions per second
- Hold and read on command

#### CONTROL INPUTS

- <u>Display Blanking</u>: (TTL, DTL compatible, 2 TTL loads). Logic "0" or grounding blanks the three data digits only, not the decimal points, overrange digit (if on) and polarity sign. Logic "1" or open circuit for normal operation. Display blanking has no effect on output data and the display reading is valid immediately upon removal of a blanking signal.
- <u>Hold</u>: (CMOS, DTL, TTL compatible, 1LP TTL load). Logic "0" or grounding causes the DPM to cease conversions and display the data from the last conversion. Logic "1" or open circuit for normal operation. After the "Hold" input is removed, one to two conversions are needed before the reading is valid.
- <u>Decimal Points</u>: Grounding or Logic "0" will illuminate the desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle when the decimal points are illuminated.

DATA OUTPUTS (See Application Section for details on data outputs)

- BCD Data Outputs: (CMOS, LP TTL or LP Schottky compatible), bit parallel, character serial format.
- Digit Strobe Outputs: (CMOS, DTL, TTL compatible, one TTL load). Logic "1" on any of these lines indicates the output data is valid for that digit.
- Polarity Output: (CMOS, TTL, DTL compatible, one TTL load). Logic "1" indicates positive polarity input, logic "0" indicates negative polarity.
- Status: (CMOS or LP TTL compatible). When this signal is at Logic "1", the output data is valid.
- Clock: (CMOS, DTL, TTL compatible, one TTL load). The clock signal is brought out to facilitate conversion from character serial to parallel data.
- INTERFACING DATA OUTPUTS. The BCD data outputs are in a bit parallel, character serial format. There are four' BCD bit outputs (1, 2, 4, 8) and four digit outputs (10<sup>0</sup>, 10<sup>1</sup>, 10<sup>2</sup>, 10<sup>3</sup>). The BCD digits are gated onto the output lines sequentially, and the BCD bits are valid for the digit whose digit line is high. The data is valid except when being updated which occurs within 2 milliseconds after the status line goes low.

#### **REFERENCE OUTPUT**

• A 6.4V ±5% analog reference output is made available. This reference should be buffered and filtered if use in external circuitry is desired.

#### POWER INPUT

• +5V dc ±5%, 1.45 watts

CALIBRATION ADJUSTMENTS (See Application Section for calibration instructions)

- Gain
- Zero
- Recommended recalibration interval: six months

#### SIZE

- 3"W x 1.8"H x 1.33"D (76 x 46 x 34mm)
- 1.90" (48mm) overall depth to rear of card edge connector.
- Panel cutout required: 3.175" x 1.810" (80.65 x 45.97mm).

#### WEIGHT

4 ounces, (115 grams)

**OPTIONS - ORDERING GUIDE** 

- Input Voltage Range: AD2021 1.9999V dc Full Scale AD2021/S – 199.9mV dc Full Scale AD2021/V – 19.99V dc Full Scale
- Display Lens Option<sup>3</sup>: Lens 5 Red with ADI logo Lens 6 – Red without ADI logo

#### CONNECTOR

- 30 pin, 0.156" spacing card edge connector. Viking 2VK15D/1-2 or equivalent.
- Optional: Order AC1501

NOTES

- <sup>1</sup>Guaranteed at 25°C and nominal supply voltage
- <sup>2</sup>Guaranteed <sup>3</sup>If no lens is specified, Lens 5 will be supplied.

Specifications subject to change without notice.



## Low Cost 4½ Digit DPMs With LED Displays

AD2024/AD2027

#### FEATURES

"Second Generation" MOS-LSI Design Large 0.43" (11mm) LED Displays 4% Digit Resolution -- 20,000 Counts Full Scale Limited Differential Input Either Line Powered (AD2024) or Logic Powered (AD2027) Industry Standard Case Designs

#### APPLICATIONS

High Resolution/High Accuracy Readout for: Test Equipment Process Control Instrumentation Analytical and Scientific Instruments

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#### **GENERAL DESCRIPTION**

The AD2024 and AD2027 are low cost 4½ digit DPMs with large LED displays. Both units offer the same features and identical performance, but the AD2024 is ac line powered and the AD2027 is +5V dc powered.

#### THE BENEFITS OF SECOND GENERATION DESIGN

The AD2024 and AD2027 are designed around MOS-LSI (Metal Oxide Semiconductor, Large Scale Integration) integrated circuits which greatly reduce the number of components and interconnections required to provide the performance and features expected in a high resolution 4½ digit DPM.

This "Second Generation" design, therefore, offers greatly increased reliability and significantly lower cost at little compromise in performance. The large 0.43 inch (11mm) LED displays offer the brightness and readability previously available only with gas discharge displays with the added advantage of an all solid state component.

#### HIGH RESOLUTION AND VERSATILE FEATURES

These DPMs measure dc input voltages over a full scale range of  $\pm 1.9999V$  with an accuracy of  $\pm 0.005\%$  reading  $\pm 0.005\%$  of full scale  $\pm 1$  digit. Using the "limited differential" input first used by Analog Devices on the AD2010, the AD2024 and AD2027 prevent ground loop problems and provide 50dB of common mode rejection at common mode voltages up to  $\pm 200$ mV. Normal mode rejection is 25dB at 50-60Hz.

BCD data outputs are provided in a bit parallel, character serial format compatible with CMOS logic systems. When applications require parallel BCD data, such as interfaces to printers, comparators or slave displays, parallel BCD output options are available that are compatible to standard TTL logic systems. External power supply outputs at +5V and -25V (-25V only on the AD2027) are made available for powering external circuitry. In addition, control inputs for conversion "Hold", display blanking and decimal point selection are provided.

#### INDUSTRY STANDARD CASE DESIGNS

Although both the AD2024 and AD2027 have identical electrical designs, they are packaged in the case sizes that have become industry standards for ac line powered and +5V dc logic powered DPMs respectively. The AD2024 fits the 3.924''x 1.682'' (99.67 x 42.74mm) panel cutout common to most ac line powered DPMs, and the AD2027 fits the 3.175'' x 1.810'' (80.65 x 45.97mm) panel cutout of the Analog Devices logic power case design, now used by several other manufacturers of logic powered DPMs. Thus, interchangeability is assured, allowing mechanical second sourcing for both these DPMs.

#### DESIGNED AND BUILT FOR RELIABILITY

Even beyond the reliability advantages of the LSI-IC design and LED displays, the AD2024 and AD2027 have had extreme care taken in their design and manufacture to insure reliability. Manufacturing processes are monitored by continual quality assurance inspections to insure proper workmanship and testing. Automatic test equipment is used to test each DPM thoroughly and without error. And each AD2024 and AD2027, like every Analog Devices DPM, receives a full one week failurefree burn-in before shipment.

## **SPECIFICATIONS**

#### DISPLAY OUTPUTS

- Seven Segment LED Display, 0.43" (11mm) high, for four data digits, 100% overrange and polarity indication.
- Overload indication by blanking all digits, polarity sign remains valid.
- Decimal points (4) selectable at input.
- Display Blanking

ANALOG INPUT

- Configuration: Bipolar, limited differential
- Full Scale Range: ±1.9999V (±19.999V, "V" Option)
- Automatic Polarity
- Input Impedance: 100MΩ (1MΩ, "V" Option)
- Bias Current: 30nA (3nA, "V" Option)
- Overvoltage Protection: 120V rms sustained

#### ACCURACY

- ±0.005% reading ±0.005% full scale ±1 digit<sup>1</sup>
- Resolution: 100µV
- Temperature Range<sup>2</sup>: 0 to +50°C operating. -20 to +85°C storage. (AD2024/B: 0 to +45°C operating)
- Temperature Coefficient: Gain:  $\pm 30 \text{ppm/}^{5}\text{C}$ . Zero Offset:  $\pm 10\mu \text{V/}^{\circ}\text{C}$  ( $\pm 40 \text{ppm/}^{\circ}\text{C}$  &  $\pm 100\mu \text{V/}^{\circ}\text{C}$ , "V" Option)
- Warmup Time: One minute to rated accuracy
- Settling Time to Rated Accuracy: 450ms

#### NORMAL MODE REJECTION

25dB at 50-60Hz

#### COMMON MODE REJECTION

- 50dB, dc to 1kHz, ±200mV common mode voltage
- AD2024 (floated on power supply transformer if data outputs and control signals are not used) 110dB at 120V rms common mode voltage, 1kΩ imbalance at input.

#### CONVERSION TIME

- 180ms for full scale reading
- 210ms for overload conversion

#### CONVERSION RATE

5 conversions per second

#### DIGITAL INTERFACE SIGNALS

Inputs

<u>Display Blank</u> – (DTL/TTL Compatible, 4 TTL Loads). Logic "0" or grounding blanks display, including polarity sign, but not decimal points. The display is valid immediately upon removal of the blanking signal.

<u>Hold</u> – (DTL/TTL Compatible, 2 TTL Loads). Logie "0" or grounding causes the DPM to hold and display the last conversion. Upon removal of the hold, the DPM resumes conversions.

<u>Decimal Points</u> – (Not TTL Compatible). Logie "0" or grounding turns on appropriate decimal point. External circuitry must sink 60mA when a decimal point is illuminated.

• Outputs

<u>DTL/TTL</u> Compatible<sup>3</sup> – Status. Logic "1" indicates conversion in process. All digital outputs are valid when status is at logic "0". 5 TTL loads. – Polarity. Logic "1" indicates positive polarity, latched. 5 TTL loads. <u>CMOS and LP Schottky Compatible</u> – Overload, Logic

"1" indicates overload (≥20,000), latched. – BCD outputs. 4½ BCD digits, character serial, bit parallel, 1 LP Schottky Load.

<u>Digital Strobe Outputs</u> – (CMOS or LP Schottky Compatible) Logic "1" on any of these line indicates the output data is valid for that digit, 1 LP Schottky Load.

<u>Parallel BCD Output</u> (Option "B"). – 4½ BCD digits, positive true, latched. Drives 5 TTL loads. – Data Ready. Logic "1" indicates output data is valid. Drives 2 TTL loads.

- EXTERNAL POWER SUPPLY OUTPUTS
  - AD2024: +5V at 25mA, -25V at 5mA
  - AD2027: -25V at 5mA
- POWER SUPPLY INPUTS
  - AD2024: ac line, 50-60Hz, 4.2W
  - AD2027: +5V dc, ±5% at 850mA
- CALIBRATION ADJUSTMENTS
- Gain
- Zero
- Recommended recalibration interval: 6 months
- SIZE
  - AD2024: 3.92"W x 1.67"H x 4.48"D (100 x 42 x 114mm) Panel cutout: 3.930" x 1.682" (99.8 x 42.7mm)
  - AD2027: 3"W x 1.8"H x 4"D (76 x 46 x 102mm) Panel cutout: 3.175" x 1.810" (80.65 x 45.97mm)

#### WEIGHT

- AD2024: 14 ounces (395 grams)
- AD2027: 10 ounces (280 grams)
- **OPTIONS ORDERING GUIDE**
- AD2024

AC Power Inputs AD2024 - 117V ac AD2024/E - 220V ac

- AD2024/F 100V ac  $\pm 10\%$
- AD2024/H 240V ac
- Input Range Options
- AD2024 ±1.9999V Full Scale
- AD2024/V ±19.999V Full Scale

Data Output Options (available with any power input options) AD2024 – Character serial data outputs

- AD2024/B Parallel BCD option
- Display Lens Options<sup>4</sup>
- Lens 7 Red with ADI logo
- Lens 8 Red without ADI logo
- <u>Connector</u> 36 pin, 0.156" spacing, card edge connector,

Viking 2VK18D/1-2 or equivalent. – Optional: Order AC2610.

AD2024/B option also requires a 30 pin, 0.156" spacing, card edge connector, Viking 2VK15D/1-2 or equivalent. - Optional: Order AC1501.

• AD2027

Input Range Options AD2027 - ±1.9999V Full Scale

 $AD2027/V - \pm 19.999V$  Full Scale

- Data Output Options
- AD2027 Character serial data outputs
- AD2027/B Parallel BCD option
- Display Lens Options<sup>4</sup>
- Lens 5 Red with ADI logo
- Lens 6 Red without ADI logo
- Connector AC1501 (see above) or equivalent. AD2027/B option requires two each.

#### NOTES

<sup>1</sup>Guaranteed at +25°C and nominal power supply voltage.

<sup>2</sup> Guaranteed. <sup>3</sup> For CMOS compatibility 3 3k pullup resistors to the +5V of

<sup>3</sup> For CMOS compatibility, 3.3k pullup resistors to the +5V output of the DPM are required.

<sup>4</sup> If no lens is specified, Lens 5 or 7 is supplied as appropriate. Specifications subject to change without notice.



Figure 1. AD2024 Wiring Interconnections



Figure 2. AD2027 Wiring Interconnections

#### Interfacing Data Outputs

The standard data outputs are in a bit parallel character serial format compatible to CMOS and LP Schottky logic systems. The BCD outputs are multiplexed, and a digit output is provided for each of the five digits of output. Thus, the four BCD lines on the output at a given time are valid for the digit whose digit line is currently high. The bit parallel character serial data is valid when the DPM status line is low for a period of 50ms between each conversion cycle. The overload line is latched output which is at logic "1", whenever the input exceeds the full 20,000 count range.

Optional parallel BCD outputs ("B" option) are available on a separate card which is internally connected to the DPM. The output data then is presented in a full parallel format and is latched. The parallel data is valid whenever the data ready output is high.

Pin connections for the "B" option are shown in the interconnection tables and a full timing diagram is shown in Figure 3.



NOTE 1. APPROX. 5ms REQUIRED TO LOAD PARALLEL-OUT REGISTERS. NOTE 2. B OPTION.

Figure 3. AD2024/AD2027 Timing Diagram

## Applying the AD2024 and AD2027

PIN	FUNCTION	PIN	FUNCTION
1	Analog Ground	A	Analog High
2	10 <sup>1</sup> Digit	В	10° Digit (LSD)
- = KE'		- = KE	
3	BCD 2	c	10 <sup>2</sup> Digit
4	10 <sup>3</sup> Digit	D	BCD 4
5	BCD 8	E	BCD 1
6	Mux Step 1	F	10 <sup>4</sup> Digit (MSD)
7	+5V dc (Out)	н	-25V dc (Out)
8	NC	J	NC
9	ac High	к	ac High
10	NC	L	NC
11	ac RETURN	M	ac Return
12	NC	N	NC
13	Digital Ground	Р	Digital Ground
14	NC	R	Status
15	Polarity	S	Hold
16	Display Blank	Т	DP1.XXXX
17	DP1XXX.X	U	DP1X.XXX
18	Overload	V	DP1XX.XX

AD2024 - Signal and Pin Connections

FUNCTION	PIN	FUNCTION
Analog High	Α	Analog Ground
10° Digit (LSD)	В	Mux Step.1
BCD 8	C	BCD 1
BCD 2	D	BCD 4
10 <sup>4</sup> Digit (MSD)	E	10 <sup>1</sup> Digit
10 <sup>3</sup> Digit	F	10 <sup>2</sup> Digit
NC	н	-25VDC (Out)
Power Ground	J.	Digital Ground
+5V (In)	к	+5V (In)
NC	L	NC
Y	- = KE	
Display Blank	м	NC
Hold	N	Polarity
Overload	Р	Status
DP1.XXXX	R	DP1X.XXX
DP1XX.XX	S	DP1XXX.X
	FUNCTION Analog High 10° Digit (LSD) BCD 8 BCD 2 104° Digit (MSD) 103° Digit NC Power Ground +5V (In) NC Display Blank Hold Overload DP1.XXXX DP1XX.XX	FUNCTION     PIN       Analog High     A       10° Digit (LSD)     B       BCD 8     C       BCD 2     D       10° Digit (MSD)     E       10° Digit (MSD)     F       NC     H       Power Ground     J       +5V (In)     K       NC     L       Y     = KEV       Display Blank     M       Hold     N       Overload     P       DP1.XXXX     R       DP1XXXX     S

NOTE 1: BCD multiplexer clock pulse available for remote placement of BCD option.

#### AD2027 - Signal and Pin Connections

		<i>.</i>	
PIN	FUNCTION	PIN	FUNCTION
1	+5V dc (In)	A	NC (Do Not Use)
2	BCD 1 (In)	B	BCD 8 (In)
-= KE	Y	-= ке	Ϋ́
3	BCD 4 (In)	С	BCD 2 (In)
4	BCD 2000	D	BCD 4
5	BCD 40	·Ε	BCD 80
6	BCD 800	F	BCD 8000
7	BCD 100	н	BCD 1000
8	BCD 10,000	J	BCD 200
9	BCD 20	к	BCD 2
10	BCD 8	L	BCD 10
11	BCD 1	М	BCD 4000
12	BCD 400	N	10 <sup>4</sup> Digit (In)
13	Data Ready	Р	Status (In)
14	Polarity (In)	R	Mux Step (In)
15	Polarity (Out)	S	Digital Ground

NOTES: 1) Overload output is on main DPM connector.

 Pins marked "In" are made available for remote placement of BCD option card and are not normally used since all connections are interval.

#### AD2024/AD2027 BCD Options – Signal and Pin Connections





#### PANEL CUTOUT: 3.930 × 1.682 (99.82 × 42.72)











#### PANEL CUTOUT: 3.175 × 1.180 (80.65 × 45.97)



Figure 5. AD2027 Mechanical Outline (Dimensions shown in inches and (mm))



## Low Cost 4¾ Digit DPMs With LED Displays

## AD2025/AD2028

#### FEATURES

"Second Generation" MOS-LSI Design Large 0.43" (11mm) LED Displays 4% Digit Resolution – 40,000 Counts Full Scale Limited Differential Input Either Line Powered (AD2025) or Logic Powered (AD2028) Interchangeable with 4% Digit DPMs (AD2024 or AD2027) Industry Standard Case Designs

#### APPLICATIONS

High Resolution/High Accuracy Readout for: Test Equipment Process Control Instrumentation Analytical and Scientific Instruments



#### GENERAL DESCRIPTION

The AD2025 and AD2028 are low cost 4<sup>3</sup>/<sub>4</sub> digit DPMs with large LED displays. Both units offer the same features and identical performance, but the AD2025 is ac line powered and the AD2028 is +5V dc powered.

The AD2025 and AD2028 are interchangeable with two 4½ digit DPMs available from Analog Devices, the AD2024 and AD2027 respectively. Thus, they can be used in applications where either a 4¼ or 4½ digit display may be desirable in one basic application.

#### THE BENEFITS OF SECOND GENERATION DESIGN

The AD2025 and AD2028 are designed around MOS-LSI (Metal Oxide Semiconductor, Large Scale Integration) integrated circuits which greatly reduce the number of components and interconnections required to provide the performance and features expected in a high resolution 4¼ digit DPM.

This "Second Generation" design, therefore, offers greatly increased reliability and significantly lower cost at little compromise in performance. The large 0.43 inch (11mm) LED displays offer the brightness and readability previously available only with gas discharge displays with the added advantage of an all solid state component.

#### HIGH RESOLUTION AND VERSATILE FEATURES

These DPMs measure DC input voltages over a full scale range of  $\pm 3.9999$ V or  $\pm 39.999$ V with an accuracy of  $\pm 0.005\%$  reading  $\pm 0.005\%$  of full scale  $\pm 1$  digit. Using the "limited differential" input first used by Analog Devices on the AD2010, the AD2025 and AD2028 prevent ground loop problems and provide 50dB of common mode rejection at common mode voltages up to  $\pm 200$ mV. Normal mode rejection is 25dB at 50-60Hz. BCD data outputs are provided in a bit parallel, character serial format compatible with CMOS logic systems. When applications require parallel BCD data, such as interfaces to printers, comparators or slave displays, parallel BCD output options are available that are compatible to standard TTL logic systems.

External power supply outputs at +5V and -25V (-25V only on the AD2028) are made available for powering external circuitry. In addition, control inputs for conversion "Hold", display blanking and decimal point selection are provided.

#### INDUSTRY STANDARD CASE DESIGNS

Although both the AD2025 and AD2028 have identical electrical designs, they are packaged in the case sizes that have become industry standards for ac line powered and +5V dc logic powered DPMs respectively. The AD2025 fits the 3.924''x 1.682'' (99.67 x 42.74mm) panel cutout common to most ac line powered DPMs, and the AD2028 fits the 3.175'' x 1.810''(80.65 x 45.97mm) panel cutout of the Analog Devices logic power case design, now used by several other manufacturers of logic powered DPMs. Thus, interchangeability is assured, allowing mechanical second sourcing for both these DPMs.

#### DESIGNED AND BUILT FOR RELIABILITY

Even beyond the reliability advantages of the LSI-IC design and LED displays, the AD2025 and AD2028 have had extreme care taken in their design and manufacture to insure reliability. Manufacturing processes are monitored by continual quality assurance inspections to insure proper workmanship and testing. Automatic test equipment is used to test each DPM thoroughly and without error. And each AD2025 and AD2028, like every Analog Devices DPM, receives a full one week failurefree burn-in with power cycling before shipment. 16

## **SPECIFICATIONS**

#### (typical at +25°C and nominal power supply voltage)

#### DISPLAY OUTPUTS

- Seven Segment LED Display, 0.43" (11mm) high, for four data digits and 300% overrange.
- Overload indication by blanking all digits except overrange, which indicates "0".
- Decimal points (5) selectable at input.
- Display Blanking

ANALOG INPUT

- Configuration: Bipolar, limited differential
- Full Scale Range: ±3.9999V (±39.999V, "V" option)
- Automatic Polarity (See applications section for details on polarity display)
- Input Impedance: 100MΩ (1MΩ, "V" option)
- Bias Current: 30nA (3nA, "V" option)
- Overvoltage Protection: 120V rms sustained

#### ACCURACY

- ±0.005% reading ±0.005% full scale ±1 digit<sup>1</sup>
- Resolution: 100µV (1mV, "V" option)
- Temperature Range<sup>2</sup>: 0 to +50°C operating. -20 to +85°C storage. (AD2025/B: 0 to +45°C operating)
- Temperature Coefficient: Gain: ±30ppm/°C. Zero Offset: ±10µV/°C (±40ppm/°C and ±100µV/°C, "V" option)
- Warmup Time: One minute to rated accuracy
- Settling Time to Rated Accuracy: 450ms

NORMAL MODE REJECTION

• 25dB at 50-60Hz

#### COMMON MODE REJECTION

- 50dB, DC to 1kHz, ±200mV common mode voltage
- AD2025 (floated on power supply transformer if data outputs and control signals are not used) -- 110dB at 120V rms common mode voltage, 1kΩ imbalance at input.

#### CONVERSION TIME

- 300ms for full scale reading
- 400ms for overload conversion

#### CONVERSION RATE

- 3 conversions per second
- DIGITAL INTERFACE SIGNALS

#### Inputs

<u>Display Blank</u> – (open collector TTL Compatible, 4 TTL Loads). Logic "0" or grounding blanks display, but not decimal points. The display is valid immediately upon removal of the blanking signal.

<u>Hold</u> – (DTL/TTL Compatible, 2 TTL Loads). Logic "0" or grounding causes the DPM to hold and display the last conversion. Upon removal of the hold, the DPM resumes conversions.

<u>Decimal Points</u> – (Not TTL Compatible). Logic "0" or grounding turns on appropriate decimal point. External circuitry must sink 35mA when a decimal point is illuminated.

Outputs

DTL/TTL Compatible<sup>3</sup> – Status. Logic "1" indicates conversion in process. All digital outputs are valid when status is at logic "0". 4 TTL loads. – Polarity. Logic "1" indicates positive polarity, unlatched. 6 TTL loads. – Overload, Logic "1" indicates overload (≥40,000), unlatched 4 TTL Loads.

<u>CMOS and LP Schottky Compatible</u> – BCD outputs, 4<sup>4</sup>/<sub>4</sub> BCD digits, character serial, bit parallel, 1 LP Schottky load.

Parallel BCD Output (Option"B"). – 4¼ BCD digits, positive true, latched. Drives 5 TTL loads. – Data Ready. Logic "1" indicates output data is valid. Drives 2 TTL loads. – Polarity. Logic "1" indicates positive polarity, latched, Drives 2 TTL loads.

<u>Digit Strobe Outputs</u> – (CMOS or LP Schottky Compatible) Logic "1" on any of these lines indicates the output data is valid for that digit, 1 LP Schottky load.

#### VOL. II, 16–30 DIGITAL PANEL INSTRUMENTS

- EXTERNAL POWER SUPPLY OUTPUTS
  - AD2025: +5V at 25mA, -25V at 5mA
  - AD2028: -25V at 5mA

#### POWER SUPPLY INPUTS

- AD2025: ac line, 50-60Hz, 4W
- AD2028: 5V dc, ±5% at 800mA
- CALIBRATION ADJUSTMENTS
  - Gain
  - Zero
  - Recommended recalibration interval: 6 months

SIZE

- AD2025: 3.92"W x 1.67"H x 4.48"D (100 x 42 x 114mm) Panel cutout: 3.930" x 1.682" (99.8 x 42.7mm)
   AD2028: 3"W x 1.8"H x 4"D (76 x 46 x 102mm)
- AD2028: 3"W x 1.8"H x 4"D (76 x 46 x 102mm) Panel cutout: 3.175" x 1.810" (80.65 x 45.97mm)

#### WEIGHT

- AD2025: 14 ounces (395 grams)
- AD2028: 10 ounces (280 grams)
- **OPTIONS ORDERING GUIDE**<sup>4</sup>
- AD2025
  - AC Power Inputs No cost option
  - AD2025 117V ac
  - AD2025/E 220V ac  $\pm 10\%$
  - AD2025/F 100V ac AD2025/H - 240V ac
  - Input Range Options No cost option
  - AD2025 ±3.9999V Full Scale
  - $AD2025/V \pm 39.999V$  Full Scale
  - Data Output Options See pricing guide
  - AD2025 Character serial data outputs
  - AD2025/B Parallel BCD option
  - Display Lens Options<sup>5</sup>
  - Lens 7 Red with ADI logo
  - Lens 8 Red without ADI logo
  - <u>Connector</u> 36 pin, 0.156" spacing, card edge connector, Viking 2VK18D/1-2 or equivalent. – Optional: Order AC2610.

AD2025/B option also requires a 30 pin, 0.156" spacing, card edge connector, Viking 2VK15D/1-2 or equivalent. – Optional: Order AC1501.

• AD2028

- Input Range Options No cost option
- AD2028 ±3.9999V Full Scale
- AD2028/V ±39.999V Full Scale
- Data Output Options See pricing guide
- AD2028 Character serial data outputs
- AD2028/B Parallel BCD option
- Display Lens Options<sup>5</sup>
- Lens 5 Red with ADI logo
- Lens 6 Red without ADI logo

<u>Connector</u> – AC1501 (see above) or equivalent. AD2028/B option requires two each.

NOTES

<sup>1</sup>Guaranteed at +25°C and nominal power supply voltage.

<sup>2</sup>Guaranteed.

<sup>3</sup> For CMOS compatibility, 3.3k pullup resistors to the +5V output of the DPM are required.

<sup>4</sup> Only one AC Power Input and/or Input Range option may be specified. The "B" option can be ordered with any combination of power and range options.

<sup>5</sup> If no lens is specified, Lens 5 or 7 is supplied as appropriate. Specifications subject to change without notice.

## Applying the AD2025 and AD2028

#### APPLYING THE AD2025 AND AD2028 Wiring Connections

Figures 1 and 2 are wiring diagrams for AD2025 and AD2028 applications. The "limited differential" input uses a  $100\Omega$ resistor to isolate the analog input from the digital and power supply sections to prevent ground loop problems. The analog input must be connected between the "analog high" and "analog ground" inputs only, since in some applications there

may be up to a ±200mV CMV difference between analog and digital grounds.



Figure 1. AD2025 Wiring Interconnections

Figure 2. AD2029 Wiring Interconnections

#### **Polarity Indication**

No direct polarity indication is provided on the AD2025 or AD2028 although both DPMs measure bipolar inputs. If indication of negative polarity is desired, the "polarity" output can be connected to the far left hand decimal point (DP .XXXXX) provided. When the polarity is negative, this decimal point will then be illuminated.

#### Interfacing Data Outputs

The standard data outputs are in a bit parallel character serial format compatible to CMOS and LP Schottky logic systems. The BCD outputs are multiplexed, and a digit output is provided for each of the five digits of output. Thus, the four BCD lines on the output at a given time are valid for the digit whose digit line is currently high. The bit parallel character serial data is valid when the DPM status line is low for a period of 150ms between each conversion cycle. The overload line is latched output which is at logic "1", whenever the input exceeds the full 40,000 count range.

Optional parallel BCD outputs ("B" option) are available on a separate card which is internally connected to the DPM. The output data then is presented in a full parallel format and is latched. The parallel data is valid whenever the data ready output is high.

Pin connections for the "B" option are shown in the interconnection tables and a full timing diagram is shown in Figure 3.



Figure 3. AD2025/AD2028 Timing Diagram

PIN	FUNCTION	PIN	FUNCTION
1	Analog Ground	A	Analog High
2	10 <sup>1</sup> Digit	В	10° Digit (LSD)
- = KE	·	- = KE	(
3	BCD 2	С	10 <sup>2</sup> Digit
4	10 <sup>3</sup> Digit	D	BCD 4
5	BCD 8	E	BCD 1
6	Mux Step <sup>1</sup>	F	10 <sup>4</sup> Digit.(MSD)
7	+5V dc (Out)	н	-25V dc (Out)
8	NC	J	NC
9	AC High	К	AC High
10	NC	L	NC
11	AC Return	M	AC Return
12	NC	N	NC
13	Digital Ground	Р	Digital Ground
14	DP .XXXXX	R	Status
15	Polarity	S	Hold
16	Display Blank	Т	DPX.XXXX
17	DPXXXX.X	U	DPXX.XXX
18	Overload	V	DPXXX.XX

NOTE	1:	BCD	multiplexer	clock	pulse	available	for
		remo	te placemer	nt of B	CD o	ption.	

AD2025	– Signal	and Pin	Connections
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PIN	FUNCTION		PIN	FUNCTION
1	Analog High		А	Analog Ground
2	10° Digit (LSD)	11	В	Mux Step <sup>1</sup>
3	BCD 8	11	С	BCD 1
4	BCD 2	11	D	BCD 4
5	10 <sup>4</sup> Digit (MSD)	11	E	10 <sup>1</sup> Digit
6	10 <sup>3</sup> Digit	11	F	10 <sup>2</sup> Digit
7	NC	11	н	-25V dc (Out)
8	Power Ground	11	J	Digital Ground
9	+5V (In)	11	к	+5V (In)
10	NC	11	L	NC
-= KE'	Y		- = KE'	Y
11	Display Blank		м	DP.XXXXX
12	Hold		N	Polarity
13	Overload	1	Р	Status
14	DPX.XXXX		R	DPXX.XXX
15	DPXXX.XX		S	DPXXXX.X

#### AD2028 — Signal and Pin Connections

PIN	FUNCTION	PIN	FUNCTION
1	+5V dc (in)	A	BCD 20,000
2	BCD 1 (In)	В	BCD 8 (In)
— = KE	Υ	= KE	Y
3	BCD 4 (In)	C	BCD 2 (In)
4	BCD 2000	D	BCD 4
5	BCD 40	E	BCD 80
6	BCD 800	F	BCD 8000
7	BCD 100	н	BCD 1000
8	BCD 10,000	J	BCD 200
9	BCD 20	к	BCD 2
10	BCD 8	L	BCD 10
11	BCD 1	М	BCD 4000
12	BCD 400	N	10 <sup>4</sup> Digit (In)
13	Data Ready	Р	Status (In)
14	Polarity (In)	R	Mux Step (In)
15	Polarity (Out)	s	Digital Ground

NOTES: 1) Overload output is on main DPM connector. 2) Pins marked "In" are made available for remote placement of BCD option card and are not normally used since all connections are internal.

AD2025/AD2028 BCD Options — Signal and Pin Connections



VOL. II, 16-32 DIGITAL PANEL INSTRUMENTS

## 

## Low Cost 3 Digit AC Line or Logic Powered DPM

## AD2026\*

#### FEATURES

Third Generation I<sup>2</sup> L LSI Design Either Line Powered or Logic Powered Large 0.56" Red Orange LEDs Balanced Differential Input/Floating 1000V, CMV Terminal Block Interface (ac Version) High Reliability: > 250,000 Hour MTBF Small Size and Weight Low Cost

#### GENERAL DESCRIPTION

The AD2026 is specifically designed to provide a digital alternative to analog panel meters. The AD2026 is available either logic powered (+5V dc) or ac line powered. Most of the analog and digital circuitry is implemented on a single I<sup>2</sup>L LSI chip, the AD2020. Only 13 additional components are required to complete the AD2026 +5V dc version. The entire dc version is mounted on a single  $3'' \times 15/8''$  PCB. AC line power is achieved with the addition of a second PCB containing the ac power transformer and power supply circuitry.

The AD2026, on both the ac line and logic powered versions, offers as a standard feature, 0.56" high LED Displays. Brightness is enhanced on both versions due to the Red Orange lens. In addition to the Red Orange lens, the AD2026 is also available with a dark red lens for applications where maximum brightness is not required and minimum backlighting is desired.

A unique patented case design utilizes molded-in fingers, both to capture the PCB in the case and to provide snap-in mounting of the DPM in a standard panel cutout. No mounting hardware of any kind is used. The dc version occupies less than 1''of space behind the panel. The line powered version offers the same mounting features but occupies 2 1/2'' of behind-panel space.

#### **EXCELLENT PERFORMANCE**

The AD2026 offers the instrument designer digital accuracy, resolution and use of readout while occupying less space than its analog counterpart. Other features of analog meters such as reliability and instantaneous response are retained in the AD2026.

The AD2026 measures and displays inputs from -99mV to +999mV, with an accuracy of 0.1% of reading  $\pm 1$  digit. Zero shift is less than one bit over the full operating temperature range, resulting in the same performance as a DPM with auto zero. The balanced differential input of the dc powered AD2026 rejects common mode voltages up to 200mV, enough to eliminate most ground loop problems. The floating differential input inherent in the ac line powered version offers 1000V of common mode voltage rejection.

\*Covered by patent numbers: 4,092,698; 29,992; 3,872,466; and 3,887,863.



Optional 10.0V full scale (F.S.) range is available on the ac line version that will accept inputs from -0.99V to 9.99V.

#### WIRING CONNECTIONS

For Balanced Differential operation with the AD2026 dc version, connect input as shown in Figure 1. The common mode loop must provide a return path for the bias currents internal to the AD2026. The resistance of this path must be less than  $100k\Omega$  and total common mode voltages must not exceed 200mV.

For applications where attenuation is required, scaling resistors can be connected between pins 6 and 7 and between pins F and H. Pin 5 must be used as the High Analog Input when scaling resistors are used and pin 4 when they are not. Pin E is the Analog Low Input.



Connection to the ac line powered AD2026 is via the terminal strip on the rear. AC line power is connected to terminals 4 and 5 and the signal input is connected to terminal 1 (Analog HI) and 2 (Analog Ground).

#### SPECIFICATIONS (typical at +25°C and nominal supply voltage unless otherwise noted)

#### DISPLAY OUTPUT

- Light emitting diode, planar seven segment display readouts, 0.56" (14.6mm) high (orange)
- Overload Indication: EEE
- Negative Indication: -XX
- Negative Overload Indication: ----
- Decimal Points: three (3) selectable at input connector (dc version); internally . on ac version

ANALOG INPUT

- Configuration: balanced differential input (dc version) single ended isolated (ac version)
- Full Scale Range: -99mV to +999mV
- -0.99V to +9.99V (10V option on ac version)
- . Automatic Polarity Input Impedance: 100MΩ; 100kΩ (10V option)
- . Bias Current: 100nA
- Overvoltage Production: ±15V dc, sustained

ACCURACY

- ±0.1% ±1 digit<sup>1</sup>
- Resolution: 1mV or 10mV
- Temperature Range<sup>2</sup>: -10°C to +60°C operating; -25°C to +80°C storage
  - Temperature Coefficient: Gain: 50ppm/°C Zero: 10µV/°C (essentially auto zero)
  - Warm-Up Time to Rated Accuracy: Instantaneous
- Settling Time to Rated Accuracy: 0.3 second for full input voltage swing (dc version); 0.75 second for full input voltage swing (ac version)

COMMON MODE REJECTION (1k source imbalance, dc to 1kHz)

- 50dB, ±200mV common mode voltage (dc version)
- 116dB (96dB on 10V range); 1000V rms max CMV (ac version)

#### NORMAL MODE REJECTION

30dB at 50-60Hz (ac version)

#### CONVERSION RATE

- 4 conversions per second
- · Hold and read on command (dc version only)

#### CONTROL INPUTS

Display Blanking/Display Power Input, (dc version only): The display of the AD2026 can be blanked by removal of power to the display power input, with no effect on conversion circuitry. If external logic switching is used, the display requires 110mA peak (85mA average) when illuminated.

Hold (deversion only): When the Hold input is at Logic "0", grounded or open circuit, the AD2026 will convert at 4 conversions per second. If a voltage of 0.6V to 2.4V is applied to this input, the DPM will stop converting and hold the last reading. A  $12k\Omega$  resistor in series with this input to +5V will provide the proper voltage input. (Consult factory for "HOLD" on ac version.)

#### DECIMAL POINT

- To illuminate decimal points on dc version, ground appropriate pin (A, B or 3).
- To illuminate decimal points on ac version, remove shroud and bridge appropriate solder pad (A, B or 3).

#### POWER INPUT LOGIC POWER<sup>3</sup>

- Converter: +5V ±5%, 0.2 watts typ; 0.33 watts max • Display: +5V ±40%, 0.45 watts typ; 0.75 watts max
- POWER INPUT AC LINE POWER
  - AC line, 50-60Hz, 1.5 watts

#### CALIBRATION ADJUSTMENTS

- Gain
- Zero
- ٠ Recommended recalibration interval: six months
- SIZE<sup>4</sup>
  - 3,43"W × 2,0"H × 0.85"D (87 × 52 × 22mm)
  - ٠ 0.88" (22mm) overall depth to rear of connector
  - Panel cutout required: 3.175 ±0.015" × 1.810 ±0.015" .
  - (80.65 ±0.38 × 45.97 ±0.38mm)

#### WEIGHT

- 1.8 ounces (53 grams) (dc version)
- 7 ounces (198 grams) (ac version)

CONNECTIONS

A 10-pin T&B/Ansley 609-1000M with two feet of 10 conductor ribbon cable is available. Order AC2618 (dc version, only).

Conductor to pin A is color coded. Sequence of ribbon connections is A, 1, B, 2, C, 3, etc.

The AD2026 ac version is complete with terminal strip for easy interface. ORDERING GUIDE



NOTES

- Guaranteed at +25°C and nominal supply voltage.
- <sup>2</sup>Guaranteed.
- <sup>3</sup>When the same power supply is used to power both display and converter, +5V, ±5%, 0.65 watts typical, 0.9 watts max is required.
- Dimensions for ac line powered version: 3.43"W X 2.0"H X 2.44"D (87mm X 52mm X 63mm)
- No Charge Options
- <sup>6</sup>10V de full scale option is available on ac power only
- Specifications subject to change without notice.

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



IMI



3 17 (80 52)

PANEL THICKNESS 0.0625 TO 0.125 (1.6) TO (3.2)

#### **PIN CONNECTIONS**



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AD2026

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## 6 Channel Scanning Digital Thermometer

## AD2036

#### FEATURES

Automatic/Manual Scan of 6 Thermocouples (TCs) External Channel Selection by BCD Code J, K, or T Thermocouple °C or °F Readout Self-Contained Linearization Isolated Analog Input Parallel BCD Output 1° Resolution, 0.1° Optional AC Line or dc Powered +5V dc at 10mA for External Logic



#### APPLICATIONS

#### Multi-Point Temperature Measurements for Remote Data Acquisition and Data Logging Temperature Monitoring in Design, Laboratory, Manufac-

turing and Quality Control

#### GENERAL DESCRIPTION

The AD2036 is a low cost 3½ digit, ac line or dc powered digital readout temperature meter. Inputs for six thermocouples of identical types, either J, K, or T and calibrated temperature ranges in °C or °F, make up a total of six available models.

Cycling on an internal clock, the AD2036 can continually scan 6 input channels. Individual channels can be manually selected via a small switch on the front. Channel selection can also be made via an external BCD input at the rear connector. A separate channel select output identifies the selected channel independent of selection mode. The channel select output together with the BCD Output provides complete information for automatic data collection. The Isolated Parallel BCD Output provides an easy interface to conventional recording and controlling instruments. For applications where there are high common mode voltages (CMV) present, the AD2036 has as a standard feature a floating opto isolated analog front end that will withstand CMV's up to 250V rms.

The AD2036 displays readings on large 0.5" (13mm) high LED displays. Both (+) and (-) polarities are indicated. Controls are provided for blanking the display.

#### AUTO/SCAN

The AD2036, while in the Auto/Scan mode, will permit unattended scanning of all six input channels. The rate of the channel select is 3.2 seconds, 1.6 seconds or 0.8 seconds. The AD2036 can be used as a stand-alone instrument and with the Scan input held high will continually scan six channels. When the Scan input is brought low the AD2036 will continue to cycle and stop at channel 0. When used with a printer the channel select number in addition to the converted BCD value can be recorded.

#### MANUAL CHANNEL SELECTION

A switch on the front enables the user to manually select an individual thermocouple. As in the Auto/Scan mode, the BCD Output of the selected channel and the channel number are available. Selection of an individual TC channel automatically disables Scan and external channel selection is overridden. The Mode Output pin indicates when the switch is in this condition. On special order, meters can be supplied with card edge control for disabling the switch.

#### EXTERNAL CHANNEL SELECTION

For remote control of channel selection the AD2036 provides an input for an external BCD code selection. This feature enables external BCD switch, automatic microprocessor or computer control.

#### STANDARD PACKAGING

The AD2036 is packaged in Analog Devices' ac line powered DPM case which uses the same panel cutout as most other ac line powered DPM's from other manufacturers. In addition, the pin connections for the AD2036 converter board are the same as for the AD2022, AD2009, AD2016 and DPM's available from several other manufacturers. 16

#### TYPES OF THERMOCOUPLE (TCs): J, K, or T

#### ACCURACY<sup>1</sup>

°C		Error ±½LSB	°F		Error ±½LSB
J	-60 to 0	±1.4	J	-76 to 32	±2.5
	0 to 500	±1.4		32 to 932	±2.5
	500 to 760	±2.2		932 to 1400	±4.0
к	-60 to 0	±1.4	к	-76 to 32	±2.5
	0 to 150	±1.4		32 to 302	±2.5
	150 to 1350	±2.6		302 to 2000	±4.7
т	-100 to 0	±1.3	т	-148 to 32	±2.3
	0 to 250	±1.5		32 to 450	±2.7
	250 to 400	±2.0		450 to 752	±3.6

#### DISPLAY OUTPUT

- Light emitting diode (LED), seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload >1999 indicated by flashing display, polarity remains valid. There is no overload indication for out of range readings.
- Decimal points (3) selectable at input connector.

Display Blanking

SIGNAL INPUT

- Input Impedance: 100MΩ
- Bias Current: 10nA
- Overvoltage Protection Between Channels: ±18V neak max
- Common Mode Voltage: ±350V peak max
- CMV Between Channels: ±6V peak max
- Temperature Coefficient: Span: +temp, 100ppm; -temp, 120ppm Zero: 0.03degrees/degree C or F
- Settling Time to Rated Accuracy: 2.0 seconds (full span step input)
- Normal Mode Rejection: 60dB at 50 400Hz
- Common Mode Rejection: 120dB @ 250V rms max CMV (Between TC's and digital gnd),  $dv_{cm}/dt{<}10^6$  V/sec, 250 $\Omega$  imbalance

#### CONVERSION RATE

- 5 conversions per second
- Hold and read on command

CONTROL INPUTS

Display Blanking (TTL Compatible, 3 LSTTL Load) - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

Converter Hold (CMOS, TTL Compatible, 1 LSTTL Load) - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD are valid.

Decimal Points (Not TTL Compatible) - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle, when decimal point is illuminated.

Data Hold (TTL Compatible, 1 TTL Load) - Logic "0" or grounding inhibits updating of latched parallel output data of AD2036. Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on the normal conversion of the DPM and its display.

Scanner Enable (CMOS/TTL Compatible 1 LSTTL Load) - Logic "1" will enable Scanner to control the channel selection. External channel input BCD lines can remain connected. A Logic "0" enables external channel selection

Scan (Scan) (CMOS/TTL Compatible, 1 LSTTL Load) - A Logic "1" ("0") for <4 seconds will initiate a scan of six channels. To use Scan input, the Scan input must be a Logic "0". Both inputs have debounce circuitry. A momentary scan pulse while in the switch or external selection mode will initiate a sequence of six readings of the channel that is addressed then stop.

Channel BCD Input (CMOS/TTL Compatible 1 LSTTL Load) - Logic "0" on Scanner Enable will allow use of external control. All other control inputs remain the same.

Channel Increment (CMOS/TTL Compatible 1 LSTTL Load) - Positive going edge will initiate sequence to the next channel.

Spare Inverter Input (CMOS, TTL Compatible 1 LSTTL Load) - Spare inverter supplied for customer convenience.

DATA OUTPUTS

Isolated Parallel BCD Outputs - 3 BCD digits, Overrange, Overload and Data Ready Outputs (TTL Compatible, 4 TTL Loads). BCD data outputs are latched positive true logic. Overrange Output is Logic "1" for data display greater than 999. Overload Output is Logic "0" for inputs greater than full scale range, Logic "1" when other data outputs are valid. Polarity Output (TTL Compatible, 4 TTL Loads latched) indicates positive polarity when high (Logic "1"). Digital outputs are fully isolated from input circuitry; all logic levels are referenced to digital ground.

Channel BCD Outputs (CMOS/TTL Compatible 2 TTL Loads) - BCD Channel number data outputs are positive true.

Mode Output (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" indicates channel selection is by switch. Logic "0" indicates selection is by scanner or external control, useful in microcomputer interface.

Data Ready (Data Ready) (CMOS/ITL Compatible 2 TTL Loads) - Logic "1" ("0") indicates data from Temperature Card is ready. Data remains valid until next clock pulse (198ms).

Spare Inverter Output (CMOS/TTL Compatible 2 TTL Loads) - Spare inverter supplied for customer convenience.

Clock OUT (CMOS, TTL Compatible, 2 TTL Loads) - Indicates E.O.C. When Clock pulse is high latches are being updated, data is invalid. Data is valid on negative going edge. Clock OUT pulse is disabled when DATA HOLD line is low.

Analog Output - Nonlinear Error ±0.5% ±1mV

 $V_{OUT}$ , °C = (1.784mV/°C) Temperature  $V_{OUT}$ , °F = (0.991mV/°F)(T-32)

TEMPERATURE RANGE<sup>2</sup>

0 to +50°C Operating
 -25°C to +85°C Storage

POWER OUTPUT

+5V dc @ 10mA

POWER INPUT

- AC line 50 400Hz, See Voltage Options below
- Power Consumption 5.8W @ 50 40011z

12V dc +20% - 10%, 4.8W ٠

• 5V dc ± 5% 4W

CALIBRATION ADJUSTMENTS

Span

- Zero
- . Recommended Recalibration Interval: six months SI7F
- 3.92" x 1.67"H x 5.80"D (100 x 42 x 147mm)
  Panel cutout 3.930" x 1.682" (99.8 x 42.7mm)
- WEIGHT

1.25 pounds (0.568 kg)

DISPLAY LENS<sup>4</sup> Lens 22-1: Red, °C with ADI Logo Lens 22-2: Red, °F with ADI Logo

Lens 23-1: Red, °C without ADI Logo Lens 23-2: Red, °F without ADI Logo

CONNECTORS(2) 2 each, 30 pin, 0.156" spacing card edge connector Viking 2VK15D/1-2 or equivalent.

Optional: Order AC1501. ORDERING GUIDE



NOTES <sup>1</sup> For 0.1° resolution accuracy remains the same. Range is limited to

Guaranteed

<sup>3</sup>Only one option may be specified. <sup>4</sup>Lens 22 is supplied if no lens option is specified.

Specifications subject to change without notice.

# 

## 6 Channel Scanning Digital Voltmeter/ Thermometer

## AD2037/AD2038

#### FEATURES

Automatic Scan of 6 Channel Inputs Manual Selection of Individual Channel External Channel Selection by BCD Code ±199.9mV or ±1.999V dc Full Scale Range Isolated Analog Input Parallel BCD Output Accessible Gain Points for Implementation of Selectable Gain, to 6V dc F.S. ±12V dc and +5V dc for External Use AD2038: High Accuracy Temperature Measurements Used with AD590/AC2626 Transducer/Probe 0.1° Resolution; 6 Channels -55.0°C to +150.0°C (-67.0°F to +199.9°F)

#### APPLICATIONS

- AD2037: Multi-point Measurements for Data Acquisition, Logging and Control
  - Data Processing from: Pressure and Flow Transducers; RTD and Thermistor Transducers; AD590 Temperature Transducers; LVDT and Level Transducers; Voltage and Current Sources.
- AD2038: Temperature Monitoring in Laboratory, Manufacturing, and Quality Control

#### AD2037 GENERAL DESCRIPTION

The AD2037 is a low-cost 3 1/2 digit, ac line powered, 6 channel digital scanning voltmeter designed to interface to printers, computers, serial data transmitters, telephone lines, etc., for display, control, logging or transmission of multichannel analog data. With appropriate external signal conditioning on each channel, the AD2037 becomes a versatile building block for a broad range of data acquisition, data logging, or control applications.

Channel selection is made via three methods: manual, using the switch provided on the front; Auto/Scan, where the AD2037 cycling on an internal clock can continually scan the 6 input channels; or External selection, where control inputs provided on the rear connector enables channel selection via external BCD code.

A separate channel select output identifies the selected channel independent of selection mode. The channel select output together with converted BCD output provides complete information for automatic data collection. For applications where there are high common mode voltages (CMV) present, the AD2037 has as a standard feature, a floating opto isolated analog front end that will withstand CMV's up to 250V rms. The  $\pm 199.9$ mV full scale range or  $\pm 1.999$ V dc full scale range are user selectable via a jumper on the rear connector. Other full scale ranges, to 6V dc, are programmable, via one (1) external resistor.



#### **AD2038 GENERAL DESCRIPTION**

The AD2038 is a dedicated 6 channel digital scanning thermometer. Based on the AD2037 and designed to be used in conjunction with Analog Devices' AD590 Temperature Transducer or Analog Devices' AC2626 Temperature Probe, the AD2038 retains all of the input/output features of the AD2037 as well as the channel selection methods.

The AD2038 and AD590/AC2626 will measure and display temperatures to  $\pm 1.3^{\circ}$ C accuracy over the temperature range of  $-55.0^{\circ}$ C to  $+150.0^{\circ}$ C ( $-67.0^{\circ}$ F to  $200.0^{\circ}$ F), over limited temperature ranges around a calibration point, accuracies approach a few tenths of a degree.

The AD590 is a laser trimmed, two terminal IC Temperature Sensor. Its output is a current  $(1\mu A \text{ per}^{\circ} K)$  linearly proportional to absolute temperature thus eliminating the need for linearization and cold junction compensation.

Due to the AD590's high impedance current output, it is insensitive to voltage drops over long lines thus enabling remote monitoring with no need for costly transmitters or special wire.

For normal applications the AD590J can be used and calibrated at a single temperature point. Where better linearity or sensor interchangeability is needed, the "K" and "L" versions are available. All versions are available to MIL-STD-883A Class B processing. In addition, the AC2626 (an AD590JF mounted in a 3/16 inch diameter, by 6 inch long stainless steel probe) is available. The probe is supplied with 3 feet of wire for easy interface to the AD2038.

For detailed information, contact factory.

#### SPECIFICATIONS (typical @ +25°C and nominal power supply voltage)

#### DISPLAY OUTPUT

- Light crititing diode (LED), seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload indicated by flashing display, polarity remains valid. Three is no indication of out of sensor range on AD208.
- Decimal Points (3) Selectable at Input Connector
- Display Blanking
- Sensor Disconnect Indication same as overload.
- ANALOG INPUT
- Opto/Transformer Isolated
- Configuration: Differential, isolated
  ±1.999V dc and ±199.9mV dc Full Scale Range
- Full Scale Range Programmable to 6V de Input Impedance: 250MΩ
- Bias Current: 1.5nA
- Overvoltage Protection: (Continuous Without Damage) Normal Mode: ±30V pk Channel to Channel: ±30V pk

ACCURACY AD2037

- ±0.05% Reading ±1 digit<sup>1</sup>
- Resolution: Programmable
  Temperature Range: 0 to +50°C operating; -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C
- Zero: 1.5µV/°C
- Warm-up Time to Rated Accuracy: Less than 5 minutes Settling Time to Rated Accuracy: 0.6 seconds ( - full scale to + full scale)
- Max Voltage Between Channels: ±199.9mV FS; ±6.1V pk ±1.999V FS; ±2.5V pl

#### ACCURACY

AD2038 Resolution 0.1°

- Range -55°C to +150°C
- -67°F to +200°F

• Accuracy (11) 1 digitizing error)	۰2	error	na.	izi	ait	d	۱°	+n	· · · /	1172	Acc	•
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	,	AD590J	AD590K	AD590L
	Sensor calibrated at +25°C (over range)	±2.2°C max	±1.2°C max	±1.2°C max
	Uncalibrated Error at +25°C	±5.2°C max	±2.2°C max	±1.2°C max
	Uncalibrated Error (over range)	±9.2°C max	±4.0°C max	±2.6°C max
	Nonlinearity (over range)	±2.0°C max	±0.5°C max	±0.5°C max
•	Temperature Coefficient: Span: 50ppm	°c		
	Offset: 0.01	learees/dearee		

#### NORMAL MODE REJECTION

 50dB at 50 - 60Hz (Additional capacitor filtering may be added between pins A and 4 with degradation of response time)

COMMON MODE REJECTION

 Floated on Power Supply: 120dB at 250V rms max CMV, dV<sub>cm</sub>/dt 10<sup>6</sup> V/sec max, 1kΩ Imbalance CONVERSION RATE

5 Conversion/sec
Hold and Read on Command

#### POWER INPUT

- AC Line 50 400Hz, see Voltage Options Below
- Power Consumption 5.8W @ 50 400Hz

#### ANALOG OUTPUTS

• ±12V dc ±10% @ 10mA (Referenced to Isolation Analog Grd.)

• +5V dc ±5% @ 30mA

Reference Voltage +6.4V ±1% (Referred to Analog Grd.) 25ppm/°C @ 50µA max output

#### DATA OUTPUTS

Isolated Parallel BCD Outputs • 3 BCD digits, overrange, overload outputs (TTL Compatible, 4 TTL Loads). BCD data outputs are latched positive true logic. Overrange output is Logic "1" for data display Louss), but not only and an interest position of the interesting on the probability of the probability of the interest of the probability of the p reference to digital ground.

Channel Address Outputs (CMOS/TTL Compatible 2 TTL Loads) - BCD Channel number data outputs are positive true

Mode Output (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" indicates channel selection is by switch. Logic "0" indicates selection is by scanner or external control, useful in Microcomputer Interface.

Data Ready (Data Ready) CMOS/TTL Compatible 2 TTL Loads) - Logic "1" ("0") indicates data from Scan Card is ready. Data remains valid until next clock pulse

Spare Inverter Output (CMOS/TTL Compatible 2 TTL Loads) - Spare inverter supplied for customer convenience.

Clock Out (CMOS/TTL Compatible, 2 TTL Loads) - Indicates EOC. When clock pulse is high, latches are being updated, data is invalid. Data is valid on negative going edge for 198ms. Clock Out pulse is disabled when Data Hold line is low.

ANALOG OUTPUT (P2 Pin A): 1mA max output

AD2037:  $V_0 = K V_{IN}$ 

Where K is gain of programmable input amplifier. (K = 1 for 1.999V F.S. and K = 10 for 199.9mV)

AD2038: V0 = (18.95mV/°C)T for T = °C  $V_0 = (10.53 \text{mV}/^{\circ}\text{F})(\text{T}-32) \text{ for } \text{T} = {}^{\circ}\text{F}$ error = ±6mV

#### NOTES

<sup>4</sup>Guaranteed at 200mV full scale at +25°C and nominal power supply. <sup>3</sup>Overall accuracy of meter plus sensor over entire sensor range (guaranteed max) Meter is factory cellibrated for ideal sensor.

is factory calibrated for ideal sensor. <sup>3</sup> Lens 22 (AD2038) Lens 28 (AD2037) supplied if no lens option is specificed. <sup>4</sup> Only one option may be specified.

Specifications subject to change without notice

#### CONTROL INPUTS

Display Blanking (TTL Compatible, 3 LSTTL Load) - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

Converter Hold (CMOS/TTL Compatible, 1 LSTTL Load) - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD are valid.

Decimal Points (Not TTL Compatible) - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle, when decimal point is illuminated. Data Hold (TTL Compatible, 1 TTL Load) - Logic "0" inhibits updating of latched parallel output data. Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on normal conversion of the DPM and its display.

Scanner Enable (CMOS/TTL Compatible 1 LSTTL Load) - Logic "1" will enable Scanner to control the channel selection. External channel input BCD lines can remain connected. A Logic "0" enables external channel selection.

<u>Scan (Scan)(CMOS/TTL Compatible; 1 LSTTL Load)</u> - A Logic "1" ("0") for <4 seconds will initiate a scan of six channels. To use Scan input, the Scan input must be a Logic "0". Both inputs have debounce circuitry. A momentary scan puble while in the writch or extremal mode will initiate a sequence of six a second s readings of the channel that is addressed then stop.

Channel Address Input (CMOS/TTL Compatible 1 LSTTL Load) - Logic "0" on Scanner Enable will allow use of external control. All other control inputs remain the same.

Channel Address Increment (CMOS/TTL Compatible 1 LSTTL Load) - Positive going edge will initiate sequence to the next channel.

Spare Inverter Input (CMOS/TTL Compatible 1 LSTTL Load) - Spare inverter supplied for customer convenience.

CALIBRATION ADJUSTMENTS

- Gain · Offset, Course
- · Offset, Fine
- Span/per Channel (AD2038 only)
- Recommended Recalibration Interval: Six Months

SIZE

3.92" x 1.67"H x 5.80"D (100 x 42 x 147mm)
 Panel Cutout 3.930" x 1.682" (99.8 x 42.7mm)

WEIGHT 1.25 pounds (0.563 kg)

OPTIONS<sup>3</sup>

- Lens: 28 Red with ADI Logo AD2037 Lens: 27 Red without ADI Logo
- Lens 22-1, Red °C with ADI Logo AD2038 Lens 22-1, Red C with ADI Logo Lens 22-2, Red °F with ADI Logo Lens 23-1, Red °C without ADI Logo Lens 23-2, Red °F without ADI Logo

CONNECTORS (2

2 each, 30 pin, 0.156" Spacing Card Edge Connector Viking 2Vk 15/1-2 or Equivalent Optional: Order AC1501



VOL. II, 16–38 DIGITAL PANEL INSTRUMENTS



## Low Cost Temperature Indicator

AD2040

#### FEATURES

Low Cost Direct Interface to AD590 or AC2626 Sensors Large 0.56" Red Orange LED Display Accuracy to  $\pm 1.0^{\circ} \pm 1$  Digit Either ac Line or +5V dc Powered Temperature Range: -55°C to +150°C -67°F to +302°F 1000V rms Isolation (ac)

Terminal Block Interface Small Size, Panel Mount

#### APPLICATIONS

Temperature Monitoring in Design, Laboratory, Manufacturing and Quality Control for Both +5V dc or Line Powered Applications



The AD2040 is a low-cost 3 digit temperature indicator. Based on the highly successful AD2026 low-cost DPM and designed to be used in conjunction with Analog Devices' AC2626 general purpose probe or the AD590 temperature transducer, the AD2040 is available in both 5V logic-powered, or ac linepowered versions.

The 5V powered AD2040-12 reads out directly in  $^{\circ}$ C,  $^{\circ}$ F,  $^{\circ}$ R or K. A precision voltage reference, resistor network, and span and zero adjusts, needed to implement display of the different temperature scales, are all self-contained. User selectable degree readout, as well as all other connections, i.e., +5V power and sensor or probe interface, are all made via a terminal block on the rear.

For many stand-alone temperature measurement applications, i.e., in factories, labs, ovens, inspection stations, etc., +5V dc power is not available. For these applications, the AD2040 is available in an ac version. The ac-powered version retains all of the features of the 5V version, with the exception of the user selectable degree readout. °C or °F must be specified when ordering (see Ordering Guide).

If required, calibration adjustments are easily accessible. No mounting hardware of any kind is used.

The AD2040 and AC2626 or AD590 will measure and display temperatures on large 0.56" orange LED displays from  $-55^{\circ}$ C to  $+150^{\circ}$ C ( $-67^{\circ}$ F to  $+302^{\circ}$ F) with accuracy to  $\pm 1.0^{\circ} \pm 1$  digit. Reliability is assured with the inherent simplicity and accuracy of the sensor, combined with the highly efficient design of the AD2040.

#### THE SENSOR

The AD590 is a laser-calibrated, two terminal IC temperature



transducer. Its output is a current  $(1\mu A \text{ per } K)$  linearly proportional to absolute temperature, thus eliminating the need for costly linearization and cold junction compensation.

Due to the AD590's high impedance current output, it is insensitive to voltage drops over long lines thus enabling remote monitoring with no need for costly transmitters or special wire.



#### AD2040-12 (dc) Block Diagram

Above is a block diagram of the AD2040-12, showing the AD2026 DPM input, the current-to-voltage conversion resistors (R1, R2, R3), the offsetting resistance network (R4, R5, R6, R7), and the connections to the terminal strip. Attenuated voltage from the AD580, 2.5V reference, provides the offsets for readout on the °F and °C scales. On the AD2040-12 dc version, jumpers are connected by the user at the terminal strip to select the appropriate units of temperature for display. °C or °F must be specified when ordering the ac version (see Ordering Guide).

6

## **SPECIFICATIONS** (typical @ +25°C and nominal supply unless otherwise specified)

<ul> <li>ACCURACY</li> <li>Resolution: 1°</li> <li>Range: -55°C to +150°C -67°F to 302°F 218K to 423K 425°R to 793°R</li> <li>Accuracy: (±1 digit)<sup>1</sup> Calibration Error @ +25°C Absolute Error (overrated performance temperature range) Without External Calibration Adjustment With +25°C Calibration Error Set to Zero Nonlinearity</li> <li>Temperature Coefficient: Offset: 0.03 degrees/degree Span: 70ppm/°C</li> <li>Common Mode Rejection (ac) 117dB, 1000V rms max Common Mode Voltage</li> <li>Normal Mode Rejection 30dB @ 50-60Hz</li> </ul>	AC2626J/ AD590J ±5.0°C max ±10.0°C max ±3.0°C ±1.5°C	AC2626K/ AD590K ±2.5°C max ±5.5°C max ±2.0°C max ±0.8°C max	AC2626L/ AD590L ±1.0°C max ±3.0°C max ±1.6°C max ±0.4°C max	· • •
DISPLAY OUTPUT <sup>2</sup> • 7 Segment, Red Orange, LED 0.56" (13mm) High	POWER INPU • AC Line	T (ac Line Pov Power, 50-60	wer) Hz, 1.5 Watts	- · · · · · · · · · · · · · · · · · · ·
<ul> <li>for 3 Data Digits</li> <li>Sensor Disconnect Indication: (for °C and °F only)</li> <li>DPM Positive Overload: EEE</li> <li>DPM Negative Overload:</li> <li>No Indication of Out of Sensor Range</li> </ul>	CALIBRATIC • Span • Zero • Recomm	N ADJUSTM G Onended Recalit	ENTS ain Offset pration Interval: S	iix Months
INPUT IMPEDANCE • °C, K: 1.0KΩ • °F, °C: 1.8KΩ	SIZE • 3.43"W • Panel Ca (80.6	X 2.0"H X 1.6 1tout Required 5 ±0.38 X 45.	55"D (87 × 52 × 4 1: 3.175 ±0.015" 97 ±0.38mm)	42mm) X 1.810 ±0.015"
CONVERSION RATE  4 Conversions Per Second  POWER INPUT	WEIGHT • 3 ounce • 7 ounce	s (88 grams) (4	+5V dc) (ac Line Powered	)
• +5.0V $\pm 5\%$ ; 160mA (dc version) • AC Line 50-400Hz; See Voltage Options Below ORDERING GUIDE POWER INPUT +5V dc 1 90-129V ac 2 198-264V ac 3 DEGREE READOUT <sup>3</sup> °C 1 °F 2 AC2626 AC2626 - AC266 - AC2626 - AC2626 - AC266 - A	NOTES <sup>1</sup> Overall accura <sup>3</sup> Leading zero of <sup>3</sup> Select Degree version offers For +5V dc ve Specifications s	cy of meter plus annot be blanko Readout when c user selectable to rsion enter 2, e.g ubject to change	s sensor over entire ed. ordering ac version o emperature scales—so g., AD2040-12.) without notice.	range. only. (+5V de ee Table I.
$\begin{array}{c} \\ \text{LENGTH} \\ 6 \end{array} \right\} - \text{ENTER} - $				

B

ss∫

AC2629 -

ENTER

AC2629

BRASS

**TYPE 316** 

STAINLESS



Figure 1. Manual Switching with Multiple Inputs

#### MULTIPLE SENSOR INPUTS

Expansion to multiple sensors via manual switching is shown in Figure 1. The sensor selected will pass a signal current through the current measuring circuitry, internal to the AD2040. Similarly automatic switching, shown in Figure 2 is accomplished. A low level input on an inverter input will allow selection of the appropriate AD590.



\*TERMINAL 5 IS -SENSOR INPUT ON THE +5V DC VERSION. THIS TERMINAL IS TERMINAL #2 ON THE AC VERSION.

Figure 2. Automatic Switching

SCALE	TERMINAL 2	TERMINAL 3	TERMINAL 4	TERMINAL 9
°C	x	×	x	
°F				
к		x	x	x
°R		x		x

Table I. Temperature Scale Selection (+5V dc Only)

#### **TEMPERATURE SCALE SELECTION**

As shown in Table I any of the standard temperature scales may be displayed using the +5V dc AD2040-12.

The AD2040-12dc version is factory calibrated in degrees Fahrenheit. Readout in degrees Celsius, Rankine or Kelvin are achieved via simple jumper connections on the terminal block, listed in the above table. (Connect terminals marked X.)

Figure 3 shows how the AD2040, in conjunction with 4 resistors, 2 trim pots, and a dual comparator, can be used to control as well as monitor particular applications via high and low set points. When the voltage at the AD2040 sense terminal (terminal 5) goes higher than the Hi Limit Set Voltage, the



Figure 3. Hi and Low Set Points

output of A1 goes low and D1 is illuminated. Similarly when the voltage at terminal 5 goes below the Lo Limit Set Voltage, the output of A2 goes low illuminating D2.

To set the high limit, replace the AD590 with a variable resistor. Adjust the resistor until the desired high temperature set point is displayed on the meter. Adjust R1 until D1 is just turning on. Repeat procedure for R2 (Lo Limit Set).

#### CALIBRATION PROCEDURE

The AD2040 is factory calibrated using an ideal sensor. The dc version is calibrated in  $^{\circ}$ F and the ac version is calibrated to order. If sensor accuracy is adequate, no calibration is required (see note). If a lower grade sensor is used (i.e., J) and calibration is required, adjust Span Adjust on the rear with sensor at a known temperature for that temperature, e.g. for  $^{\circ}$ F place sensor in Ice Bath at 32 $^{\circ}$ F and adjust span for reading of 32.

Recalibration may be required after six (6) months; if so, proceed as follows:

- 1. With AD590 disconnected, short input of AD2040 (terminal 5 to 9 on dc version, or 2 to 3 on ac version). Remove AD2040 lens and adjust Front Panel ZERO Adjust to display 000.
- Attach AD590 sensor and stabilize at a known Reference Temperature; e.g., Ice Bath. Connect terminal 9 to terminal 3 (on dc version) or terminal 3 to access port (on ac version) and adjust Rear SPAN Adjust for a display of 273 plus Reference Temperature for °C or 460 plus Reference Temperature for °F.
- 3. Remove jumper between terminals 9 and 3 (dc version) or 3 and access port (ac version). Adjust the Rear OFFSET Adjust for Reference Temperature. (For K or °R omit step 3.)

For optimum linearity calibration for  $^{\circ}$ C, repeat steps two (2) and three (3) with Reference Temperature at 0. Then with sensor at 100 $^{\circ}$ C adjust Front Panel <u>GAIN</u> Adjust for a meter display of 100. Other high end temperatures may be used with this procedure as long as they are known to be accurate.

For °F repeat steps two and three with Reference Temperature at 32°F. Then with sensor at the high temperature, adjust Front Panel <u>GAIN</u> Adjust for readout equal to high temperature. The above temperature can be selected for optimum linearity over user's temperature range.

NOTE: If other than °F readout on the dc version is desired, follow step 2 and 3 of Recalibration Procedure.

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#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



#### **THE AC2626**

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the new AD590F, the probe is available in linearity grades of 0.4°C, 0.8°C or 1.5°C.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AD2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.



The AD590 temperature transducer is available in two packages-the "H" package (TO-52) and the "F" package (ceramic







## Microprocessor Based Thermocouple Meters

## AD2050/AD2051

#### FEATURES

Automatic Self-Calibration for Gain, Offset, Cold Junction Compensation and Thermocouple Linearization

J, K, T, E, R, S Thermocouple Selections (AD2050) Universal Meter (AD2051), User Programmable Character Serial ASCII Digital Output Optional Linearized Analog Output: 1mV/degree Optional Isolated 20mA Loop/TTL Serial Outputs Meets DIN/NEMA Dimension Specifications Temperature Ranges: -265°F to +1999°F -165°C to +1760°C

Power Options: 120V ac, 240V ac, +7.5V dc to +28V dc APPLICATIONS

Temperature Monitoring in Laboratory, Manufacturing, and Quality Control Environments Process Control Temperature Measurements

**Remote Data Logging** 

#### **GENERAL DESCRIPTION**

The AD2050 and AD2051 are high performance single channel  $3\frac{1}{2}$  digit thermocouple meters that can measure temperatures accurately between -265 and +1999 in degrees Celsius or Fahrenheit. The AD2050 is supplied factory programmed to interface directly with any of the following six thermocouple types: J, K, T, E, R and S. The AD2051 is a universal instrument in which the user selects one of the six thermocouple types via switch programming. Being microprocessor based, all gain and offset error correction, cold junction compensation, thermocouple linearization, and °C/°F scaling are automatically performed in firmware.

The AD2050 and AD2051 display temperature information on large 0.56" (14.3mm) high LEDs. Digital information is provided in standard ASCII character serial format with rate selection for easy interface to printers, terminals, and other peripherals. For remote data acquisition applications, an optional isolated 20mA



serial loop/TTL compatible interface is available. Also an optional analog output linearized to 1mV/degree is provided for driving recorders and other analog instruments. Selection of °C or °F scaling is accessed by removing the front panel lens and setting the selector switch to its proper position.

The AD2050 and AD2051 can also be ordered with any of the following power versions: 120V ac, 240V ac, or +7.5V dc to +28V dc. Input overvoltage protection for 300V peak (thermocouple to ac line shorts) and common mode voltages as high as 1400V peak (ac version) with overrange and open thermocouple detection are provided. These instruments are rated for operation over the  $+10^{\circ}$ C to  $+40^{\circ}$ C temperature range. Testing is performed per MIL-STD-202E Method 103B to insure specified operation over various relative humidity conditions. The AD2050 and AD2051 are supplied in rugged high impact plastic cases that meet DIN/NEMA standard dimensions.



Figure 1. AD2050 & AD2051 Functional Block Diagram

## **SPECIFICATIONS** (typical @ + 25°C and rated supply voltages unless otherwise specified)

#### THERMOCOUPLE INPUTS

- Thermocouple Types: J, K, T, E, S, R
- Input Impedance: >100MΩ
- $\bullet\,$  External (Lead) Resistance Effect:  ${<}20\mu V$  per 350 $\Omega$  of Lead Resistance
- Cold Junction Compensation Error:  $\pm 0.5^{\circ}$ C max (10°C to  $+ 40^{\circ}$ C)
- Open Thermocouple: + EEE Display; + EEEE ASCII Digital Output; + 2.048V Analog Output
- Thermocouple Short to ac Line: Internal Protection Provided to 300V peak (200V ac rms)
- Common Mode Voltage: 1400V peak (dc or ac), between Input and Power Line Ground (ac Versions)
- Common Mode Rejection Ratio: >130dB with 250Ω Source Imbalance (ac Versions); (dc to 60Hz)
- Normal Mode Rejection Ratio: >80dB @ 50/60Hz
- DIGITALOUTPUTS
  - Character Serial ASCII
    - Data: Nine transmitted characters, (each 7 bits plus strobe) Drive Capability: 2TTL loads, CMOS/TTL compatible Strobe: Negative transition determines when character serial data is valid. CMOS/TTL compatible. Character Rate: Selectable on J1 (pin 32) Grounded: 25 characters/sec. (SLOW) Open: 100 characters/sec. (FAST)
  - Isolated Serial Output (Optional) Data: Asynchronous ASCII 20mA current loop (Optically isolated to ± 600V peak) Baud Rate: Selectable on J1 (Pin 32) Grounded: 300 baud (SLOW) Open: 1200 baud (FAST) Distance: 10,000 ft. max
  - Serial Output (Nonisolated, Optional) Data: Serial ASCII
     Drive Capability: 2TTL Loads, CMOS/TTL compatible
     Baud Rate: (same as Isolated Serial Output)
  - Overrange: ± EEEE
  - Minimum Time Between New Data Update: 150ms

DIGITALINPUTS

- REQ: Low-Level Triggered: Must go low at any time other than during data transmission to be recognized. REQ line taken low during data transmission will not be acknowledged and the ASCII digital output transmission will not occur. Display readings are not effected by REQ.
   SERIAL INPUT (Optional): Edge Triggered, Current On to
- SERIAL INPUT (Optional): Edge Triggered, Current On to Current Off: Must be triggered at any time other than during data transmission to be recognized. Serial Input triggered during data transmission will not be acknowledged and the 20mA isolated/TTL compatible serial output transmission will not occur. Display readings are not effected by Serial Input.

ANALOGOUTPUT (OPTIONAL)

- Voltage: 1mV/degree, linearized
- Current: ±2mA max drive
- CMV: 1400V peak (ac or dc) Peak between Analog Output Ground & ac Power Line Ground
- Overrange: +2.048V, -0.512V

ACCURACY

- Temperature Resolution: 1°C/1°F
- All Ranges are Guaranteed Monotonic
- Range Temperature Coefficient: ±25ppm/°C typ, ±60ppm/ °C max
- Readout Accuracy @25°C:

Sensor	
Type	

уре	Range	Accu	racy
J	- 165°C to 760°C	±0.7°C	±1/2LSD
J	- 265°F to 1400°F	±1.3°F	±1/2LSD
K	- 50°C to 1250°C	±0.9°C	± 1/2LSD
K	- 58°F to 1999°F	±1.6°F	± 1/2LSD
Т	150°C to 400°C	±0.8°C	± 1/2LSD
Т	- 238°F to 752°F	±1.4°F	± 1/2LSD
Ε	- 100°C to 870°C	±1.0°C	± 1/2LSD
Ε	- 148°F to 1598°F	± 2.0°F	± 1/2LSD
S,R	+ 300°C to 1760°C	±1.5°C	± 1/2LSD
	0° to 299°C	±6.0°C	± 1/2LSD
S,R	+ 572°F to 1999°F	± 3.0°F	± 1/2LSD
-	+ 32°F to 571°F	±12.0°F	±1/2LSD

ANALOG TO DIGITAL CONVERSION

- Technique: Offset Dual Slope with Gain and Offset Error Correction
- Rate: 2.5 Conversions/Second Typical

- Input Integration Period: 100ms for 50/60Hz Noise Rejection
- POWER REQUIREMENTS (Choice of Three Supply Ranges)
  ac: 90V ac to 132V ac (a 25mA (47Hz to 500Hz)
  - 198V ac to 264V ac (*u* 12.5mA (47Hz to 500Hz) ● dc: +7.5V to +15V dc (*u* 200mA (Protected Against Supply Reversals)

DISPLAY

- Type: Seven Segment Orange LED 0.56" (14.3mm) high
- Polarity Indication: "+" or "-" displayed
- Overrange Indication: ± EEE
  - Display Test: At Power Turn-On, 3 Second Display of "+ 1888" Tests all Segments of Display
- ENVIRONMENTAL
  - Rated Temperature Range: +10°C to +40°C
  - Operating Temperature Range: -10°C to +50°C
  - Storage Temperature Range: -40°C to +85°C
- Relative Humidity: Meets MIL-STD-202E, Method 103B DIMENSIONS
  - Case: 3.78" × 1.89" × 5.13" (96.8mm × 48.9mm × 131.3mm), high impact molded plastic case. DIN/NEMA Standard
  - Weight: 15.2 oz (431 grams) max, ac powered 12.0 oz (341 grams) max, dc powered

RELIABILITY

- Burn In: 168 Hours at +50°C and Power ON/OFF Cycles.
- Calibration: NBS Traceable
- Recalibration: Recommended 15-Month Intervals
- Warranty: 12 months
- CONNECTOR

ORDERING GUIDE

One 44 pin 0.1" (2.54mm) spacing card edge connector Viking 3VH22/1 JN5 or equivalent Optional: Order AC2630



Figure 2. Rear Panel View

AD2051 /\_\_\_ AD2050 THERMOCOUPLE TYPE\* ĸ Т ENTER Е ٠R s POWER OPTION\* (1)120V ac (2) 240V ac ENTER (3) + 7.5V dc to + 15V dcANALOG OUTPUT OPTION (A) Contains Analog Output ENTER (Blank) Does Not Contain Analog Output SERIAL OUTPUT OPTION (S) Contains Serial Output ENTER (Blank) Does Not Contain Serial Output

\*Only one option can be ordered. The thermocouple type does not need to be specified when ordering the AD2051 since it is user programmable. Specifications subject to change without notice.

# 

## Microprocessor Based Autoranging RTD/Thermistor Meter

## AD2060/AD2061

#### FEATURES

Temperature Ranges: -328°F to +1562°F -200°C to +850°C

Autoranging: 0.1° from – 199.9° to + 199.9°; 1°≥200° Sensor Selection (AD2060): RTD 100Ω Platinum

 $\alpha\!=\!0.00385,\,0.00390,\,0.00392$  or 2252 $\Omega$  Thermistor Universal Meter (AD2061) Sensor User Programmable Switch Selectable Sensor Configuration: 2, 3 or 4-wire 7-Bit ASCII Character Serial Data Output

Automatic Self-Calibration for Gain, Offset, Excitation and Sensor Linearization

Optional Linearized Analog Voltage Output: 1mV/degree

**Optional Isolated 20mA ASCII Loop/TTL Serial Outputs** 

#### APPLICATIONS

Temperature Monitoring in Laboratory, Manufacturing and Quality Control Environments

Process Control Temperature Measurements Remote Data Logging

#### **GENERAL DESCRIPTION**

The AD2060/AD2061 are high performance single channel  $3\frac{1}{2}$  digit RTD/Thermistor meters that can measure temperature accurately between  $-328^{\circ}$ F and  $+1562^{\circ}$ F ( $-200^{\circ}$ C and  $+850^{\circ}$ C), Both meters offer autoranging from  $0.1^{\circ}$ C/F to  $1^{\circ}$ C/F. The AD2060 is supplied factory programmed for one of four sensor types:  $100\Omega$  Platinum RTDs:  $\alpha = 0.00385$ , 0.00390, 0.00392 or a 2252 $\Omega$  Thermistor. The AD2061 is a universal meter in which the user selects one of the four sensor types via switch programming. The microprocessor based AD2060/AD2061 provides gain, offset and excitation error correction, linearization and °C/°F scaling in firmware. The AD2060/AD2061 display temperature information on large  $0.56^{\circ}$ (14.3mm) high LEDs. Digital information is provided in 7-bit standard ASCII character serial



format with baud rate selection for easy interface to printers, terminals and other peripherals. For remote data acquisition applications, an optional isolated 2-wire 20mA ASCII serial loop/TTL compatible interface is available. For driving recorders or other analog instruments, an optional linearized analog voltage output of ImV/degree is available. Selection of °C or °F scaling is accessed by removing the front panel lens and setting the selector switch to its proper position.

The AD2060/AD2061 can be ordered in one of the following power versions: 120V ac, 240V ac or +7.5V dc to +28.0V dc. Input voltage protection of 180V peak (RTD short to ac line), common-mode voltage to 1400V peak (ac version) with overrange and open sensor detection is provided. These meters are rated for operation over the 0 to  $+40^{\circ}$ C temperature range. Each AD2060/AD2061 is burned-in for 168 hours @ 50°C with on/off power cycles for increased reliability. The AD2060/AD2061 are supplied in rugged molded plastic cases that meet UL94V-0 and DIN/NEMA standard dimensions.

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Figure 1. AD2060 & AD2061 Functional Block Diagram

## SPECIFICATIONS (typical @ + 25°C and rated supply voltages unless otherwise specified)

#### RTD INPUTS

#### • RTD Types:

$\alpha = 0.00385$ (Per DIN 437)	50)
0.00100	

 $\alpha = 0.00392$ 

1000 Platin

- Configuration: 2, 3 or 4 Wire
- Excitation Current: 0.25mA nominal
- External Lead
- Resistance Effect: Automatically Compensated for 3 & 4 wire configurations Lead Resistance:  $50\Omega/Lead$  max; RTD + Lead Resistance must be less than  $400\Omega$
- 3 Wire Error: 2.8°C/Ω of impedance imbalance
- Open Sensor: DISPLAY + EEE
- RTD Short to ac Line: Internal protection provided to 180V peak (130V rms)
- Maximum Common-Mode Voltage: 1400V peak (ac or dc) between input and power line ground (ac version)
- · Common-Mode Rejection Ratio: 100dB ac power to RTD input
- Normal Mode Rejection: 60dB @ 50/60Hz

#### THERMISTOR INPUTS

- Thermistor Type: Series 400 R = 2252Ω
- Configuration: 2 Wire
- Open Sensor: DISPLAY -EEE

ACCURACY

- Temperature Resolution: Autoranging (0.1° from 199.9° to + 199.9°, 1°≥200°)
- All Ranges Guaranteed Monotonic
- Range Temperature Coefficient: 20ppm/°C typ, 30ppm/°C max

٠	Readout	Accuracy*	@	+25℃	
---	---------	-----------	---	------	--

Sensor	Range	Accuracy
$100\Omega RTD \alpha = 0.00385$	- 200°C to + 850°C	±0.3°C ± 1/2LSD
	- 328°F to + 1562°F	$\pm 0.6^{\circ}F \pm 1/2LSD$
$100\Omega RTD \alpha = 0.00392$	- 200°C to + 640°C	±0.3°C ± 1/2LSD
	- 328°F to + 1184°F	± 0.6°F ± 1/2LSD
$100\Omega RTD \alpha = 0.00390$	- 200°C to + 640°C	±0.3°C±1/2LSD
	- 328°F to + 1184°F	±0.6°F ± 1/2LSD
Thermistor $R = 2252\Omega$	- 30°C to + 100°C	±0.4°C±1/2LSD
	- 22°F to + 212°F	$\pm 0.8^{\circ}F \pm 1/2LSD$

\*Readout Accuracy: Includes Gain and Offset Errors. Recommended Recalibration Interval 15-MONTHS.

#### DIGITAL OUTPUTS

- Character Serial ASCII
  - Data: Eleven transmitted characters, (each 7 bits plus strobe)
- Drive Capability: 2TTL loads, CMOS/TTL compatible Strobe: Negative transition determines when character serial data is valid. CMOS/TTL compatible.

Character Rate: Selectable on P1 (Pin 32) Grounded: 25 characters/sec. (SLOW)

- Open: 100 characters/sec. (FAST)
- Isolated Serial Output (Optional) Data: Asynchronous ASCII 20mA current loop (Optically isolated to ±600V peak) Baud Rate: Selectable on J1 (Pin 32) Grounded: 300 baud (SLOW)
- Open: 1200 baud (FAST)
- Distance: 10,000 ft. max
- Nonisolated Serial Output (Optional) Data: Serial ASCII

Drive Capability: 2TTL Loads, CMOS/TTL compatible Baud Rate: (same as Isolated Serial Output)

- Overrange: ± EEE.E
- · Minimum Time Between New Data Update: 150ms

#### DIGITAL INPUTS

- REQ: Low-Level Triggered: Must go low at any time other than during data transmission to be recognized. REQ line taken low during data transmission will not be acknowledged and the ASCII digital output transmission will not occur. Display readings are not effected by REQ.
- SERIAL INPUT (Optional): Edge Triggered, Current On to Current Off: Must be triggered at any time other than during data transmission to be recognized. Serial Input triggered during data transmission will not be acknowledged and the 20mA isolated/TTL compatible serial output transmission will not occur. Display readings are not effected by Serial Input.

#### ANALOG OUTPUT (OPTIONAL)

- Voltage: 1mV/degree, linearized
- Current: ± 2mA max drive
- CMV: 1400V peak (ac or dc) between Analog Output Ground & ac Power Line Ground
- Overrange: +2.048V, -0.512V
- Accuracy: ±2mV from Display Reading

Specifications subject to change without notice.

ANALOG TO DIGITAL CONVERSION

- Technique: Offset Dual Slope with Gain and Offset Error Correction
- Rate: 2.5 Conversions/Second Typical
- Input Integration Period: 100ms for 50/60Hz Noise Rejection
- POWER REQUIREMENTS (Choice of Three Supply Ranges)
  - ac: 90V ac to 132V ac @ 25mA (47Hz to 500Hz)
    - 198V ac to 264V ac @ 12.5mA (47Hz to 500Hz)
  - dc: +7.5V to +28V dc @ 200mA (Protected Against Supply Reversals)

#### DISPLAY

- Type: Seven Segment Orange LED 0.56' (14.3mm) high Polarity Indication: "+" or "--" displayed
- Overrange Indication: ± EEE
- Display Test: At Power Turn-On, 3 Second Display of "+188.8." Tests all Segments of Display

#### ENVIRONMENTAL

- Rated Temperature Range: 0 to +40°C
- Operating Temperature Range: -10°C to +50°C
- Storage Temperature Range: -40°C to +85°C
- Relative Humidity: Meets MIL-STD-202E, Method 103B (0 to 90%, Noncondensing)
- DIMENSIONS
  - Case: 3.78" × 1.89" × 5.13" (96.8mm × 48.9mm × 131.3mm), rugged molded
  - plastic case. Meets UL94V-0 and DIN/NEMA Standard dimensions • Weight: 15.2 oz (431 grams) max, ac powered
  - 12.0 oz (341 grams) max, dc powered.

#### RELIABILITY

- MTBF: >55,000 hours calculated
- Burn In: 168 Hours at +50°C and Power ON/OFF Cycles.
- Calibration: NBS Traceable
- Recalibration: Recommended 15-Month Intervals
- Warranty: 12 months

#### CONNECTOR

One 44 pin 0.1" (2.54mm) spacing card edge connector Viking 3VH22/1 JN5 or equivalent

Optional: Order AC2630



Figure 2. Rear Panel View



\*Only one option can be ordered. The sensor type does not need to be specified when ordering the AD2061 since it is user programmable.

## **Microcomputer Analog I/O Subsystems**

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## Selection Guide Microcomputer Analog I/O Subsystems

Analog Devices Real-Time Interface (RTI) products provide a direct memory-mapped interface between popular microcomputers and analog input and output signals. Each RTI board is electrically and mechanically compatible with the bus it is designed to interface with. No additional interface logic or power are required for the board, which plugs directly into the microcomputer card cage.

As the Selection Guide indicates, there are Input-only, Outputonly, and—in most cases—Input/Output cards available for each bus type. Within each card family, there are optional features available to provide a close fit to the individual user's application. For STD-bus users, there is a "smart" subsystem, the A/D-CPU Base Card and RTI-1271 Signal-Conditioning Cards. Included are sensor signal conditioning and on-board intelligence to perform scaling, linearization, and conversion to engineering units for up to 16 channels of low- or high-level analog input.

The Selection Guide provides selection information in capsule form, permitting card types to be matched to desired features. Additional information and complete specifications are provided on the individual card or family data sheets.

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FEATURE SELECTION CHART												
				VMEb MOTORC GNETICS MOSTEK	DLA N	MICROCOMPUTER BUS COM MULTIBUS <sup>TM</sup> (IEEE-796) INTEL NATIONAL				STD BUS PRO-LOG MOSTEK		
		FILES	a line	en la		at and	5 × 14	R. 1.25	Scitt.	R11.	\$1.1.00	e /
Board Type	Input Input/Output Output			• • •	•	•	•	•	•	•	an ann	
Channel Capacity	Input (Single ended/ differential) Output	32/16	4	32/16	4	32/16 2	16/8	16/8 2	32/16	4	16/16	
Input Resolution	10 Bits 12 Bits			•		•	•	•	•		•	
Output Resolution	8 Bits 12 Bits	Constant Con	•		•	•		•		•		
Additional Feature: DC/DC Converte Software PGA Gains of 1, 2, Resistor PGA Gains of 1 to 4-20mA Output Digital Output D Direct Sensor In	s er 4, 8V/V 1000V/V Privers terface TD	100 C	•	•	•		•	•	•	•	•	
Volume II Page	cs, K1Ds	17-5	17-5	17-7	17-7	17-7	17-9	17-9	17-17	17-17	17-19	

NOTES

<sup>1</sup> RTI-1200, 1201 and 1202 I/O boards not listed, but still available.

<sup>2</sup> This product includes sensor signal conditioning and on-board intelligence to perform scaling, linearization and conversion

to engineering units.

Shading indicates new product since publication

of 1982-1983 Databook Update.



μCOMPUTER ANALOG I/O SUBSYSTEMS VOL. II, 17-3

#### VOL. ΙΙ, 17–4 μCOMPUTER ANALOG Ι/Ο SUBSYSTEMS

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#### FEATURES

RTI-600 ANALOG INPUT BOARD 32SE/16D Input Channels User Configurable Gains of 1 to 1000 12-Bit A/D Resolution (AD574)

RTI-602 ANALOG OUTPUT BOARD 4 Analog Output Channels 12-Bit D/A Resolution (AD7541) Optional 4-20mA Output

#### GENERAL

#### Low Cost

Compatible with All VME Microcomputers Interfaces through Primary Connector (P1) Memory Mapped into VME Short I/O Address Space Single Eurocard Format (100 × 160mm) Single +5V Power Requirement 0 to +70°C Temperature Range

#### GENERAL DESCRIPTION

The RTI-600 Series products from Analog Devices are high performance analog input and output boards compatible with the VMEbus. They provide a cost effective and convenient means of interfacing your microcomputer to the real (i.e., analog) world. The boards feature 12-bit resolution, programmable gain for low-level signals, analog channel expansion, 4-20mA outputs, and on-board dc/dc converter.

The series consists of an analog input board (RTI-600) and an analog output board (RTI-602); each of which interfaces to the VMEbus P1 connector, as a block of contiguous address locations (memory mapped interface) in the VMEbus short I/O address space.

The RTI-600 Analog Input Board provides data acquisition for 16 single-ended or 8 differential channels with optional expansion to 32 single-ended or 16 differential. The instrumentation amplifier is user configurable for gains of 1 to 1000. Combining this with a sample-hold circuit and 12-bit A/D converter, the data acquisition section features  $\pm 0.01\%$  accuracy, 12-bit resolution and conversion rates up to 25kHz. The RTI-602 Analog Output Board uses four, 12-bit D/A converters to provide independently programmed voltage output channels. In addition, two channels can be configured for 4-20mA outputs by using optional voltage to current converters which install on the board.

## Low Cost VMEbus Compatible Analog I/O Boards RTI-600 Series



Analog signal connections are made using reliable socket and header connectors which enables flat ribbon cable to be combined with gas tight and corrosion resistant connectors. An optional screw termination panel is also offered for simple and convenient field wire connections.

All boards are single height  $(100 \times 160 \text{ mm})$ , require +5V power and have an operating temperature range of 0 to +70°C.

#### **OPTIONAL SIGNAL CONDITIONING**

For low-level analog signal conditioning such as sensor-based applications, Analog Devices 3B Series Signal Conditioning I/O Subsystem offers rail-mounted industrial hardened analog signal interface modules with a single channel format and high level analog output. Optional sensor signal conditioning, transformer isolation of  $\pm$  1500V, high common-mode and normal-mode noise rejection and 130V input protection makes the 3B series an ideal for analog input and output signal conditioning for the RTI-600 series.

Whether you require sensor signal conditioning, analog I/O boards or both, Analog Devices is the source of the widest selection of solution for any measurement and control application control application. They are key elements in factory automation, process control, laboratory applications as well as OEM usages.

				INPUT			OUTPUT	
-	,	Channel C	Capacity		A/D		D/A	4-20mA
Card Type	Model No.	STD	ОРТ	Gain Range	Resolution	Channel Capacity	Resolution	(OPT)
Analog Input Analog Output	RTI-600 RTI-602	16SE/8D	32SE/16D	1-1000 N/A	· 12 Bits	4	N/A ——— 12 Bits	2

RTI-600/602 Function Chart

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

## **SPECIFICATIONS** (typical @ +25°C with nominal supply voltage unless otherwise noted)

RTI-600 ANALOG INPUT CARD	
Number of Input Channels	16 Single-Ended or 8 Differential (Jumper Selectable)
	Expandable to 32 Single-Ended or 16 Differential using
	two plug-in multiplexers (ADI Part #OA10)
Input Overvoltage Protection	± 35V (Dielectrically Isolated)
Input Impedance	>10°11
Input Current	± 50nA
Analog Connector	SUpin IDE
A/D Input Kanges <sup>-</sup>	$0.00 \pm 10^{\circ}$ , $\pm 10^{\circ}$
A/D Resolution	12 Bits (4090 Counts) Binary Officet Binary Two's Complement
A/D Output Codes	1 to 1000V/V (Resistor Programmable Gain)
Instrumentation Amplifier Gam Ranges	Tto Tooov/v (Resistor Programmable Gam)
Gain Equation	$G = 1 + \frac{20k\Omega}{M}$
A/D Conversion Time	$\frac{C-1}{25us}$ R <sub>G</sub>
System Throughput <sup>3</sup>	25.000 Channels/sec (G<150)
	20.000 Channels/sec (150 <g>300)</g>
	11,000 Channels/sec $(G = 1000)$
Common Mode Voltage (CMV)	$\pm 10V \min$
Common Mode Rejection (CMR)	78dB
Linearity	$\pm 1/2$ LSB
Differential Nonlinearity	± 1LSB
Total System Errors	$\pm 0.01\%$ of FSR (G = 1 to 10)
	$\pm 0.05\%$ of FSR (G = 100)
	$\pm 0.1\% \text{ of FSR}$ (G = 1000)
Temperature Coefficient	
Gain	$\pm 30$ ppm/°C of FSR (G = 1)
Offset	$\pm 100$ ppm/°C FSR (G = 1000)
	$\pm 10$ ppm/°C FSR (G = 1)
	$\pm 100$ ppm/°C of FSR (G = 1000)
RTI-602 ANALOG OUTPUT CARD	
Number of Output Channels	4
D/A Resolution	12 Bits (4096 Counts)
D/A Input Codes <sup>2</sup>	Binary, Offset Binary
Output Voltage Range <sup>2</sup>	$0V \text{ to } + 5V, 0V \text{ to } + 10V, \pm 5V, \pm 10V @ 5mA$
Output Current Range*	4-20mA using 2 V/I converters
(Optional-2 Channels Only)	(ADI Part #OA08)
Analog Connector	26 pin IDE
Nonlinearity	± 1/2L5B
Differential Nonlinearity	$\pm 1/2LSB$
Coin Enger (Adjustable to Zero)	$25\mu s(to \pm 1/2LSB)$ + 0.01% of ESP
Offect Error (Adjustable to Zero)	± 0.01% of FSR
Temperature Coefficient	- 0.02 /001 F 3N
Gain	+ 15ppm/°C of ESR
Offset	+ 2511 V/C
IN I EKFACE PAKAMETERS	Manage II also second and a second second State State State
	Meets an electrical and mechanical VMEbus specifications
Implementation	memory mapped I/O, compatible with all CPU types
Address Selection	2 continuous hutes in a 256 hute block (Tumper calestable !-
K11-000	the VM Fbus short I/O space)
RTI-602	and visitious short in a 256 bute block (Tumper selectable in
1711-072	the VMF hus short I/O space)
BOWER BROUDER (D) TO	and the mail and the space i
POWER REQUIREMENTS	
K11-600	$+5V \pm 5\%$ @ 650mA typ, 700mA max
K11-602	$+$ 5V $\pm$ 5% ( $\oplus$ 550mA typ, 650mA max
	(on-board dc/dc converter generates an isolated
	$\pm$ 15 v to power the data acquisition components.)
TEMPERATURE	
Operating	0 to + 70°C
Storage	- 55°C to + 85°C
<b>RELATIVE HUMIDITY</b>	Meets or exceeds MIL-STD 202 Method 103
NOTES	

NOTES <sup>1</sup>Specified with power applied, ± 20V with power off. <sup>2</sup>User selectable with wire-wrap jumpers. <sup>3</sup>Does not include CPU latency time. Throughput = multiplexer + amplifier settling time + A/D conversion time. <sup>4</sup>Solder in option, + 16V to + 30V loop power required. FSR = Full Scale Range.

Specifications subject to change without notice.

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## MULTIBUS<sup>™</sup> (IEEE-796) Compatible Analog Input/Output Boards

## RTI-711, 724, 732

#### FEATURES

Direct Plug-In Replacements With Industry
Standard 711/724/732 Analog I/O Boards
RTI-711 Input Board
32SE/16D Input Channels
Programmable Gain Amplifier
12-Bit A/D Resolution
RTI-724 Output Board
4 Output Channels
12-Bit D/A Resolution
4-20mA Current Loop Outputs (Optional)
RTI-732 Input/Output Board
(Same as 711 and Includes)
2 Output Channels
12-Bit D/A Resolution
4-20mA Current Loop Outputs (Optional)
General
Compatible With All MULTIBUS (IEEE-796)
Microcomputers
Memory-Mapped I/O Operation Over 24-Bit Address
Range ·
Operates Under Intel's RMX-80 Real-Time
Multitasking Exec
Single +5V Power Requirement

#### **GENERAL DESCRIPTION**

Analog Devices RTI-711, RTI-724, and RTI-732 are complete, single board analog input/output subsystems that interface with any MULTIBUS (IEEE-796) compatible microcomputer. These boards provide measurement and control capability to a wide range of data acquisition and voltage actuated applications.

The series is comprised of an input only board (RTI-711), an output only board (RTI-724) and a combination I/O board (RTI-732); each of which interfaces to the microcomputer as a



block of address locations (memory mapped interface). All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage.

All boards are direct replacements for industry's standard 711/ 724/732 analog I/O boards. In addition, Analog Devices boards offer extended memory-mapped addressing over the entire 24bit address range. This extended memory permits direct compatibility to SBC-80, SBC-86, SBC-88, or any other 8- or 16-bit microcomputer that requires address capability up to 16M byte. In addition, the RTI-711, 724, 732 boards are designed to operate under Intel's RMX-80 analog software drivers.

A compatible signal conditioning subsystem (3B Series) is also offered by Analog Devices which provides signal conditioning necessary for direct connections to thermocouples, RTDs and strain gages.

µCOMPUTER ANALOG I/O SUBSYSTEMS VOL. II, 17-7

			INPU	т	OUTPUT			
Model	Board Type	Channel Standard	Capacity Optional	Gain Range	A/D Resolution	Channel Capacity	D/A Resolution	4-20mA Output
RTI-711	Analog Input	16SE/8D	32SE/16D	1,2,4,8	12 Bits	-	N/A	
RTI-732	Analog Input/Output	16SE/8D	32SE/16D	1, 2, 4, 8	12 Bits	2	12 Bits	2
RTI-732-V	Analog Input/Output	16SE/8D	32SE/16D	1, 2, 4, 8	12 Bits	2	12 Bits	-
RTI-724	Analog Output	-	N/.	A		4	12 Bits	4 .
RTI-724-V	Analog Output	-	N/.	A		4	12 Bits	-

#### RTI-711/724/732 Functional Chart

MULTIBUS RMX-80 is a trademark of Intel Corporation.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

## SPECIFICATIONS

ANALOG INPUT (RTI-711, 732) Number of Input Channels

Input Overvoltage Protection<sup>1</sup> Input Impedance Input Bias Current Analog Connector A/D Input Voltage Ranges<sup>2</sup> A/D Resolution A/D Output Codes<sup>2</sup> Instrumentation Amplifier Gain Ranges A/D Conversion Speed System Accuracy<sup>3</sup>

System Temperature Coefficient

Common Mode Rejection (CMR) Common Mode Voltage (CMV) System Throughput<sup>4</sup> Sample Rate (Single Channel) Channel to Channel Rate External Trigger Pacer Clock

#### ANALOG OUTPUT (RTI-724, 732)

Number of Output Channels

D/A Resolution D/A Input Codes<sup>2</sup> Output Voltage Ranges<sup>2</sup> Output Current Range (RTI-724, 732) Output Connector Slew Rate Accuracy<sup>3</sup> Temperature Coefficient

#### INTERFACE PARAMETERS Compatibility

Implementation

Addressing

#### POWER REQUIREMENT RTI-711 RTI-724 RTI-732

#### TEMPERATURE RANGE Operating Storage

#### **RELATIVE HUMIDITY**

NOTES

<sup>1</sup>Specified with power applied,  $\pm 20V$  with power off.

<sup>2</sup>User selectable with wire-wrap jumpers.

<sup>3</sup>Includes 3 sigma noise, linearity, offset gain and dynamic response errors.

<sup>4</sup>Assuming 8MHz CPU clock includes time required to transfer data from RTI to system memory.

Specifications subject to change without notice.

#### (typical @ 25°C with nominal supply voltage unless otherwise noted)

16 Single-Ended or 8 Differential (Jumper Selectable) Expandable to 32 Single-Ended or 16 Differential Using Two Plug-In Multiplexers (ADI P/N OA10) ±35V (Dielectrically Isolated)  $>10^8\Omega$  $\pm 50 nA$ 50 pin (Mating Connector 3M #3415-000)  $0 \text{ to } + 5\text{V}, 0 \text{ to } + 10\text{V}, \pm 5\text{V}, \pm 10\text{V}$ 12 Bits (4096 Counts) Binary, Offset Binary, Two's Complement 1, 2, 4, 8 (Software Programmable) 40kHz 0.05% FSR  $\pm 1/2$ LSB (Gain = 1) 0.07% FSR  $\pm 1/2$ LSB (Gain = 2,4,8) 0.0025% FSR/°C (Gain = 1) 0.0030% FSR/°C (Gain = 2,4,8) 60dB (Differential Input) ± 10.24V (Signal Plus Common Mode) 33,000 Channels/sec

25,000 Channels/sec 25,000 Channels/sec TTL Compatible, 1.5 $\mu$ s (min) Pulse Width Crystal Controlled Accuracy 0.05% Divider Range of  $\frac{1000}{2^n}$  ms where n = 0 to 10

4 (RTI-724) 2 (RTI-732) 12 Bits Binary, Offset Binary, Two's Complement 0 to + 5V, 0 to + 10V, ± 5V, ± 10V @ ± 5mA 4-20mA 50 Pin (Mating Connector 3M #3415-000) 10V/µs 0.05% FSR ± 1/2LSB ± 50ppm of FSR/°C

Meets all Electrical and Mechanical MULTIBUS (IEEE-796) Specifications Memory Mapped I/O Compatible With all CPUs Reserved a Block of Contiguous Memory Locations Relative to a Jumper Selectable Memory Base Address

 $+5V \pm 5\% 0.8A$ +5V ± 5% 0.6A +5V ± 5% 1.2A

0 to + 70°C - 55°C to + 85°C

#### Meets or Exceed MIL-STD- 202 Method 103

### VOL. II, 17–8 μCOMPUTER ANALOG I/O SUBSYSTEMS

# 

## Low Cost, STD Bus Compatible Analog I/O Subsystems

## RTI-1225/1226

#### **FEATURES**

RTI-1225 ANALOG INPUT/OUTPUT CARD 16 Single-Ended/8 Differential Input Channels 2 Output Channels 10-Bit A/D and 8-Bit D/A Resolution

RTI-1226 ANALOG INPUT CARD 16 Single-Ended/8 Differential Input Channels 10-Bit A/D Resolution

#### GENERAL

Low Cost Single +5V Power Requirement Memory Mapped or I/O Selectable Compatible with All STD CPU Cards

NEW FEATURE Memory Mapped or Port I/O Selectable



#### SERIES DESCRIPTION

Analog Devices' RTI-1225 series products handle analog inputs and outputs for STD Bus microcomputer systems. These subsystems provide a cost effective solution to interfacing with the analog world by minimizing the hardware development time and providing low function cost.

The RTI-1225 combines both analog input and output functions on a single card, thus reducing components count. This design provides data acquisition of analog signals from 8 differential or 16 single-ended, jumper-selectable voltage inputs and 2 independent voltage outputs. Also included is a differential amplifier, a sample and hold circuit and a 10-bit A/D converter (AD571). Throughputs of 25,000 channels per second are achievable. The analog output section consists of two 8-bit D/A converters. Each channel has a user selectable output range of 0 to +10V,  $\pm 5V$ and  $\pm 10V$ . The RTI-1226 Analog Input Card provides the same analog functions as the RTI-1225, but does not include the two channels of 8-bit analog output. An ideal choice when only analog inputs are required, this card can be configured for 0 to +10V,  $\pm 5V$  and  $\pm 10V$  input ranges.

Reliable analog connections are made using 3M's "Scotchflex" socket and header connectors which enable a flat ribbon cable to be combined with gas tight and corrosion resistant connectors. An optional screw termination panel is also offered for simple and convenient field wire connections.

The RTI-1225 series cards come complete with their own dc/dc converters, allowing the cards to operate directly from the microcomputers +5V supply. Configured as a block of contiguous memory locations (memory mapped interface), these products simplify the task of interfacing STD Bus microcomputers to the real world.

-		INPUT		OUTPUT	
Card Type	Model No.	Channel Capacity	A/D Resolution	Channel Capacity	D/A Resolution
Analog Input/ Output	RTI-1225	16SE/8D	10 Bits	2	8 Bits
Analog Input	RTI-1226	16SE/8D	10 Bits	N	I/A ———

RTI-1225/1226 Function Chart

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

## SPECIFICATIONS (typical @ 25°C with nominal supply voltage unless otherwise noted)

INPUT				
Number of Output Channels	16 Single-Ended or 8 Differential (Jumper Selectable)			
Input Overvoltage Protection <sup>1</sup>	± 35V (Dielectrically Isolated)			
Input Impedance	>10 <sup>8</sup> Ω			
Input Current	$\pm 50 nA$			
Input Voltage Ranges <sup>2</sup>	$0V \text{ to } + 10V, \pm 5V, \pm 10V$			
Input/Output Connector	3M # 3493, 34 pin			
A/D Resolution	10 Bits (1024 Counts)			
A/D Output Codes <sup>2</sup>	Binary, Offset Binary, Two's Complement			
Instrumentation Amplifier Gain Range	1V/V			
A/D Conversion Time	25µs			
System Throughput	25.000 channels/sec			
Common Mode Voltage (CMV)	$\pm 10V \min$			
Common Mode Rejection (CMR)	60dB			
Linearity	$\pm 1/2LSB$			
Differential Nonlinearity	$\pm 1/2LSB$ $\pm 1/2ISB$			
Total System Error				
(Adjustable to Zero)	$\pm 0.1\% \text{ of FSR}$			
Temperature Coefficient				
Gain	+ 50ppm/°C of FSR (Full Scale Range)			
Offset	+ 25npm/°C of FSR			
OUTPUT (RTI-1225 Only)	2			
D/A Develution				
D/A Resolution	8 Bits (256 Counts)			
D/A Input Codes	Binary, Offset Binary, I wo's Complement			
Output voltage Ranges	$0 \vee to + 10 \vee, \pm 5 \vee, \pm 10 \vee @ 5 mA$			
Output Settling 1 ime	$25\mu s(to \pm 1/2LSB)$			
Nonlinearity	± 1/2LSB			
Differential Nonlinearity	$\pm 1/2LSB$			
Total Error (Adjustable to Zero)	±0.4%			
l'emperature Coefficient				
Gain	± 50ppm/°C of FSR			
Offset	± 30µV/°C			
INTERFACEPARAMETERS				
Compatibility	Meets all Electrical and Mechanical STD Bus Specifications			
Implementation	Memory Mapped I/O Compatible with All CPU Types			
	Port Mapped I/O Compatible with 8080, 8085, 8086 and Z-80			
	Family of CPUs.			
Address Selection	5 Contiguous Bytes in a 16 Byte Block. (Jumper Selectable			
	in Any One of 256 Locations in 64K of Memory Space.)			
Port Selection	5 Contiguous Ports in a 16 Port Block. (Jumper Selectable			
	on Any 16 Port Boundary in Either an 8-Bit or 16-Bit Port Image.)			
Expansion Options	MEMEX and IOEXP Fully Supported with Jumper			
	Selectable Enable High, Enable Low and Ignore Expansion Options.			
POWER REQUIREMENT	+ 5V + 5%@ 750mA			
	(On-Board dc/dc Converter Generates An Isolated ± 15V to			
	Power the Data Acquisition Components)			
	rome in Dawriequisition components)			
TEMPERATURE	A			
Operating				
Storage	- >> 0 to + 85 U			
<b>RELATIVE HUMIDITY</b>	Meets or Exceeds MIL-STD 202 Method 103			

NOTES <sup>1</sup>Specification with power applied,  $\pm 20V$  with power off. <sup>2</sup>User selectable with wire-wrap jumpers.

Specifications subject to change without notice.

#### **ORDERING GUIDE**

ADI Model No.	Description	Used On	
Cards RTI-1225	Analog Input/Output Card	· _	
Mating Connectors	6		
AC1562	34-pin flat cable connector		
	with 3' color coded cable		
	Analog Input/Output	RTI-1225	
	Analog Input	RTI-1226	
Screw Termination	Panel		
AC1585-3	Screw terminal for field wiring.	RTI-1225/1226	
User's Manual*	-		
AC1564	User's Manual for RTI-1225/1226	-	

\*A user's manual is furnished with each shipment. Additional copies are available under this part number.
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### Micromodule Motorola Compatible Analog I/O Subsystems

### MODELS RTI-1230, 1231, 1232

### **FEATURES**

Complete Analog I/O Systems for OEM Applications Motorola Micromodule and EXORcisor Compatible Memory Mapped I/O Interface **Convenient Address and Features Selection** 12-Bit ADC Direct Operation from ±12V, +5V Bus Power Analog Input Subsystem RTI-1230 Up to 32 Input Channels Each Input Channel Protected to V<sub>CC</sub> +20 Volts Software or Resistor Programmable Gain Software Controlled EOC Interrupt Auto Scan Capability 0-20mA Current Loop Input Analog Combination I/O Subsystem RTI-1231 Same Analog Input Features Plus: Two 12-Bit D/A Converters **4 Quadrant Multiplication On-Board or External Reference Capability** Analog Output Subsystem RTI-1232 Four Independent 12-Bit Analog Outputs Four Software Controlled, High Current Logic Driver Outputs **Optional 4-20mA Current Loop Converter Outputs DAC and Logic Driver Reset** Remote Load Sensing

### SERIES DESCRIPTION

The RTI-1230 series are complete 12-bit analog I/O subsystems which are electrically and mechanically compatible with the Motorola EXORcisor Development System and Micromodule single board microcomputer. The series is comprised of an input only board (RTI-1230), an output only board (RTI-1232), and a combination I/O board (RTI-1231); each of which interfaces to the microcomputer as a block of 16 address locations (memory mapped interface). All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional features and options reduce both the hardware and the software effort required to interface analog signals to the microcomputer, freeing the designer to spend more time and effort on his particular application.

### **RTI-1230 ANALOG INPUT SUBSYSTEM**

The basic function of the RTI-1230 input subsystem is to digitize analog signals and transfer the converted digital data to the microcomputer. The design includes protected input multiplexers, either a resistor-programmable-gain or a software programmable-gain instrumentation amplifier, a sample and hold amplifier, a 12-bit analog to digital (A/D) converter (RTI-1230-R and RTI-1230-S) and the associated digital interface logic.



### RTI-1231 COMBINATION ANALOG I/O SUBSYSTEM

The RTI-1231 provides the same analog input functions as the RTI-1230 *plus* two channels of high resolution, 12-bit analog voltage output. The 12-bit digital to analog converters are capable of full 4 quadrant multiplication. Four output voltage ranges can be jumper selected independently for each output channel, by using the on-board references.

### RTI-1232 ANALOG OUTPUT SUBSYSTEM

The RTI-1232 output subsystem provides 4 channels of 12-bit analog output and 4 high current, digital logic driver outputs. The four digital outputs are software controlled, open collector drivers capable of sinking 300mA and sustaining voltages up to +30V. They can be used to provide "ON/OFF" system functions for driving relays, solenoids, and valve control.

The DAC's used are 4 quadrant multiplying 12-bit DAC's. Each DAC input code and output range are jumper selectable.

The analog output channels can also be ordered with optional 4-20mA current loop outputs ideal for use in process and industrial control applications. These high compliance voltage to current (V/I) converter modules (P/N 0A08) meet all the requirements of ISA-S50.1 compatibility of signal for Type 3, Class L, nonisolated 4-20mA current loop transmitters.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

### **SPECIFICATIONS** (typical @ +25°C and +5V, ±15V unless otherwise noted)

ANALOG INPUT	•										
Model Numbers -	Input Boards	:	RTI-1230	-R	RTI	1230-S					
	Combo I/O B	oards:	RTI-1231	-R	RTI	·1231-S					·
Input Channels:	Basic Board		16 SE, 16	PD, 8 Diff.	•						
	with On-Boar	d Expansion	32 SE, 32	PD, 16 Diff.							
	with Off-Boa	rd Expansion	1 256 Total	A ALONE C	0.61	517 17 S as +10	WEE				
Input Range at Ca	ard Edge		TUMV F.S	s. to ±10v F.S.	0.62	5V F.S. to ±10	JV F.S.				
Current Loop Inp	uts		+(V_=_ +2)		•						
Switching Charact	teristics		Break-Bef	ove-Make	•						
Switching charact			Dicak-Den		<b>c c</b>						
Instrumentation A	Amplifier Gair	1	Resistor P	rogrammable	Soft	ware Programn	nable .				
Gain Range			10/0 to 1	1000 v / v	1, 2,	4,00/0					
CMV Range	(U_)				•						
Lunus Caseline Tin	(C = 1)		15// max		100	max					
Input Settling I in	ne(G=1)		$>10^8 \Omega$		• •	max					
Input Riss Curron			+50nA		±5n	A max					
niput Blas Curren			±70nA m:	ax	±50	nA max					
			10 8		12.5						
ADC Resolution			12 Bits		12 0	its					
Three Date			25µs max	nels/sea							*
ADC Input Rate	-		+5V +5 1	2V +10V +102	94V						
ADC input Kange	5		±2.5V	+5V. +10V. +10	24V *						
ADC Output Code	es		BIN OBN	250	•						
Nonlinearity Erro	сэ . т		+1/21 SB	typ (+11 SB max)	•						
Offset Error			Adi, to Ze	ero	″ ÷∙						
			(, 50)			°c					
Offset TC (RTI)			$(1+\frac{1}{G})$	μV/°C	±50	μν/ C					
Gain Error			Adj. to Że	ero	•						
Gain TC (RTI)			±25ppm c	of RDG./°C						·	
Noise Error (G =	1)		±1/4LSB	max							
Overall Error (G =	= 1)'		±1LSB ma	ax	•						
Overall Error			±1LSB at	G = 100	±1.5	LSB at $G = 8$					
ANALOG OUTPU	JT			P	OWER RE	QUIREMENT	s				
Model Numbers -					Without	de-de Ontion	Input Bo	ards	Output Boards	Combo Boards	0408(2)
Combo I/O Boa	ards:	RTI 1231	R, S		±15V	/±3%	30mA		50mA	50mA	10mA
Output Boards:	:			RTI-1232	-15V	/±3%	30mA		40mA	45mA	2mA
<b>Output Channels</b>		2		4	+5V/	±5%	700mA		350mA	900mA	0mA
DAC Resolution		12 Bit		•	With de-	de Ontion				•	
		-			with uc	ac option					
Nonlinearity Erro	or	±0.05% FS	R	•	+5V/:	±5%	1100mA	1	950mA		
Nonlinearity Erro Settling Time for	a 20V Step	±0.05% FS 10μs max	R	•	+5V/	±5%	1100mA	1	950mA	-	
Nonlinearity Erro Settling Time for Output Ranges	a 20V Step	±0.05% FS 10μs max ±5V, ±10V	R 7, +5V, +10V	* * *	+5V/:	±5%	1100mA	1	950mA	-	
Nonlinearity Erro Settling Time for Output Ranges Output Current	a 20V Step	±0.05% FS 10µs max ±5V, ±10V 5mA @ 10	R 7, +5V, +10V V	•	+5V/:	±5%	1100mA	1	950mA		
Nonlinearity Erro Settling Time for Output Ranges Output Current Offset Error	a 20V Step	±0.05% FS 10μs max ±5V, ±10V 5mA @ 10' Adj. to Zet	R 7, +5V, +10V V 70	• • • •	+5V/:	±5%	1100mA	!	950mA	 -	- ,
Nonlinearity Erro Settling Time for Output Ranges Output Current Offset Error Offset TC	or a 20V Step	±0.05% FS 10μs max ±5V, ±10V 5mA @ 10' Adj. to Zet ±25μV/°C	R 7, +5V, +10V V 70	•	+5V/:	±5%	1100mA	OR	950mA DERING G	UIDE	- ,
Nonlinearity Erro Settling Time for Output Ranges Output Current Offset Error Offset TC Gain Error Coin TC	or a 20V Step	±0.05% FS 10µs max ±5V, ±10V 5mA @ 10' Adj. to Zet ±25µV/°C Adj. to Zet ±25pm/°C	R 7, +5V, +10V V 70	•	+5V/:	±5%	1100mA	OR	950mA DERING G	UIDE	
Nonlinearity Erro Settling Time for Output Ranges Output Current Offset Error Offset TC Gain Error Gain TC Evernal Reference	or a 20V Step	±0.05% FS 10μs max ±5V, ±10V 5mA @ 10' Adj. to Zer ±25μV/°C Adj. to Zer ±25ppm/°C	R V V To C L LOV	•	+5V/:	40005	1100mA	OR	950mA DERING G	UIDE	
Nonlinearity Erro Settling Time for Output Ranges Output Current Offset Error Offset TC Gain Error Gain TC External Reference	or a 20V Step ce Range	±0.05% FS 10μs max ±5V, ±10V 5mA @ 10' Adj. to Zet ±25μV/°C Adj. to Zet ±25ppm/°C -10V to +3 10kΩ Each	R V V To C 10V 1 DAC	•	+5V/:	MODEI	1100mA	OR	950mA DERING G	UIDE	
Nonlinearity Erro Settling Time for Output Ranges Output Current Offset Error Offset TC Gain Error Gain TC External Referent Input Impedance DAC Input Codes	or a 20V Step ce Range	±0.05% FS 10µs max ±5V, ±10V 5mA @ 10' Adj. to Zet ±25µV/°C Adj. to Zet ±25ppm/°C -10V to + 10kΩ Each BIN. OBN.	R 7, +5V, +10V V ro C C 10V DAC 25C		+5V/:	MODE NUMBE	1100mA L R	OR	950mA DERING GI DESCRIF	UIDE	
Nonlinearity Error Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Undation	or a 20V Step ce Range	$\pm 0.05\%$ FS 10µs max $\pm 5V, \pm 10V$ 5mA @ 10' Adj. to Zet $\pm 25\mu V/^{\circ}C$ Adj. to Zet $\pm 25\mu V/^{\circ}C$ Adj. to Zet $\pm 25ppm/^{\circ}C$ -10V to + 10kΩ Each BIN, OBN, Double Bu	R 7, +5V, +10V V ro C 10V DAC 2SC (ffered	• • • • • • •	+5V/:	MODE NUMBE RTI-1230	1100mA L R	OR	950mA DERING G DESCRIF Board with 12	UIDE PTION Bit A/D and	
Nonlinearity Error Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Input Codes DAC Updating Load Sensing	or a 20V Step ce Range	$\pm 0.05\%$ FS 10 $\mu$ s max $\pm 5V, \pm 10V$ 5mA @ 10' Adj. to Zet $\pm 25\mu V/^{\circ}C$ Adj. to Zet $\pm 25\mu V/^{\circ}C$ -10V to + 10k $\Omega$ Each BIN, OBN, Double Bu Each DAC	R Y, +5V, +10V V To C 10V DAC 2SC ffered	•	+5V/:	MODE NUMBE RTI-1230	1100mA L R	OR Input Resist	950mA DERING GI DESCRIF Board with 12 tor Programmal	UIDE PTION Bit A/D and ble Gain Amplifi	 er
Nonlinearity Error Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Input Codes DAC Updating Load Sensing	or a 20V Step ce Range	±0.05% FS 10µs max ±5V, ±10V 5mA @ 10' Adj. to Zer ±25µV/°C Adj. to Zer ±25pm/°C -10V to +1 10kΩ Each BIN, OBN, Double Bu Each DAC	R (, +5V, +10V V ro C 10V DAC 2SC ffered	• • • • • •	+5V/:	MODE NUMBE RTI-1230 RTI-1230	1100mA L R R -S	OR Input Resist Input	950mA DERING GU DESCRIF Board with 12 Board with So	UIDE PTION Bit A/D and ble Gain Amplifie ftware PGA	 er
Nonlinearity Erro Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Input Codes DAC Updating Load Sensing CURRENT LOOR	or a 20V Step ce Range P OUTPUTS (	±0.05% FS 10µs max ±5V, ±10V 5mA @ 10' Adj. to Zet ±25µV/°C Adj. to Zet ±25pm/°C -10V to +1 10kΩ Each BIN, OBN, Double Bu Each DAC RTI-1232)	R , +5V, +10V V ro C 10V DAC 2SC ffered (Option P/N ( SA SEG 1 T	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	+5V/:	MODEI NUMBE RTI-1230 RTI-1231 RTI-1231	1100mA L R R R R	OR Input Resist Input	950mA DERING GI DESCRIF Board with 12 tor Programmal Board with So ogard with Resis	UIDE PTION Bit A/D and ble Gain Amplifii fitware PGA stor Programmab	er le
Nonlinearity Error Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Updating Load Sensing CURRENT LOOI Type Number	or a 20V Step ce Range P OUTPUTS (	±0.05% FS 10μs max ±5V, ±10V 5mA @ 10 Adj. to Zer ±25μV/°C Adj. to Zer ±25pm/°C -10V to + 10kΩ Each BIN, OBN, Double Bu Each DAC RTI-1232)	R y, +5V, +10V V ro C 10V DAC 2SC ffered (Option P/N ( ISA-550.1, TAC One per DAC	0 0 0 0 0 0 0 0 0 0 0 8 0 0 0 0 8 0 0 0 0 8 0	+5V/:	MODE  NUMBE RTI-1230 RTI-1231 RTI-1231	1100mA L R -R -R -R	OR Input Resist Input I/O B Gain	950mA DERING GI DESCRIF Board with 12 tor Programmal Board with Resis Amplifier	UIDE PTION Bit A/D and ble Gain Amplific ftware PGA stor Programmab	er le
Nonlinearity Error Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Input Codes DAC Updating Load Sensing CURRENT LOOF Type Number Output Current F	or a 20V Step ce Range P OUTPUTS (	±0.05% FS 10μs max ±5V, ±10V 5mA @ 10 Adj. to Zet ±25μV/°C Adj. to Zet ±25ppm/° -10V to + 10kΩ Each BIN, OBN, Double Bu Each DAC RTI-1232)	R (, +5V, +10V V co C 10V 10V 10AC 2SC ffered (Option P/N ( ISA-S50.1, T) One per DAC (Aron Provide Control (Non	DA08) prpe 3, Class L	+5V/:	MODE: NUMBE RTI-1230 RTI-1231 RTI-1231 RTI-1231 RTI-1231	1100mA L R -R -R -S -S	OR Input Resist Input I/O B Gin B	950mA DERING GI DESCRIF Board with 12 tor Programmal Board with So oard with So oard with Soft oard with Soft	UIDE PTION Bit A/D and ble Gain Amplifi ftware PGA stor Programmab ware PGA	er .
Nonlinearity Error Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Input Codes DAC Updating Load Sensing CURRENT LOOI Type Number Output Current F Supply Voltage R	or a 20V Step ce Range P OUTPUTS ( Range Range	±0.05% FS 10µs max ±5V, ±10V 5mA @ 10 Adj. to Zet ±25µV/°C -10V to +1 10kΩ Each BIN, OBN, Double Bu Each DAC RTI-1232)	R (, +5V, +10V V co C 10V DAC 2SC ffered (Option P/N ( ISA-SS0.1, T) One per DAC 4-20mA (Non	DA08) ype 3, Class L issolated)	+5V/:	MODE: NUMBE RTI-1230 RTI-1231 RTI-1231 RTI-1232	1100mA L R -R -R -R -S	OR Input Resist Input I/O B Gain I/O B Output	950mA DERING GU DESCRIF Board with 12 Board with Soft Amplifier oard with Soft ut Board with 4	UIDE PTION Bit A/D and ble Gain Amplific ftware PGA stor Programmab ware PGA b DAC's	er le
Nonlinearity Error Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Input Codes DAC Updating Load Sensing CURRENT LOOI Type Number Output Current F Supply Voltage R Load Resistance	or a 20V Step ce Range P OUTPUTS ( Range tange Range	±0.05% FS 10µs max ±5V, ±10V 5mA @ 10 Adj. to Zet ±25µU/°C Adj. to Zet ±25ppm/°C -10V to + 10kΩ Each BIN, OBN, Double Bu Each DAC RTI-1232)	R , +5V, +10V V ro C 10V 10V 2SC ffered (Option P/N ( ISA-S50.1, T) One per DAC 4-20mA (Non +15V to +30V 0Ω to 475Ω	DA08) ype 3, Class L iisolated)	+5V/:	MODEI NUMBE RTI-1230 RTI-1231 RTI-1231 RTI-1232 ACCESSO	1100mA L R R S R S R IES	OR Input Input I/O B Gain I/O B Output	950mA DERING G1 DESCRIF Board with 12 tor Programmal Board with Soft Amplifier oard with Soft ut Board with 4	UIDE PTION Bit A/D and ble Gain Amplifit ftware PGA stor Programmab ware PGA I DAC's	 er le
Nonlinearity Error Settling Time for Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Input Codes DAC Updating Load Sensing CURRENT LOOI Type Number Output Current F Supply Voltage R Load Resistance I Offset TC	or a 20V Step ce Range P OUTPUTS ( Range Range Range	±0.05% FS 10μs max ±5V, ±10V 5mA @ 10 Adj. to Zet ±25µV/° C Adj. to Zet ±25pm/° 10kΩ Each BIN, OBN, Double Bu Each DAC RTI-1232)	R (, +5V, +10V V το C 10V DAC 2SC ffered (Option P/N ( ISA-S50.1, T) One per DAC 4-20mA (Non +15V to +30V 0Ω to 475Ω	DA08) ype 3, Class L uisolated)	+5V/:	MODEI NUMBE RTI-1230 RTI-1231 RTI-1231 RTI-1232 ACCESSO	1100mA L R R R S -R -S ORIES	OR Input Resist Input I/O B Gain I/O B Output	950mA DERING GI DESCRIF Board with 12 tor Programmal Board with Resis Amplifier oard with Soft ut Board with 4	UIDE PTION Bit A/D and ble Gain Amplifit ftware PGA stor Programmab ware PGA I DAC's	er Ie
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Nonlinearity Error Settling Time for Output Ranges Output Ranges Output Current Offset Error Gain Error Gain TC External Referent Input Impedance DAC Input Codes DAC Updating Load Sensing CURRENT LOOI Type Number Output Current F Supply Voltage R Load Resistance I Offset TC Gain TC Nonlinearity Settling Time DIGITAL OUTPU Type Number Current Range Supply Voltage F MECHANICAL Size Weight TEMPERATURE	or a 20V Step ce Range P OUTPUTS ( Range Range UTS (RTI-1232 Range	±0.05% FS 10µs max ±5V, ±10V 5mA @ 10 Adj. to Zer ±25µV/°C Adj. to Zer ±25ppm/° -10V to +1 10kΩ Each BIN, OBN, Double Bu Each DAC RTI-1232)	R ', +5V, +10V V ', +5V, +10V V ', +5V, +10V ', -5V, +10V ', -5V, +10V ', -2V, +10V ', -2V, +10V ', -2V, -2V, +10V ', -2V, -2V, +10V ', -2V, +	DA08) pre 3, Class L isolated) Preripheral Driv tly Controlled) bink Current at 0. he Collectors x 0.6" 156.2mm x 15.2r )	ver .1V mm)	MODE: NUMBE RTI-1230 RTI-1230 RTI-1231 RTI-1231 RTI-1232 ACCESSC 0A08 0A09 0A10 CONNECT AC1556 AC1557 AC1559 *ALL CO ATTACH	1100mA L R -R -S -R S RIES TORS NNECTOR	OR Input Input I/O B Gain J I/O B Output 4–20 DC-D DC-D Multij 20 Pin 50 Pin 50 Pin 50 Pin 53 FIA	DERING GI DESCRIF Board with 20 Board with 20 Board with So oard with Resis Amplifier oard with Soft ut Board with Soft ut Board with Soft to Converter plexer Expansion n, Card Edge* n, Card Edge* n, Card Edge* N, Card Edge*	UIDE PTION Bit A/D and ble Gain Amplifit ftware PGA tor Programmab ware PGA DAC's e on Kit	er le
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\*Same specifications as for RTI-1231-R. Specifications subject to change without notice.

VOL. II, 17–12 µCOMPUTER ANALOG I/O SUBSYSTEMS

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#### FEATURES

RTI-1240 Input Board
32SE/16D Input Channels
Programmable Gain Amplifier
12-Bit A/D Resolution
RTI-1241 Input/Output Board
(Same as RTI-1240 and Includes)
2 Output Channels
12-Bit D/A Resolution
4-20mA Current Loop Outputs (optional)
RTI-1242, 1243 Output Boards
4 or 8 Output Channels
12-Bit D/A Resolution
8 Logic Drivers

### GENERAL

Compatible to all TM990 Microcomputers Selectable 64K, 1M or 16M Address Space Single +5V Power Requirement (Optional)

### **GENERAL DESCRIPTION**

Analog Devices RTI-1240 Series are complete, 12-bit resolution, analog input, output and combination input/output subsystems that interface to any Texas Instruments TM990 Microcomputer Module. These boards provide analog measurement and control capability in a wide range of data acquisition and voltage actuated applications. These products simplify the task of interfacing a digital microcomputer to the analog world and incorporate design techniques which maximize the performance.

The series is comprised of an input board (RTI-1240), a combination input/output board (RTI-1241) and two output boards (RTI-1242, 1243); each of which interfaces to the TM990 microcomputer as a block of contiguous address locations (memory mapped interface). The boards are electrically and mechanically compatible to any TM990 microcomputer.

### TM990 Compatible Analog I/O Boards RTI-1240 Series



The RTI-1240 Series boards provide a cost effective solution to interfacing to the real world and feature 12-bit resolution, programmable gain for low level signals, analog channel expansion, 4-20mA output, high current logic driver outputs and on-board power supplies.

#### APPLICATIONS

In a typical application there are several transducers which convert real world variables such as temperature, pressure, and flow into changing electrical units such as voltage, current and resistance. The analog input board allows the microcomputer to measure these varying signals. The computer collects and digitally processes the data and makes decisions based on these measurements according to programs stored in memory. The analog output board receives a digital word from the microcomputer and converts it into an analog signal that can be used to drive chart recorders, proportional valves, positioners, and motors.

		INPUT					OUTPUT			
Model	Board Type	Channel Capacity Standard Optional		Gain Range SR		A/D Resolution	Channel Capacity	D/A Resolution	4-20mA Output	
RTI-1240 RTI-1241 RTI-1242 RTI-1243	Analog Input Analog Input/Output Analog Output Analog Output	16SE/8D 16SE/8D	32SE/16D 32SE/16D N/A	1,2,4,8 1,2,4,8	1–1000 1–1000	12 Bits 12 Bits	2 4 8	- N/A 12 Bits 12 Bits 12 Bits	2	

RTI-1240 Series Functional Chart

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

### SPECIFICATIONS

(typical @ + 25°C and nominal supply voltage)

ANALOG INPUT (RTI-1240, RTI-1241) Input Channels <sup>1</sup>	16-Single Ended or 8 Differential	
Input Overvoltage Protection Input Impedance Input Bias Current	Expandable to 32-Single Ended or 16 Different two plug-in multiplexers (ADI P/N OA10) $\pm$ 35V (Dielectrically Isolated) $> 10^8\Omega$ $\pm$ 50nA max	lai Using
Input Connector A/D Input Voltage Ranges <sup>1</sup>	50 pin (Mating Connector 3M#3415-000) 0 to + 10V, 0 to + 10.24V ± 5V, ± 5.12V, ± 10V, ± 10.12V 0 to + 5V, 0 to + 10V, 0 to + 10.12V	
A/D Resolution A/D Output Codes <sup>1</sup>	12 Bits (4096 Counts) Binary, Offset Binary, Two's Complement	
	RTI-1240-R, RTI-1241-R	RTI-1240-S, RTI-1241-S
Instrumentation Amplifier Gain Range System Accuracy	1 to 1000V/V Resistor Programmable ± 0.025% FSR max (Gain = 1) ± 0.05% FSR max (G = 200)	1, 2, 4, 8 V/V Software Programmable ± 0.025% FSR max (Gain = 1, 2, 4, 8)
System Temperature Coefficient Offset Error (RTI)	$\pm \left(1 + \frac{50}{G}\right) \mu V ^{\circ}C$	±30µV/°C
Gain Error	± 25ppm of Reading/°C	± 20ppm of Reading/°C
Common Mode Rejection (CMR)	76dB min	*
Common Mode Voltage (CMV) System Throughput <sup>2</sup>	± 10.24V (Signal Plus Common Mode)	*
Single Channel Rate	33,000 Conversions/sec	*
A /D Conversion Speed	25,000 Channels/sec	*
External Trigger	TTL Compatible 1 Sus (min) Pulse Width	*
ANALOGOUTPUT (PTL 1241 PTL 124	2 PTI 1242)	
Number of Output Channels	2(RTI-1243)	
i amori oi o'alpat Giannois	4(RTI-1242)	
	8 (RTI-1243)	
D/A Resolution	12-Bits	
D/A Input Codes <sup>1</sup>	Binary, Offset Binary, Two's Complement	
Output Voltage Ranges <sup>1</sup>	$0 \text{ to } + 10\text{V}, 0 \text{ to } + 10\text{V}, \pm 5\text{V}, \pm 10\text{V} @ \pm 5\text{mA}$	
Output Current Range <sup>2</sup>	4-20mA Using V/I Converter (P/N OA08)	
(Optional 2 Channel on R 11-1241 Only)	. 0.010/	
Differential Nonlinearity	$\pm 0.01\%$ max	•
Gain Error (adjustable to zero)	+0.01% of FSR (Full Scale Bange)	
Offset Error (adjustable to zero)	$\pm 0.02\%$ of FSR	
Temperature Coefficient		
Gain	± 30ppm of FSR/°C	
Offset	$\pm 25 \mu V/^{\circ}C$	
Output Connector	50 pin (Mating Connector 3M #3415-000)	
INTERFACE PARAMETERS		
Compatibility	Meets all TM990 Module Mechanical and	
A J J	Electrical Specifications	
Implementation	Memory Mapped 1/O Module (64K, 1M or 16M	ble L/OL costions Polative to
imprementation	a jumper selectable base address	
Power Requirements	_,	
Using OA09	+5V ±5%@1.6A	
External Power	+5V ±5%@1.1A	
	$+15V \pm 3\% @ 50mA$	
	$-15V \pm 3\% @ 40mA (RTI-1240)$	
	$-15V \pm 5\% (@ 80mA (K11-1241, K11-1242))$ -15V + 3% @ 150mA (PTI-1242)	
TEMPERATURE	1.57 ± 570 (# 150mm (R11-1245)	
Operating	0 to + 70°C	
Storage	- 55°C to + 85°C	
NOTES	<sup>2</sup> The effective through pitters is the second state of	data bandiin annaine anna anna data in an
	<sup>3</sup> V/I converter requires + 16V to + 20V loss power	uata nandling routine, processor type and gain setting.

\*Specifications same as RTI-1240-R, RTI-1241-R. <sup>1</sup>User selectable with wire-wrap jumpers.

<sup>2</sup>The effective throughput rate is determined by software data handling routine, processor type and gain setting <sup>3</sup>V/I converter requires + 16V to + 30V loop power. Specifications subject to change without notice.

### **ANALOG** DEVICES

### DEC LSI-11 LSI-11/2 and LSI-11/23 Compatible Analog I/O Subsystems

### MODELS RTI - 1250, 1251, 1252

### FEATURES

Complete Analog I/O Subsystems Digital Equip. Corp. 16-Bit LSI-11/2 and 11/23 Compatibility Memory Mapped I/O Interface 12-Bit Resolution and Accuracy Single +5V Power Requirement 4-20mA Current Loop I/O Capability Convenient Wire Wrap Feature Selection

RTI-1250 Analog Input Subsystem 16 Input Channels – Expandable On-Board to 32 Channels Input Overvoltage Protection to ±35 Volts Resistor or Software Programmable Gain Amplifier Software Control of Interrupt, Channel Scanning and External Trigger

- RTI-1251 Analog I/O Subsystem 16 Input Channels and 2 12-Bit Analog Output Channels Four Quadrant Multiplying DAC's On-Board Reference
- RTI-1252 Analog Output Subsystem 2- or 4-, 12-Bit Analog Output Channels Field Expandable from 2 to 4 DAC Outputs 4 High Current Digital Logic Drivers Optional 4-20mA Current Loop Outputs Selectable DAC and Logic Driver Reset

### SERIES DESCRIPTION

The RTI-1250 Series products are complete, 12-bit resolution, analog I/O subsystems which are electrically and mechanically compatible with the Digital Equipment Corp. LSI-11, LSI-11/2, and LSI-11/23 single board microcomputers. The series is comprised of an input only board, an output only board, and a combination I/O board; each of which interfaces to the microcomputer as a block of 4 address locations (memory mapped interface). All bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional capabilities, features and options are included to reduce both the hardware and software effort required to interface analog signals to the microcomputer.

### **RTI-1250 ANALOG INPUT SUBSYSTEM**

The basic function of the RTI-1250 is to convert analog signals into a digital format and to present this digital data to the microcomputer. The design includes a protected input multiplexer for switching up to 32 single-ended inputs, either a software or resistor programmable gain instrumentation amplifier, a sample and hold amplifier, a 12-bit A/D converter and the associated digital interface logic.



#### INPUT MULTIPLEXER

The RTI-1250 is available with up to 32 single-ended/16 differential protected input channels on board. The multiplexer (MUX) channel can be randomly selected by writing to the MUX ADDRESS BYTE in the memory map. Also, in the AUTO MUX INC mode the MUX can be automatically incremented to the next channel following the receipt of a convert command. This auto increment feature is enabled by a software command which allows sequential scanning and random channel addressing to be mixed under software control.

### INSTRUMENTATION AMPLIFIER/SAMPLE AND HOLD AMPLIFIER

The RTI-1250 is available with two types of instrumentation amplifiers (IA) which provide 12-bit compatible CMRR and CMV specifications. The software-programmable-gain (1-2-4-8) IA provides dynamic range expansion through subtranging as well as the flexibility of using different gains for each input channel to accommodate different signal levels. The resistorprogrammable gain IA may be used for input ranges from 10mV F.S. to  $\pm 10V$  F.S.

The sample and hold amplifier (SHA) allows sampling of high slew rate signals and is automatically switched to the hold mode upon receipt of a convert command. The RTI-1250 also has a built-in provision which delays the convert command to allow the input section to fully settle following a gain change or channel change. For very high gain applications, the convert command delay can be increased either through software or by addition of a single resistor.

### **SPECIFICATIONS**

### (typical @ +25°C and nominal supply voltages unless otherwise noted)

			INPUT ONLY BO	ARDS	COMBINATIO	N	
ANALOG INPUT	(	· · · · · · · · · · · · · · · · · · ·	<b>^</b>				
Model Numbers		RTI-1250-R		RTI-1250-S	RTI-1251		
Input Channels			n : (c 1				
Expansion On-Board		10 SE, 10 PD, 8	Diff."		None		
Expansion on-board		±10mVFS to ±10	WFS	t0.625VES to ±10VES	+10mVFS to +	IOVES	
Current Loop Inputs <sup>3</sup>		0 to 50mA, 0-20	mA. etc.	•	•		
Input Protection		±(V <sub>CC</sub> +20V)		•	•		
Mux Switching		Break-Before-Ma	ke	•	•		
Input Impedance		>10 <sup>8</sup> Ω		•	•		
Input Bias Current		±50nA max		±5nA max	±50nA max		
Instrumentation Amplifier		I/UNA Resistor Program	mable Cain	±50nA Software Programmable Cain	±70nA Peristor Progra	mmable Cain	
Gain Range		1 to 1000V/V	mable Gam	1 2 4 8V/V	1 to 1000V/V	animable Gam	
CMV Range		±10V min	,	*	•		
CMRR (dc - 500Hz)		76dB min		•	•		
Input Settling Time*		20µs max (G = 1)	)	15μs max (G = 1 to 8)	20µs max (G =	1)	
ADC Input Ranges		±2.5V, ±5V, ±10	V, 0 to 10V, 0 to 5V	•	±5V, ±10V, 0V	/ to +10V	
Resolution		12 Bits					
Throughput Rate <sup>5</sup>		25µs max 30.000 Chappel/		•			
Output Codes <sup>1</sup>		Binary, Offset Bi	nary. Two's Complement	•	•		
Nonlinearity Error		±1/2LSB typ (±1	LSB max)	•	•		
Offset Error <sup>6</sup>		Adj. to Zero		•	•		
Gain Error <sup>6</sup>		Adj. to Zero		•	•		
Offset TC		$\pm (1 + \frac{50}{2}) \mu V/^{\circ} C$	C (RTI)	±30µV/°C (RTI)	$\pm (1 + \frac{50}{2}) \mu V$	'/°C (RTI)	
Coin TC		+20mm of ada (	C (BTI)	the second se	- (- G /-	<sup>e</sup> c (prp)	
Noise Error <sup>7</sup>		±20ppm of rdg./	C(KII)	±25ppm of rdg./ C (R11)	±20ppm of rdg	./ C (RTI)	
Overall Error $@G = 1^8$		±11.SB max		•	•		
SHA Aperture Delay		90ns		•	•		
SHA Aperture Width		20ns		•	•		
SHA Aperture Uncertainty		5ns	,	•	•		
ANALOG OUIPUT		DTI 1261					
Output Channels		2		RII-1252-2			
Resolution		12 Bits		2 expandable to 4	1		
Output Ranges1 (with on board	Ref)	+5V, +10V, ±5V	±10V	+5V. +10V. ±2.5V. ±5V. ±10V			
Output Current		±5mA min. @ ±1	ov	••			
Nonlinearity Error		±0.01% max		±0.01%			
Offset Error	1	Adj. to Zero		••			
Gain Error		Adj. to Zero		••			
Gain TC <sup>10</sup>		$\pm 25\mu V/C$		$\pm 25\mu V/C$			
Settling Time <sup>8</sup> (for 20V step to	±0.01%)	10us max		**			
Input Codes	,	Binary, Two's Co	mplement, or Offset				
		Binary	• •	••			
Reference		-10.00V or -5.00	v	+6.3V ±2%		•	
OTHER OUTPUTS (RTI-1252 (	ONLY)	V/I Current Loop	Converter (Option 0A08	) 4 Logic Drivers			
Type		ISA-S50.1, Type	3, Class L	Open Collector			
Output Current Range		4-20mA		300mA sink @ 0.7V		0	RDERING GUIDE
Supply Voltage Range		+15V to +30V		+30V max		MODEL	
Offset Error		Adi to Zero				NUMBER	DESCRIPTION
Gain Error		Adj. to Zero					
Offset TC12		±0.4µA/°C				RT1-1250-R	Input Board with Resistor
Gain TC <sup>12</sup>		±30ppm/°C				RT1-1250-S	Input Board with Software
Nonlinearity Error (V/I Only)		±0.01% max				DTI 1251	Programmable Gain Amplifier
Settling Time-		50µs max to 0.02	.%				Programmable Gain Amplifier and
POWER REQUIREMENTS						BTI-1252-2	Two Multiplying DAC's
+5V +5%		1 4 4	1 5 4	R11-1252	V/I (2)	RTI-1252-4	Output Board with Four Trimmed DAC's
		1.77	1.5A	1.4A	1./A .	ACCESSORIES	
MICROCOMPUTER INTERFAC	CE					0408	4.20m0 V/I Module
Complies with D.E.C. bus loa	iding and ele	ectrical specificatio	'ns			0A10	Multiplexer Expansion Kit
TEMPERATURE RANGE						0412	(2 ea. HI-0508A-5) 12-Bit DAC for BTL1252-2
Operation	0 to +70°C	C (0 - 95% RH non	-condensing)				
Storage	-55° C to +	85°C				CONNECTORS	
MECHANICAL						AC1553 AC1554	50 Pin, Flat Cable Connector* 26 Pin, Flat Cable Connector*
Size	5" × 8.5" (	(per D.E.C. Drawin	g)			AC1560	14 Pin, Dip Plug Connector*,
weight	10 ounces	C					
Connectors	See Ordern	ng Guide				*All Connectors	Have 3' of Color Coded Cable Attached
*Same as for RTI-1250-R *Same as for RTI-1251-R							. ,

Specifications subject to change without notice.

NOTES User selectable by wire-wrap jumpers. <sup>1</sup>The full scale input signal range is the A/D converter range divided by the gain of the instrumentation amplifier. <sup>1</sup>The user may install one resistor per channel (4 max with RTI-1251, 8 max with RTI-1250) to convert the <sup>1</sup>The user may install one resistor per channel (4 max with RTI-1251, 8 max with RTI-1250) to convert the <sup>1</sup>The input current spans can be derefore be accommodated. <sup>2</sup>This time can overlap A/D conversion period. The setting time increases to 50µs @ G = 1000. <sup>3</sup>The effective throughput rate idstermined by the user's software data handling capability. The max through-put rate listed is exclusive of the CPU interface operations which may or may not be completed during the sub-system's conversion time. The user's software and interface time must be added to the conversion time to deter-mine the maximum effective throughput rate. <sup>4</sup>For any one programmable gain setting other than the one used during calibration.

<sup>7</sup> Noise error increased to ±1/2LSB max @ G = 8 for the SPG models and to ±1LSB @ G = 100 for the RPG models. \*Overall error increases to ±2LSB max @ G = 8 for the SPG models and 2LSB max @ G = 500 for the RPG <sup>10</sup>Overall error increases to 24258 max e G = 6 to use 2 cu incorta and a 258 max e G = 6 500 Ω may be models. <sup>10</sup> The current loop load resistance range is 0Ω to 450Ω with a +15V supply. A load resistance of 500Ω may be used with > 1.8V supply. <sup>10</sup> Temperature coefficients are specified for the ±10V full scale range. <sup>11</sup> The on-board references are also available at the card edge. Users must limit any current load to less than 2mA. External reference inputs have an input impedance of greater than 5kΩ. <sup>12</sup> Specified for V/I module only (P/N 0A08).

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### High Performance STD Bus Compatible Analog I/O Subsystems

#### FEATURES

RTI-1260 ANALOG INPUT CARD 32 Single-Ended/16 Differential Channels User Configurable Gains of 1 to 1000 12-Bit A/D Resolution NEW FEATU

RTI-1262 ANALOG OUTPUT CARD Me 4 Analog Output Channels po 12-Bit D/A Resolution Optional 4-20mA Current Loop Outputs

00 NEW FEATURE Memory Mapped or Memory Selectable Port I/O Selectable

GENERAL

### Low Cost

Single +5V Power Requirement Memory Mapped or Port I/O Selectable Compatible with All STD CPU Cards



**RTI-1260/1262** 

### **GENERAL DESCRIPTION**

The RTI-1260 Series products from Analog Devices are high performance analog input and output cards compatible with the STD bus. They provide a cost effective and convenient means of interfacing your microcomputer to the real (i.e., analog) world. The cards feature 12-bit resolution, resistor programmable gain for low-level signals, analog channel expansion capabilities, 4-20mA outputs and on-board dc/dc converter.

The series consist of an analog input card (RTI-1260) and an analog output card (RTI-1262). The cards interface to the STD bus as either a memory mapped or an I/O port peripheral through a user-selection jumper option.

The RTI-1260 Analog Input Card provides data acquisition for 16 single-ended or 8 differential channels with optional expansion to 32 single-ended or 16 differential channels. The instrumentation amplifier is user configurable for gains of 1 to 1000. Combining this with a sample-hold circuit and 12-bit a/d converter, the data acquisition section features  $\pm 0.01\%$  accuracy, 12-bit resolution and throughput rates up to 25kHz.

The RTI-1262 Analog Output Card uses four 12-bit d/a converters to provide independently programmed voltage output channels. In addition, two channels can be converted to 4-20mA outputs by using optional voltage-to-current modules which install on the board.

Reliable analog connections are made using 3M's "Scotchflex"

socket and header connectors which enables a flat ribbon cable to be combined with gas tight and corrosion resistant connectors. An optional screw termination panel is also offered for simple and convenient field wire connections.

All cards have an operating temperature range of 0 to  $+70^{\circ}$ C and come complete with dc/dc converter, allowing them to operate from the microcomputer's +5V supply.

### ORDERING GUIDE

ADI Model No.	Description	Used On
Cards		
RTI-1260	Analog Input Card	-
RTI-1262	Analog Output Card	-
Accessories		
OA08	V/I converter provides 4-20mA output	RTI-1262 (2 max)
	from D/A. One required per channel.	
OA10	Multiplexer Expansion Kit expands	RTI-1260
	channel capacity from 16SE/8D to	•
	32SE/16D. One required per board.	
Mating Connectors		
AC1553	50-pin flat cable connector with 3'	
	color coded cable (Analog Input).	RTI-1260
AC1554	26-pin flat cable connector with 3'	
	color coded cable (Analog Input).	RTI-1262
AC1585-6	3B01 to RTI-1260	RTI-1260
AC1585-7	3B01 to RTI-1262	RTI-1262
Screw Termination I	Panel	
AC1585-1	Screw terminal connection to field wiring.	RTI-1260
AC1585-2	Screw terminal connection to field wiring.	RTI-1262
User's Manual*		
AC1563	User's Manual for RTI-1260/1262	

NOTE \*A user manual is furnished with each shipment. Additional copies are available under this part number.

		INPUT				OUTPUT			
Card Type	Model No.	Channel C STD	apacity OPT	Gain Range	A/D Resolution	Channel Capacity	D/A Resolution	4-20mA (OPT)	
Analog Input Analog Output	RTI-1260 RTI-1262	16SE/8D	32SE/16D	1-1000 - N/A	12 Bits	4	N/A 12 Bits	2	

RTI-1260/1262 Function Chart

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

### **SPECIFICATIONS**

RTI-1260 ANALOG INPUT CARD					
Number of Input Channels	16 Single-Ended or 8 Differential (Jumper Selectable)				
	Expandable to 32 Single-Ended or 16 Differential Using				
	Two Plug-In Multiplexers (ADI Part #OA10)				
Input Overvoltage Protection <sup>1</sup>	± 35V (Dielectrically Isolated)				
Input Impedance	$>10^{8}\Omega$				
Input Bias Current	$\pm 50 nA$				
Analog Connector	3M #3433, 50 pin				
A/D Input Ranges <sup>2</sup>	$0 \text{ to } + 10 \text{V}, \pm 10 \text{V}$				
A/D Resolution	12 Bits (4096 Counts)				
A/D Output Codes <sup>2</sup>	Binary, Offset Binary, Two's Complement				
Instrumentation Amplifier Gain Ranges	1 to 1000V/V (Resistor Programmable Gain)				
Gain Equation	$G = 1 + \frac{20k\Omega}{R_G}$				
A/D Conversion Time	25µs				
System Throughput <sup>3</sup>	25,000  Channels/sec (G < 150)				
	20,000 Channels/sec $(150 < G > 300)$				
	11,000 Channels/sec $(G = 1000)$				
Common Mode Voltage (CMV)	$\pm 10V \min$				
Common Mode Rejection (CMR)	78dB				
Linearity	+ 1/2LSB				
Differential Nonlinearity	+ 1LSB				
Total System Error (Adjustable to Zero)	$\pm 0.01\% \text{ of FSB}$ (Gain = 1 to 10)				
	$\pm 0.05\% \text{ of FSR}$ (Gain = 100)				
	$\pm 0.05\%$ of FSR (Gain = 1000)				
Temperature Coefficient	20.1700115K (Gam = 1000)				
Gain	$\pm 30$ nmm/°C of FSP (G = 1)				
Offset	$\pm 100$ mm/°C of ESP (G = 1000)				
Oliset	$\pm 100ppm/CortESP(G-1)$				
	$\pm 100$ ppm/°C of FSR (G = 1000)				
INTERFACE PARAMETERS					
Compatibility	Meets all Electrical and Mechanical STD Bus Specifications				
Implementation	Memory Mapped I/O Compatible with All CPU Types				
<b>FF</b>	Port Mapped I/O Compatible with 8080, 8085, 8086 and Z-80				
	Family of CPUs				
Address Selection	3 Contiguous Bytes in a 16 Byte Block. (Jumper Selectable				
	in Any One of 256 Locations in 64K of Memory Space				
Port Selection	3 Contiguous Ports in a 16 Port Block (Jumper Selectable				
	on Any 16 Port Boundary in Either an 8-Rit or 16-Rit Port Image				
Expansion Options	MFMFX and IOFXP Fully Supported with Jumper Selectable				
Expansion Options	Enable High, Enable Low or Ignore Expansion Options				
POWER REQUIREMENTS	$+ 5V \pm 5\%$ (@ 450mA (On-Board dc/dc Converter Generates an Isolated $\pm 15V$ to Power the Data Acquisition Components.)				
TEMPERATURE					
Operating	$0$ to $\pm 70^{\circ}$ C				
Storage	$-55^{\circ}$ C to $+85^{\circ}$ C				
Storage					

UV with power off. <sup>2</sup>User selectable with wire-wrap jumpers. <sup>3</sup>Does not include CPU latency time.

Specifications subject to change without notice.

### **STD Bus Compatible ANALOG DEVICES** Sensor Based Data Acquisition Subsystem

### FEATURES

Direct Analog Connection Thermocouples, RTDs, mV and V Signals, Strain Gages, Process Currents (4-20mA) Complete Signal Conditioning Input Protection, Filtering, Isolation, Amplification **Cold Junction Compensation, Excitation** Microcomputer Based Linearization, Conversion to Engineering Units Single +5V Power Requirement

### APPLICATIONS

Industrial Process Control Laboratory and Scientific Data Acquisition Food Process Equipment Medical Equipment **Production Machinery Energy Monitoring** Data Logging

#### **GENERAL DESCRIPTION**

The RTI-1270 Series is the first easy-to-use, easy-to-implement analog subsystem optimized for temperature and low level signal measurements. This series consist of an RTI-1270 A/D-CPU Base card and two RTI-1271 Signal Conditioning/Multiplexer cards.

This subsystem is a complete solution to system integrators who must interface thermocouples (J, K, S, T, R, E, B, W type), RTDs (1000 platinum), strain gage mV, V or mA signal to the STD bus in the presence of electrical noise, ground loops and high common mode voltages.

The RTI-1270 Subsystem include screw terminal connection, sensor signal conditioning, optional  $\pm 1000V$  isolation, 16-channel analog multiplexing, 13-bit A/D conversion, data manipulation (cold junction compensation, linearization, conversion to engineering units) and maps as a contiguous block of memory onto the STD bus.

All signal conditioning is already done with cold junction compensation provided for thermocouples and excitation for RTDs. The input data is scaled, linearized and converted to engineering units which allows you to simply connect your sensors via industrial screw terminals, plug the cards into the STD bus and go. Modular design permits the ability to mix and match on a four-channel bases and expand to a sixteen channel input subsystem.

The on-board intelligence performs all data acquisition control and preprocesses the data, thus reducing the software overhead by the STD bus host CPU. The RTI-1270 Subsystem requires a single +5V power supply and will operate with any STD bus system employing a Z80 or 8085 CPU.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

### **RTI-1270** Series



### APPLICATIONS

The RTI-1270 Subsystem can be easily integrated into a broad range of industrial and laboratory measurement applications. Whether it be on-line food canning process monitoring or recording temperatures in a research lab, this subsystem is an ideal choice.

### USER BENEFITS

Ease of Use: Direct sensor interface via screw terminal connectors, output in engineering units provide fast and easy system implementation.

Integral Signal Conditioning: High quality signal conditioning provides input protection and isolation, cold junction compensation for thermocouples, RTD excitation, and sensor linearization and scaling, eliminating the need for expensive external signal conditioning.

Flexible: Modular design allows the mix and match of different input types on a four-channel basis and up to sixteen analog signals per subsystem.

Reliability: State-of-the-art design combines high performance with reliability using transformer-isolated analog input multiplexers. This provides common mode voltages of  $\pm 1000V$  and normal mode input protection to 130V rms.



RTI-1270 A/D-CPU BASE CARD RTI-1271 SIGNAL CONDITIONING CARD



### FUNCTIONAL DESCRIPTION RTI-1270 SUBSYSTEM

The RTI-1270 and RTI-1271 are a multicard subsystem which interfaces analog signals to the STD bus. The subsystem consists of an RTI-1270 A/D-CPU base card and up to four RTI-1271 signal conditioning/multiplexer cards. All cards are electrically and mechanically compatible with the STD bus with the exception being the RTI-1271's component height. This requires the use of a backplane with 0.75" spacing or the use of two card slots.

The RTI-1271-A and RTI-1271-B are signal conditioning/multiplexer cards which accommodate a wide range of input ranges and signal types. Each card accepts 4 differential analog signals and provides analog signal conditioning for the RTI-1270. These high performance signal conditioning cards include input protection, isolation (RTI-1271-B) and common mode rejection, multiplexing, filtering and amplification: The cards can be configured to accept a wide range of inputs by simple DIP switch programming. Connection to the RTI-1270 is made through a flat 20-pin ribbon cable.

The RTI-1270 base card is the heart of the subsystem. It includes the A/D converter, a  $\mu$ P and bus interface logic. The 13-bit, integrating A/D converter offers excellent noise immunity of 50/60Hz noise pickup and can be set to continuously convert at either 15 or 30 conversions per second. The onboard  $\mu$ P runs independent of the STD bus host and controls all data acquisition functions. The resultant data, stored in 1k of common RAM can the be read by the STD CPU HOST.

### **RTI-1271 SIGNAL CONDITIONING CARD SELECTION**

All four channels of the RTI-1271 are dedicated to a single input range and accept the input ranges listed in Table I. The specific input range/type for the individual cards is switch selectable. Upon initialization, the switch is read by the  $\mu$ P and its code is stored in RAM. This information is used to direct the execution of linearization and unit conversion routines. Although the input range/type cannot be mixed on a card, several RTI-1271 cards each having a different input can be supported by the RTI-1270 A/D-CPU card.

# $\begin{array}{c|c} Signal \ Conditioning \ Card \\ RTI-1271-A \\ Input \ Type/Span \\ dc, \pm 25mV, \pm 50mV, \pm 100mV \\ dc, \pm 1V, \pm 5V, \pm 10V^{\star} \\ dc 0-1mA, 0-20mA, 4-20mA^{\star\star} \\ Type \ J,K,S,T,R,E,B,W \ Thermocouple \\ 100\Omega \ Platinum \ RTD \\ Strain \ Gage \pm 30mV, \pm 100mV \ Inputs \\ AD590, \ AC2626 \ Temperature \ Sensor \\ \end{array}$

\*Requires resistor divider kit.

\*\*Requires shunt resistor kit.

#### Table I. Signal Conditioning Card Selection

#### Isolated vs. Nonisolated Inputs

The RTI-1270-A accepts many of the same input types/ranges as the RTI-1271-B; however, the RTI-1271-B includes  $\pm 1000V$ isolation to eliminate ground loops and solve common mode voltage problems. A reliable transformer isolation design is used and the analog inputs meet the IEEE Standard for transient voltage protection (472-1974:SWC). This card is recommended for industrial applications such as measuring grounded thermocouples.

#### **Analog Connections**

The RTI-1271 provides the signal conditioning for a wide range of sensor and analog input ranges. Field wiring connections are made by means of industrial screw terminals which handle up to 14 gauge wire. A temperature sensor is mounted next to the screw terminal to monitor the temperature and provide cold junction compensation for thermocouple inputs.

#### Signal Conditioning

The RTI-1271 is optimized for high performance measurements by providing normal mode input protection (130V rms),  $\pm 1000V$  common mode voltage isolation (RTI-1271-B), low pass filtering and low drift amplification. Signal integrity is further preserved by excellent normal mode rejection and high immunity to electromagnetic fields and RFI.

### VOL. II, 17-20 µCOMPUTER ANALOG I/O SUBSYSTEMS

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### **Measurement-and-Control Subsystems**

### FEATURES

Analog Inputs Thermocouples, RTDs, Strain Gages, AD590s High and Low Level Voltages, Current Loops ±1000V Isolated and Nonisolated **Analog Outputs** Voltage and Current ±1000V Isolated and Nonisolated **Digital Inputs/Outputs Contact Closures** ac and dc Signals (High and Low Level) Microcomputer Based Linearization, Unit Conversion, Limit Checking **Powerful Command Set** Serial Communications 20mA or RS-232C Integral Power Supply ac or +24V dc

#### **GENERAL DESCRIPTION**

The  $\mu$ MAC-4000 Measurement and Control System is a complete, low cost solution designed to simplify process to computer interface in a wide range of industrial automation applications.

The  $\mu$ MAC-4000 offers an unprecedented set of hardware and software capabilities that can be easily tailored to virtually any automation application. Modular design permits expansion within the system and the flexibility to accept a variety of analog and digital input and output functions.

The  $\mu$ MAC-4000 is optimized for high performance measurement and control. Analog inputs handling capability offers reliable operation in harsh, electrically noisy, industrial environments. The high performance is assured by high quality signal conditioning featuring input protection,  $\pm$  1000V channel-to-channel and input-to-output isolation, high common mode rejection, filtering, low drift amplification and 13-bit A/D conversion. A unique plug-in module approach allows the selection of standard signal conditioning modules for direct connection to a wide range of sensors. The  $\mu$ MAC-4000 scales, linearizes and converts the input data to engineering units.

Both analog and digital control capability is provided by the  $\mu$ MAC-4000 system. Analog outputs feature 12-bit resolution, voltage and 4-20mA/0-20mA current outputs with  $\pm$  1000V isolation, as well as increment/decrement and bumpless transfer for precise control in either manual or computer mode. Digital I/O offers direct interface to contact closures, TTL levels or high level ac and dc voltages.

The  $\mu$ MAC-4000 system is designed to operate with any host computer which has a 20mA or RS-232C serial port. The  $\mu$ MAC-4000 can be either used as a local front end or located up to 10,000 feet from the host. A powerful command set is included in the  $\mu$ MAC's firmware which allows control via the serial interface bus. Once the command is executed, the results are transmitted back to the host in an ASCII format-at speeds up to 9600 baud.



μ**MAC-4000** 

The  $\mu$ MAC-4000 system requires either ac line power or +24V dc. Circuitry is provided to detect intermittent ac power losses and switch automatically to an external battery backup mode.

A wide variety of packaging options are available to match user requirements. These options include single board enclosures, card cage/rack mounting or NEMA enclosures.

### APPLICATIONS

The  $\mu$ MAC-4000 is a versatile, self-contained measurement and control system designed for a broad range of industrial and laboratory applications. It is extremely useful in both control room and remote locations where monitoring and control of temperature, pressure, flow, analog and digital signals are required.

#### DESIGN FEATURES AND USER BENEFITS

Ease of Use: Direct sensor interface via screw terminal connectors, output in engineering units, powerful command set, make the  $\mu$ MAC-4000 extremely easy to use.

Integral Signal Conditioning: High quality signal conditioning provides input protection and isolation, cold junction compensation for thermocouples, RTD excitation, and sensor linearization and scaling, climinating the need for expensive external signal conditioning.

High Noise Rejection: The  $\mu$ MAC-4000 preserves high system accuracy in electrically noisy environments, providing excellent common mode and normal mode noise rejections and RFI/EMI immunity.

**Control Capability:** Analog and digital outputs are provided to control motor speeds, dictate valve positions and drive actuators.

Features such as isolation, bumpless transfer and DAC readback are included in the design.

**Expandability:** Expansion capability to 384 analog input channels, 256 analog output channels, 1088 digital inputs and 1088 digital outputs on one 20mA serial line using the  $\mu$ MAC-4000 with expander boards.

MAC-4000 MAC-4010/4015 Analog Input Expander MAC-4030 Analog Output Expander MAC-4020 High Level

Digital I/O Expander

Digital I/O

INPUT/OUTPUT

### **Analog Inputs** Thermocouples: J, K, T, S RTDs: 100Ω Platinum Solid State Temperature Sensors: AD590 or AC2626 Strain Gage Transducers: $\pm 30mV$ and $\pm 100mV$ spans dc Voltage: $\pm 25 \text{mV}$ , $\pm 50 \text{mV}$ , $\pm 100 \text{mV}, \pm 1 \text{V}, \pm 5 \text{V}, \pm 10 \text{V}$ dc Current: 4 to 20mA, 0 to $\pm 1$ mA, 0 to $\pm 20$ mA Common Mode Voltage: ±1000V pk (chan/chan/gnd)-isolated input modules Input Protection: 130V rms continuous IEEE-472 (SWC) transient A/D Converter: 13-Bit Dual Slope Scan Rate: 15 or 30 chan/sec **Analog Outputs** Voltage: $\pm 5V$ , $\pm 10V$ 0 to $\pm 15V$ , 0 to $\pm 10V$ Current: 4 to 20mA, 0 to 20mA Resolution: 12-Bits Isolation: ±1000V pk (chan/ chan/gnd)-current outputs Output Protection: 130V rms **Digital Inputs** Compatibility: TTL signals or

### $\mu$ MAC-4000 System Configuration The $\mu$ MAC-4000 system consists of a family of boards providing the measurement and control functions through interfaces to analog and digital inputs and outputs and the host computer.

The system includes: the  $\mu$ MAC-4000 Master Board, the  $\mu$ MAC-4010 Analog Input Expander, the  $\mu$ MAC-4030 Analog Output Expander, the  $\mu$ MAC-4040 Digital I/O Expander, and the  $\mu$ MAC-4020 High Level Digital I/O Subsystem. You select only the functions which are required.

A typical configuration can consist of a single  $\mu$ MAC-4000 Master Board which accepts 4, 8 or 12 analog inputs and includes 8 digital inputs and 8 digital outputs. A multiple board configuration (cluster) consists of one  $\mu$ MAC-4000 Master Board and up to six Expander Boards selected in any combination from up to three  $\mu$ MAC-4010's and/or  $\mu$ MAC-4015's, up to four  $\mu$ MAC-4030's and up to four  $\mu$ MAC-4040's. A  $\mu$ MAC-4000 Master Board must reside in each cluster since it contains the communications and intelligence.

### µMAC-4000 System Specifications

contact closures and µMAC-4020 for high level inputs Isolation: ±300V pk **Digital Qutputs** Compatibility: TTL signal and µMAC-4020 for high level outputs **Channel Capacity per Board** µMAC-4000 and µMAC-4010 12 Analog Inputs 8 Digital Inputs 8 Digital Outputs µMAC-4015 12 Analog Inputs µMAC-4030 8 Analog Outputs µMAC-4040 32 Digital Inputs 32 Digital Outputs µMAC-4020 16 High Level Digital Inputs and Outputs Capacity per Cluster **48** Analog Inputs 32 Analog Outputs 152 Digital Inputs 152 Digital Outputs **Total System Capacity** 8 addressable clusters on



one serial communication port COMMUNICATIONS

Mode: 4 wire full duplex 20mA current loop or RS-232C Format: Serial Asynchronous ASCII Rate: Selectable from 110 to 9600 baud Distance: RS-232C: 50 ft (15m) 20mA, 10,000 ft (3048m) Protocol: Command/Reply (prompted)

### POWER

100/115/220/240V ac, 50/60Hz or + 24V dc

 $\begin{array}{l} \textbf{MECHANICAL} \\ \text{Single Board: } 9.5'' \times 13'' \\ & (241.3 \times 330.2 \text{ mm}) \\ \text{4-Slot Card Cage: } 14.8'' \times 11.2'' \times 10.3'' \\ & (376.0 \times 284.5 \times 261.6 \text{ mm}) \\ \text{7-Slot Card Cage: } (15.75'' \times 19'' \times 11'' \\ & (400.0 \times 482.6 \times 279.4 \text{ mm}) \\ \textbf{ENVIRONMENTAL} \\ \text{Operating Temperature: } 0 \text{ to } + 60^\circ\text{C} \end{array}$ 

Operating Temperature: 0 to +60°C Humidity: meets MIL-STD 202, Method 103 Vibration: meets MIL-STD 167-1 Magnetic Field Immunity: 200 gauss RFI Immunity: 5W @27MHz @3 ft.

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### Complete BASIC Programmable Stand-Alone Measurement and Control System

### μMAC-5000

### FEATURES/BENEFITS

Low Cost, Completely Integrated Measurement and Control System On a Single Board

- Wide Selection of Functionally Complete Analog and Digital I/O
- Operates from ac or dc Power

Integral Signal Conditioning Allows Direct Connection to a Wide Variety of Signal Sources

- Sensors: Thermocouples, RTDs, Strain Gages, Load Cells, AD590/AC2626
- Millivolt and Voltage Sources
- 4-20mA/0-20mA Process Current Inputs
- Counter or Pulse Inputs Provide for Frequency or Event Counting

Powerful Measurement and Control µMACBASIC Language

- Programs Developed and Run On Board
- Analog and Digital I/O Are Performed By Key Words In BASIC
- Program Storage in PROM or Battery Backed-Up RAM

Advanced µMACBASIC Features

- Functions and Procedures Allow User Defined Key Words
- Advanced Block Structures Allow Modular, Self-Documenting Programs

**Powerful Communications Capabilities** 

- Supports Communications in RS-232C, 20mA, RS-422 and RS-423
- Supports Asynchronous Communications
- Protocol Emulation Easily Accomplished with μMACBASIC

### GENERAL DESCRIPTION

The  $\mu$ MAC-5000 Measurement and Control System is a complete, low cost solution designed to solve a broad range of industrial measurement and control problems. It can be used in applications requiring distributed intelligence or as a local front end.

The  $\mu$ MAC-5000 offers an unprecedented set of hardware and software capabilities that can be easily tailored to virtually any measurement and control application. Modular design permits expansion within the system and the flexibility to accept a variety of analog and digital input and output functions. A powerful Measurement and Control BASIC language,  $\mu$ MACBASIC, is provided with each product.

The  $\mu$ MAC-5000 is optimized for high performance measurement and control. Analog input handling capability offers reliable operation in harsh, electrically noisy, industrial environments. The high performance is assured by high quality signal conditioning featuring input protection,  $\pm 1000V$  channel-to-channel and input-to-output isolation, high common mode noise rejection,



filtering, low drift amplification and 14-bit A/D conversion (13 bits + sign). A unique plug-in module approach allows the selection of standard signal conditioning modules for direct connection to a wide range of sensors. The  $\mu$ MAC-5000 scales, linearizes and converts the input data to engineering units.

Both analog and digital control capability are provided by the  $\mu$ MAC-5000 system. Analog outputs, provided by the  $\mu$ MAC-4030 Analog Output Expander, feature 12-bit resolution, voltage and 4-20mA/0-20mA current outputs with  $\pm$  1000V isolation, as well as the capability of either auto or manual operation with bumpless transfer and programmable slew rate. Digital I/O offers direct interface to contact closures, TTL levels or high level ac and dc voltages. Two pulse accumulator or frequency inputs are available on each  $\mu$ MAC-5000 and both have a 32-bit counter and operate over a 0 to 20kHz frequency range.

The  $\mu$ MAC-5000 board is designed to operate efficiently in stand-alone applications. The  $\mu$ MAC-5000, which has two serial ports, can be used with any host computer. The local port can communicate in RS-232C, RS-422, or RS-423 and is primarily used for program development or for supporting a local printer or terminal. The remote port supports RS-232C, 20mA, RS-422, and RS-423. In supervisory control applications, the  $\mu$ MAC-5000 can be used either as a local front end or located up to 10,000 feet from a host and can operate at speeds up to 19.2K baud in an asynchronous mode.

The  $\mu$ MACBASIC language was designed to address the needs of both the experienced and inexperienced programmers. The language provides the less experienced programmer with a powerful version of the popular BASIC programming language which allows programmers with only a fundamental knowledge of BASIC to easily write programs.  $\mu$ MACBASIC also provides the experienced programmer with a truly modular, structured language which simplifies the task of writing larger, more complex programs and provides higher quality programs.

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.



Photograph of the µMAC-5000, showing the system architecture.



System functional block diagram.

## Overview of the µMAC 5000

1) Multiplexed Signal-Conditioning Modules. Three plug-in 4-channel signal conditioning modules provide multiplexing, preamplification, and optional transformer isolation and bridge excitation. Four mixmatchable module types are available to handle many input sources: thermocouples, RTDs, strain gages, 4-20mA current loops, and millivolt, volt, and milliampere signals.

2) Programmable-Gain Amplifier (PGA). Digital logic sets the gain of the PGA to amplify the preamplified input signal to the full-scale range of the a/d converter (hidden).

3) A/D Converter. An integrating converter provides resolutions from 14 bits (13 bits + sign) to 11 bits, depending on the desired number of conversions per second (hidden).

4) Intelligence. A 16-bit  $\mu$ C with 80K bytes of ROM and 32K bytes of battery backedup RAM supports stand-alone applications. Plug-in sockets support an optional 16K Bytes of ROM and 32K bytes of RAM. The  $\mu$ MAC BASIC compiler and operating system use 80K bytes of ROM and 12K bytes of RAM. A DIP-switch option permits running programs from either ROM or RAM.

5) Communications. Two serial ports connect the μMAC-5000 to any host computer. Local and remote ports communicate in RS-232C, RS-422, or RS-423. The remote port also supports 20-mA current loops.

6) Power Supply. An ac/dc converter and dc/dc converter generate +5V and  $\pm 15V$  system voltages from an ac power line or +24V dc source. Using both, the system can detect brownouts or power outages and switch to dc without disturbing program execution. Factory-set line-voltage options are: 100V, 115V, 220V, or 240V.

7) Digital I/O. 8 digital inputs, optically isolated for 300V peak, can sense contact closures or accept TTL signals. The 8 latched-TTL outputs can sink up to 24mA. The  $\mu$ MAC-4020, connected to the digital I/O port, controls and monitors digital signals at line voltages. Two counters provide for pulse accumulator and frequency inputs.

8) **Expansion Port.** The expansion port provides for up to 6 mix/match expansion boards to greatly increase the number of available analog and digital I/O channels.



### SYSTEM CONFIGURATION

A single board system configuration consists of one  $\mu$ MAC-5000 Programmable Master Board which accepts 4, 8, or 12 analog inputs and includes 8 digital inputs and 8 digital outputs. Two of the digital inputs can optionally be used as pulse accumulators or frequency inputs.

A multiple board configuration (cluster) consists of one  $\mu$ MAC-5000 programmable Master Board and up to six Expander Boards. The  $\mu$ MAC-4000 Series of expander products provides a wide range of analog and digital I/O capability and a cost effective solution to large point applications (see Table I). A  $\mu$ MAC-5000 must reside in each cluster since it contains the communications capability and intelligence. A network using up to 16 clusters in a multidrop configuration allows your host computer to monitor and control up to 1344 analog or 4864 digital points or varying combinations of both types from a single 20mA or RS-422 communications line.

### COMMUNICATIONS

The  $\mu$ MAC-5000 System is designed to operate in stand-alone applications and can communicate with any host computer or terminal that has a 20mA, RS-232C, RS-422, or RS-423 port. The  $\mu$ MAC-5000 has two serial communication ports. Both ports have 256 byte RAM-buffers. A full duplex USART is used to receive and transmit data at selectable baud rates. The  $\mu$ MAC-5000's serial link allows use of either a party line (Figure 1) or radial system configuration.

The local communications port is primarily used for program development and will support RS-232C, RS-422, and RS-423. It can also be used to support a printer or terminal in a run time environment. This port is capable of communicating from 150 to 19.2K baud in an asynchronous mode. The local port can be used in either a full duplex or half duplex mode and can be used in a party line configuration when RS-422 is used.

The remote communication port supports RS-232C, 20mA, RS-422 and RS-423. In the asynchronous mode, it can operate from 110 to 19.2K baud. This port can be used in either a full duplex or half duplex mode and can be used in either a party line or radial configuration. The remote port has control lines (RTS, DCD, DTR, and CTS) which allow connection to a modem for long distance communications. The 20mA loop is optically coupled for harsh industrial environments.

Model	Function	Description
µMAC-4010	–Analog input –Digital I/O	-Up to 12 channels using QMX modules -16 channels digital I/O
µMAC-4015	–Isolated analog input	-Low cost, 12 channels of same input type -1500V isolation
µMAC-4030	-8 channels analog output	Voltage or isolated 4-20mA outputs Readback, bumpless transfer
μMAC-4040	–Digital I/O	-32 channels isolated digital inputs -32 channels digital outputs (TTL)
µМАС-4050	Multi- function digital I/O 8 channels, mixed function	-Pulse accumulator -input -Frequency input -Pulse output -Time proportional output
μMAC-4020	-Interface subsystem to high level ac and dc voltages and currents	–Solid state relay subsystem 16 channels, mix of input and output functions

Table I. μMAC Series Expander Boards (See Data Sheet)



Figure 1. Party Line Connection (Multidrop)

### SPECIFICATIONS µMAC-5000 Board Features

Input Types

12 channels, mix and match

Thermocouples: J,K,T,S,R,E,B,W (linearized) RTD: 100Ω Platinum (linearized) Strain Gage: 30mV and 100mV spans DC Voltage: 25mV to 10V

Process Currents: 0-1mA, 4-20mA, 0-20mA Inputs Selectable by 4-channel QMX module—mix 3 types per board

QMX03, 04 modules isolated to 1000V channel-to-channel, input-to-output with IEEE-472 (SWC) transient protection

A/D Converter: 14-bit integrating

### Digital I/O

8 channels isolated digital or contact closure inputs
 8 channels digital outputs
 Connector-compatible with μMAC-4020 high-level solid-state
 relay subsystem

Pulse Inputs (optional use of two digital inputs)
2 channels of frequency or pulse accumulator inputs
32 bits pulse accumulation: 20kHz max frequency

### Two Communication Ports.

4-wire full duplex 256 byte RAM buffered; asynchronous Selectable baud rate: 110 to 19,200 baud Distance: 20mA-10,000 ft. (3048m)

RS-232—50 ft. (15m) RS-422—10,000 ft. (3045m) RS-423—1,000 ft. (305m)

8088-Based Microcomputer 32K RAM – expandable

80K PROM 16K user PROM socket

### Power

On-board ac power supply: 100V/115V/220V/240V or +24V dc (used as primary power or back-up to ac line)

#### Environmental

Operating Temperature: 0 to +60°C Humidity: meets MIL-STD 202, method 103 Vibration: meeds MIL-STD 167-1 Magnetic Field Immunity: 200 gauss RFI Immunity: 5W @ 27MHz @ 3 feet

#### Mechanical

μMAC-5000 Board: 9.5" × 13"(241.3 × 330.2mm) μMAC-5000 Board Enclosure: 9.2" × 14.3" × 3"(234.2 × 363.2 × 76.2mm) 2-Board Enclosure: 10" × 15" × 6"(254.0 × 381.0 × 152.4mm) 4-Board Card Cage: 14.8" × 11.2" × 10.3"(376.0 × 284.5 × 261.6mm)

7-Board Card Cage:  $15.75'' \times 19'' \times 11''(400.0 \times 482.6 \times 279.4 \text{mm})$ 

### **µMAC-5000 APPLICATIONS**

Industrial Process Control and Monitoring: Temperature, pressure, flow and digital I/O measurements, and PID loop control are readily performed on the  $\mu$ MAC-5000 in stand-alone applications.  $\mu$ MACBASIC allows for the creation of proprietary algorithms that can be hidden from the end user.

Machine/Boiler/Furnace Control: High immunity to electrical noise, 1000V isolation, 60°C operation, and single board packaging provide highly reliable operation in harsh industrial environments. The  $\mu$ MAC-5000 is an ideal replacement for programmable controllers where analog I/O is required in addition to digital I/O.

**Remote Terminal Units** for data acquisition and control in pipe line, utilities and oil field applications.  $\mu$ MAC-5000 can readily emulate existing protocols with  $\mu$ MACBASIC and is readily integrated into applications requiring distributed intelligence.  $\mu$ MAC-5000 can also be used with modems in remote applications.

Energy Management: The  $\mu$ MAC-5000 is a low cost solution for small point counts requiring a high degree of I/O flexibility in distributed monitoring and control applications – making it a natural for energy management applications.

**Industrial, Government or University R&D:** µMAC-5000's broad functionality, low cost and ease of use make it the logical choice for monitoring or controlling experiments or pilot plants in a lab environment. Programs can be developed and edited with a dumb terminal and stored in battery backed-up RAM or PROM.

Personal Computers as Data Loggers: The  $\mu$ MAC-5000 is an ideal intelligent "front end" to a personal computer which allows it to be used to acquire, log, process, store and display data from a lab experiment or remote process. The  $\mu$ MAC-5000 with a printer can be used as a stand-alone data logger with the capability of sending exception messages to a host. Personal Computers can also be used as program development work stations for the  $\mu$ MAC-5000.



Figure 2. µMAC-5000 Measurement and Control Concept



### **Measurement and Control Systems**

### MACSYM

#### THE MACSYM 150

A 16-bit 8086 CPU combined with an 8087 math processor provide the power necessary for real-time measurement and control.

MACBASIC 3 – a real-time multitasking BASIC optimized for Measurement and Control applications. Special commands have been added to standard BASIC which simplify real-world data acquisition, graphic presentation and control signal output.

High resolution graphics ( $640 \times 240$  pixels) with either a black and white or color display.

The MACSYM family of Measurement and Control Systems is configured around the powerful MACSYM 150 work station. The MACSYM 150 is a 16-bit microcomputer with integral floppy and/or external Winchester disk storage, and internal RAM up to 512K bytes. Specialized I/O cards (Series 100 cards) plug into a six slot internal backplane providing analog, digital, communications I/O and memory expansion.

The MACSYM 350 combines the processing power of the MACSYM 150 with the accuracy, sampling speed, signal conditioning, and local data storage of the MACSYM 200. The MACSYM 200 is an intelligent measurement and control front end which greatly extends the analog/digital capability of the MACSYM 150. The MACSYM 200 provides for software selectable high speed 12-bit or high resolution 16-bit A/D conversion, and has a 16-bit CPU which controls the analog/digital I/O backplane and handles local data processing needs. Analog and digital I/O cards (ADIO cards) can plug directly into the 16 slot backplane of the MACSYM 200. Over thirty ADIO cards are available for interfacing to virtually any real-world sensor, transducer, or actuator. Communication between the MACSYM 150.

Because of this flexible and modular design, a stand-alone MACSYM 150 can be upgraded into a MACSYM 350 with the

#### THE MACSYM 200

A specialized measurement and control front end and I/O card provide for fast, accurate analog and digital measurements.

A family of over 30 analog and digital I/O cards for direct connection to sensors, actuators and contact devices.

Sampling rates to 30kHz.

Auto calibration and 12- or 16-bit resolution for accurate measurement of up to 512 inputs per MACSYM 200.

Configure up to 15 MACSYM 200's over 5000'.

addition of a MACSYM 200. This results in a system with unprecendented power and flexibility. The system has the capability of addressing an extremely wide range of complex computerized measurement and control applications.

The MACSYM product line has four major elements: the MACSYM 150 work station, the Series 100 family of I/O cards, the MACSYM 200 intelligent front end and the ADIO (Analog/ Digital Input/Output) family of I/O cards.

The MACSYM 150 is a 16-bit computer work station with integral disk storage, up to 512K bytes of RAM, black and white or color graphics, and an 82 key detached keyboard.

Series 100 I/O Cards plug directly into the backplane of the MACSYM 150 and provide analog and digital input and output, serial communications, IEEE-488 bus control, RAM memory expansion, and a Winchester disk interface.

The MACSYM 200 is an intelligent measurement and control front end designed around the 8088 16-bit microprocessor and featuring dual mode 12/16-bit A/D conversion, 12-bit sampling rates up to 33,000 samples per second burst mode, and a capacity for monitoring up to 512 channels of I/O.

ADIO (Analog Digital Input Output) Cards plug directly into the MACSYM 200 I/O backplane and provide signal conditioning for a wide range of sensors, transducers and actuators.

### **SPECIFICATIONS**

MACSYM 150 CPU

RAM

MASS STORAGE

### VIDEO DISPLAY GENERATOR

Text

Graphics

VIDEO DISPLAY

**KEYBOARD** 

COMMUNICATIONS

### DATA ACQUISITION

MACSYM 200

CPU RAM/PROM COMMUNICATIONS

DATA ACQUISITION 12-Bit Successive Approximation

16-Bit Integrating Mode

Calibration\*

Temp. Coefficient\* Long Term Stability\*

### ANALOG DIGITAL I/O

MEASUREMENT INPUT Isolated and Nonisolated Analog Inputs Thermocouple Inputs (J,K,T,E,R,S) Strain Gage Input RTD Input

Specifications subject to change without notice

Standard 8086 5MHz 16-bit CPU 8087 math coprocessor 256K bytes RAM

5 1/4" disk drive single-sided, 96 tpi 320K bytes formatted storage 250K bits/sec transfer rate

24 lines × 80 characters blinking, underline, reverse video attributes 640 × 240 high resolution 320 × 240 medium resolution

High resolution 12" green phosphor monitor 82 key detached keyboard with 12 cursor control and editing keys and 10 user definable special function keys

TTL ASCII: Keyboard to console interface RS-422: MACSYM 150 to MACSYM 200 interface

### 5MHz 8088 CPU

26K bytes

307K baud RS-422: dedicated for communicating with the MACSYM 150

0.024% accuracy 25µs conversion speed 33,000 samples/sec burst mode 0.024% accuracy 16.6ms conversion (60Hz systems) 20.0ms conversion (50Hz systems) Self calibration minimizes RTI, RTO and gain errors over changing environmental conditions. ± 3ppm/°C max 25ppm/1000 hours

> ANALOG OUTPUT Unipolar and Bipolar Voltage Output Current Output Loop Powered Analog Output DIGITAL INPUT/OUTPUT Isolated ac and dc Input Isolated Solid State Input/Output Isolated Digital Output Form "A" and "C" Relay Output

### Optional

Up to 512K bytes Hamming Code Error Correction

Second 5 1/4" disk drive for a total of 640K bytes of floppy disk storage

10M byte Winchester disk

Black and white with gray scale

8-color Black and white with gray scale

8-color

RS-232 RS-422, RS-423, 20mA current loop, IEEE-488

16/32 channel 12-bit analog input card, 4/8 channel analog output card, 16 channel digital I/O card

Up to 48K bytes

### PULSE INPUT/OUTPUT

Pulse Counter and Output Frequency Input Priority Interrupt MISCELLANEOUS Watchdog Timer Speech Synthesizer Setpoint/Alarm Blank Breadboard

### Modular AC/DC Power Supplies

Analog Devices' ac/dc Power Supplies are designed to provide OEMs and circuit designers with a broad line of high reliability, regulated and short circuit protected power supplies at low overall cost. These modules are available with 5 volt to 15 volt outputs (single, dual and triple) and current ratings from 25mA to 2 amps. Most Analog Devices' Power Supplies are available from stock in both large and small quantities. Substantial discounts apply on quantity orders.

#### **ADVANTAGES**

Packaged circuit modules have found wide acceptance. Engineers have discovered the convenience and economy of plugin building blocks . . . op amps, logic cards, miniature A/D and D/A converters are now available in wide varieties. Now a complete line of modular power supplies is available from Analog Devices. These encapsulated units are shipped ready to use, at prices below the internal manufacturing cost of most OEM users.

### TRIPLE OUTPUT SUPPLIES

Analog Devices offers four triple output ac/dc designs which are particularly useful in A/D, D/A and signal conditioning applications. Using a triple output supply is often less expensive than purchasing two separate supplies and also saves on space.

Models 972 and 926 provide ±15V @ ±150mA and +5V @ 300mA. Models 974 and 927 provide ±15V @ ±150mA and +5V @ 1000mA. Models 972 and 974 are chassis-mountable while models 926 and 927 are printed-circuit mountable.

#### **5 VOLT 3 AMP SUPPLY**

Models 976 and 928 supplies combine the primary advantages of switching linear regulated supplies in a single, compact package. This +5V 3 amp supply is available in PC-mountable (928) and chassis-mountable models (976).

#### AC/DC POWER SUPPLIES FEATURES

- Current limited short circuit protection
- PC mounted and chassis mount designs
- Single, dual and triple output designs
- Current outputs of 25mA to 500mA for dual output supplies, 250mA to 3A for single output supplies
- Free-air convection cooling—no external heat sink required

#### **GENERAL SPECIFICATIONS FOR ALL MODELS**

Input Voltage: 105V ac to 125V ac, 50 to 400Hz Temperature Coefficient:  $0.02\%^{\circ}$ C Input Isolation: 50M $\Omega$ Breakdown Voltage: 500V rms, minimum

Operating Temperature: -25°C to +71°C

Operating at elevated temperatures may require derating. Consult factory.

Storage Temperature: -25°C to +85°C

Short Circuit Protection: All of the ac/dc Power Supplies employ current limiting. They can withstand substantial overload including direct shorts. Prolonged operation should be avoided since excessive temperature rises will occur.

SPECIFICATIONS	(typical @ +25°C and 115V ac 60Hz unless otherwise noted;
	higher voltage inputs available, consult factory.)

	Туре	Model	Output Voltage Volts	Output Current mA	Line Reg Max %	. Load Reg. Max %	Output Voltage Error Max	Ripple & Noise mV rms Max	Dimensions Inches
		915	±15	± 25	0.2	0.2	± 1%	1 .	3.5×2.5×0.875
T		904	±15	± 50	0.02	0.02	± 200mV - 0mV	0.5	$3.5 \times 2.5 \times 0.875$
		902	± 15	± 100	0.02	0.02	+ 300mV - 0mV	0.5	3.5×2.5×1.25
	Dual Output	902-2	±15	±100	0.02	0.02	+ 300mV - 0mV	0.5	$3.5\times2.5\times0.875$
		920	±15	± 200	0.02	0.02	+ 300mV - 0mV	0.5	$3.5\times2.5\times1.25$
	5 C	925	±15	± 350	0.02	0.02	± 1%	0.5	3.5×2.5×1.62
nted -		921	±12	± 240	0.02	0.02	+ 300mV - 0mV	0.5	3.5×2.5×1.25
10		906	5	250	.0.02	0.04	±1%	1	3.5 × 2.5 × 0.875
÷,	Circula.	903	5	500	0.02	0.04	±1%	1	3.5×2.5×1.25
5	Single	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
ĕ	Output	922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
2 A		928	5	3000	0.05	0.10	± 2%	5(typ)	$3.5 \times 2.5 \times 1.25$
1	_	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+ 5	500	0.02	0.05	±1%	0.5	
		926	±15	±150	0.02	0.02	± 2%	0.5(typ)	$3.5 \times 2.5 \times 1.62$
			+ 5	300	0.02	0.10	± 2%	1.0(typ)	
	Iriple	927	±15	±150	0.02	0.02	± 2%	0.5(typ)	3.5×2.5×1.62
	Output		+ 5 -	1000	0.02	0.10	± 2%	1.0(typ)	
		2B35J	±15	±65	0.08	0.1	(-0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15*	125	0.08	0.1		0.25	
1		2B35K	±15	±65	0.01	0.02	(-0, +300 mV)	0.5	3.5 × 2.5 × 1.25
			+1 to +15*	125	0.01	0.02		0.25	
		952	±15	±100	0.05	0.05	± 2%	1	$4.4 \times 2.7 \times 1.44$
T	Dual	970	±15	± 200	0.05	0.05	± 2%	1	4.4×2.7×1.44
2	Output	973	±15	± 350	0.05	0.05	± 2%	1	$4.4 \times 2.7 \times 2.00$
g	-	975	±15	± 500	0.05	0.05	± 2%	1	4.4×2.7×2.00
ŵ	Single	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.44
Sis	Output	976	5	3000	0.05	0.10	± 2%	5(typ)	$4.75 \times 2.7 \times 2.00$
has		972	±15	±150	0.02	0.02	± 2%	0.5(typ)	4.75×2.7×1.45
Ŷ	Triple		+ 5	300	0.02	0.10	± 2%	1.0(typ)	
1	Output	974	±15	±150	0.02	0.02	± 2%	0.5(typ)	$4.75 \times 2.7 \times 1.45$
	•		+ 5	1000	0.02	0.10	± 2%	1.0(typ)	

\*Resistor Programmable

#### POWER SUPPLIES VOL. II, 20-1

### **Modular DC/DC Converters**

Analog Devices' compact dc-dc converters satisfy a wide variety of floating power requirements in analog (Computational Circuits, Op Amps, Instrumentation Amps) and digital (a-d/d-a) applications. Available in five power levels of 1 watt, 1.8 watt, 4.5 watt, 6 watt and 12 watt, these designs offer accurate (±0.05% max error), regulated outputs with very low noise. Most models are high efficiency (typically over 60% at full load) that feature complete 6-sided continuous shielding for EMI/RFI protection.

#### **DUAL OUTPUT MODELS**

Logic to analog power conversion is available with several models delivering floating power ( $\pm 12V$  and  $\pm 15V$ ) from logic power sources ( $\pm 5V$ ). This permits analog networks to be separated from digital systems in order to avoid intersystem grounding problems. Model 945 derives regulated  $\pm 15V$  outputs from any combination of inputs between 23 and 31 volts. The 945 can be powered from dual 12 volt, dual 15 volt,  $\pm 24$  volt or  $\pm 28$  volt power supplies.

#### **DC/DC CONVERTERS FEATURES**

ture range

- Inaudible (>20kHz) converter switching frequency
- Continuous, six-sided EMI/RFI shielding except on
- 1 watt and 1.8 watt models
  Free air convection cooling—no external heat sink or specification derating is required over operating tempera-

- Output short circuit protection (either output to common) for at least 8 hrs. at  $T_A = +71^{\circ}C$
- Automatic restart after short condition removed
- Automatic starting with reverse current injected into outputs

#### **GENERAL SPECIFICATIONS FOR 4.5W, 6W, 12W MODELS**

Line Regulation-full range: ±0.05% max (±0.02% max, 960 series)

Load Regulation-no load to full load: ±0.05% max (±0.02% max, 960 series)

Output Noise and Ripple: 1mV rms maxBreakdown Voltage: 500V dc minimum Input Filter Type:  $\pi$ Operating Temperature Range:  $-25^{\circ}C$  to  $+71^{\circ}C$ Storage Temperature Range:  $-40^{\circ}C$  to  $+100^{\circ}C$ 

### GENERAL SPECIFICATIONS FOR 1W AND 1.8W MODELS Line Regulation-full range: ±0.3% (±1% max, 949)

Load Regulation—no load to full load: 30% (±0.5% max, 949) Output Noise and Ripple: 20mV p-p (with  $15\mu$ F tantalum

capacitor across each output), (1mV rms max, 949) Breakdown Voltage: 300V dc (500V dc min, 949) Input Filter Type:  $\pi$  (models 958, 960, 962, 964) Operating Temperature Range: -25°C to +71°C Storage Temperature Range: -40°C to +100°C

Model	Output Voltag <del>e</del> Volts	Output Current mA	Input Voltage Volts	Input <sup>1</sup> Voltage Range Volts	Input Current Full Load	Output Voltage Error Max	Temperature Coefficient /°C Max	Efficiency Full Load Min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	$2.0 \times 2.0 \times 0.38$
957*	5	100	5	4.5/5.5	200mA	± 5%	$\pm 0.01\%$ (typ)	50%	$1.25 \times 0.8 \times 0.4$
958	5	100	5	4.5/5.5	200mA	±5%	$\pm 0.01\%(typ)$	50%	$1.25 \times 0.8 \times 0.4$
941	±12	±150	5	4.75/5.25	1.17A	±0.5%	±0.01%	58%	$2.0 \times 2.0 \times 0.38$
959*	±12	±40	5	4.5/5.5	384mA	±5%	$\pm 0.01\%$ (typ)	50%	1.25×0.8×0.4
960	±12	±40	5	4.5/5.5	384mA	±5%	$\pm 0.01\%$ (typ)	50%	$1.25 \times 0.8 \times 0.4$
961*	±15	± 33	5	4.5/5.5	396mA	± 5%	$\pm 0.01\%$ (typ)	50%	$1.25 \times 0.8 \times 0.4$
962	±15	±33	5	4.5/5.5	396mA	±5%	$\pm 0.01\%(typ)$	50%	$1.25 \times 0.8 \times 0.4$
963*	±15	±33	12V	10.8/13.2	165mA	±5%	$\pm 0.01\%(typ)$	50%	$1.25 \times 0.8 \times 0.4$
· 964	±15	±33	12V	10.8/13.2	165mA	±5%	±0.01%(typ)	50%	1.25×0.8×0.4
965	±15	±190	5V	4.65/5.5	1.7A	±1%	±0.005%(typ)	62%(typ)	$2.0 \times 2.0 \times 0.38$
966	±15	±190	12V	11.2/13.2	710mA	±1%	±0.005%(typ)	62%(typ)	$2.0 \times 2.0 \times 0.38$
967	±15	± 190	24V	22.3/26.4	350mA	±1%	±0.005%(typ)	62%(typ)	$2.0 \times 2.0 \times 0.38$
968	±15	±190	28V	26/30.8	300mA	±1%	$\pm 0.005\%$ (typ)	62%(typ)	$2.0 \times 2.0 \times 0.38$
949	±15	±60**	5	4.65/5.5	0.6A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35A	±0.5%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250mA	±0.5%	$\pm 0.01\%$	61%	$2.0 \times 2.0 \times 0.38$
951	±15	±410	5	4.65/5.5	3.7A	±0.5%	±0.01%	62%	$3.5 \times 2.5 \times 0.88$

SPECIFICATIONS (typical @ +25°C over the full range of input voltages unless otherwise noted)

NOTES

\*Unfiltered Models

\*\*Single-ended or unbalanced operation is permissible such that total output current load

does not exceed a total of 120mA.

<sup>1</sup>Models 940 and 941 will deliver up to 120mA output current (and model 943 will deliver up to 600mA) over an input voltage range of 4.65 and 5.5 V dc.

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•New product since publication of 1982-1983 Databook Update.

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•New product since publication of 1982-1983 Databook Update.

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•New product since publication of 1982–1983 Databook Update. DACPORT is a registered trademark of Analog Devices, Inc.

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•New product since publication of 1982-1983 Databook Update.

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### Product Families Not in This Databook (But Still Available)

The information published in this Databook is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs or in designs for which they are uniquely suitable. Data sheets on these products are available upon request.

AD108A/208A/308A       ADC-8S       DAS1151       THS-0225       424         AD111/211/311       ADC-10Z       MAS-0801       40       426         AD351       ADC-12QZ       MAS-0801       40       426         AD370/371       ADC-14/17I       MDA-10Z       43       432         AD502       ADC-16Q       MDH-0870       44       433         AD511       ADC1100       MDH-1001       45       434         AD512       ADC1102       MDH-1001       45       434         AD514       ADC1103       MDS-0815       48       436         AD520       ADC1109       MDS-1020       105       441         AD523       ADC1111       MDS-1020       105       441         AD528       ADC1111       MDS-1020       105       441         AD530       ADC1133       MDS-1240       119       452         AD540       AD6200       MDSL-1025       141       454         AD540       AD6201       MDSL-1025       144       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD2003       DAC-QG       RTI-1201       180       610	AD108/208/308	ADC-QU	DAS1150	THS-0060	311
AD111/211/311       ADC-10Z       MAS-0801       40       426         AD351       ADC-12QZ       MAS-1001       42       428         AD370/371       ADC-14U/17I       MDA-10Z       43       432         AD502       ADC-16Q       MDH-0870       44       433         AD511       ADC1100       MDH-1001       45       434         AD512       ADC1102       MDH-1202       46       435         AD514       ADC1103       MDS-0815       48       436         AD520       ADC1105       MDS-0815       48       436         AD523       ADC1109       MDS-1020       105       441         AD530       ADC1133       MDS-1240       119       452         AD531       ADG200       MDSL-0825       141       454         AD540       ADG201       MDSL-1250       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD2003       DAC-QG       RTI-1200       165       606         AD2004       RTI-1200       165       606       606         AD2005       DAC-QS       RTI-1201       180       610 <td< td=""><td>AD108A/208A/308A</td><td>ADC-8S</td><td>DA\$1151</td><td>THS-0225</td><td>424</td></td<>	AD108A/208A/308A	ADC-8S	DA\$1151	THS-0225	424
AD351       ADC-12QZ       MAS-1001       42       428         AD370/371       ADC-14/171       MDA-10Z       43       432         AD502       ADC-16Q       MDH-10870       44       433         AD511       ADC1100       MDH-1001       45       434         AD512       ADC1102       MDH-1202       46       435         AD514       ADC1103       MDS-0815       48       436         AD520       ADC1105       MDS-0815E       52       440         AD523       ADC1109       MDS-1020       105       441         AD528       ADC1111       MDS-1020E       118       450         AD530       ADC1133       MDS-1240       119       452         AD540       ADG200       MDSL-1035       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD2003       DAC-QG       RTI-1200       165       606         AD2003       DAC-QG       RTI-1201       180       610         AD2009       DAC-QZ       RTI-1201       183       751         AD2002       DAC-QZ       RTI-1221       230       756         A	AD111/211/311	ADC-10Z	MAS-0801	40	426
AD370/371       ADC-141/17I       MDA-10Z       43       432         AD502       ADC-16Q       MDH-0870       44       433         AD511       ADC110Q       MDH-1001       45       434         AD512       ADC1102       MDH-1202       46       435         AD514       ADC1103       MDS-0815E       52       440         AD520       ADC1105       MDS-1020       105       441         AD523       ADC1109       MDS-1020       105       441         AD528       ADC1111       MDS-1020E       118       450         AD530       ADC1133       MDS-1240       119       452         AD531       AD6200       MDSL-1250       141       454         AD540       AD6201       MDSL-1035       146       456         AD503       DAC-QG       RTI-1200       165       606         AD2003       DAC-QG       RTI-1202       183       751         AD2009       DAC-QZ       RTI-1202       184       752         AD2020       DAC-10DF       SCM1677       232       934         AD2033       DAC102       SDC1604       233       942         AD2033	AD351	ADC-12QZ	MAS-1001	42	428
AD502       ADC-16Q       MDH-0870       44       433         AD511       ADC1100       MDH-1001       45       434         AD512       ADC1102       MDH-1202       46       435         AD514       ADC1103       MDS-0815       48       436         AD520       ADC1105       MDS-0815E       52       440         AD523       ADC1111       MDS-1020       105       441         AD530       ADC1113       MDS-1020E       118       450         AD530       ADC1133       MDS-1240       119       452         AD531       ADG200       MDSL-0825       141       454         AD540       ADG201       MDSL-1250       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD801       DAC-M       RTI-1200       165       606         AD2003       DAC-QG       RTI-1201       180       610         AD2020       DAC-QK       RTI-1202       183       751         AD2020       DAC-QZ       RTI-1220       184       752         AD2020       DAC-10Z       SCM1677       232       934         AD2023 <td>AD370/371</td> <td>ADC-14I/17I</td> <td>MDA-10Z</td> <td>43</td> <td>432</td>	AD370/371	ADC-14I/17I	MDA-10Z	43	432
ADS11       ADC1100       MDH-1001       45       434         ADS12       ADC1102       MDH-1202       46       435         ADS14       ADC1103       MDS-0815       48       436         AD520       ADC1105       MDS-0815E       52       440         AD523       ADC1109       MDS-1020       105       441         AD528       ADC1133       MDS-1200E       118       450         AD530       ADC100       MDSL-0825       141       454         AD540       ADG200       MDSL-0825       141       454         AD540       ADG201       MDSL-1035       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD801       DAC-M       RTI-1200       165       606         AD2003       DAC-QG       RTI-1201       180       610         AD2009       DAC-QS       RTI-1202       183       751         AD2020       DAC-QS       RTI-1220       184       752         AD2033       DAC-10DF       SDC1604       233       942         AD2033       DAC1009       SHA-1A       260       944         AD7513 </td <td>AD502</td> <td>ADC-16Q</td> <td>MDH-0870</td> <td>44</td> <td>433</td>	AD502	ADC-16Q	MDH-0870	44	433
ADS12       ADC1102       MDH-1202       46       435         AD514       ADC1103       MDS-0815       48       436         AD520       ADC1105       MDS-0815E       52       440         AD523       ADC1109       MDS-1020       105       441         AD528       ADC1111       MDS-1020E       118       450         AD530       ADC1133       MDS-1240       119       452         AD540       ADG200       MDSL-1035       146       456         AD540       ADG201       MDSL-1035       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD2003       DAC-QG       RTI-1200       165       606         AD2008       DAC-QG       RTI-1201       180       610         AD2009       DAC-QS       RTI-1201       184       752         AD2020       DAC-QZ       RTI-1221       230       756         AD2023       DAC-10DF       SCM1677       232       934         AD7513       DAC102       SDA-102       33       942         AD7513       DAC1106       SHA-2A       261       946         AD7519<	AD511	ADC1100	MDH-1001	45	434
AD514       ADC1103       MDS-0815       48       436         AD520       ADC1105       MDS-0815E       52       440         AD523       ADC1109       MDS-10200       105       441         AD528       ADC1111       MDS-1020E       118       450         AD530       ADC1133       MDS-1240       119       452         AD531       AD6200       MDSL-0825       141       454         AD540       AD6201       MDSL-1035       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD2003       DAC-QG       RTI-1200       165       606         AD2008       DAC-QG       RTI-1201       180       610         AD2009       DAC-QZ       RTI-1202       183       751         AD2020       DAC-QZ       RTI-1220       184       752         AD2033       DAC-10Z       SDC1604       233       942         AD2033       DAC1009       SHA-1A       260       944         AD7513       DAC108       SHA-3       272       947         AD7527       DAC1108       SHA-4       273       956         AD7544 <td>AD512</td> <td>ADC1102</td> <td>MDH-1202</td> <td>46</td> <td>435</td>	AD512	ADC1102	MDH-1202	46	435
AD520       ADC1105       MDS-0815E       52       440         AD523       ADC1109       MDS-1020       105       441         AD528       ADC1111       MDS-1020E       118       450         AD530       ADC1133       MDS-1240       119       452         AD531       ADG200       MDSL-0825       141       454         AD540       ADG201       MDSL-1035       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD2003       DAC-QG       RTI-1200       165       606         AD2009       DAC-QG       RTI-1201       180       610         AD2009       DAC-QS       RTI-1202       183       751         AD2020       DAC-QZ       RTI-1220       184       752         AD2020       DAC-10Z       SDC1604       233       942         AD2033       DAC109       SHA-1A       260       944         AD7513       DAC106       SHA-2A       261       946         AD7513       DAC108       SHA-3       272       947         AD7527       DAC118       SHA-4       273       956         AD7555	AD514	ADC1103	MDS-0815	48	436
AD523       ADC1109       MDS-1020       105       441         AD528       ADC1111       MDS-1020E       118       450         AD530       ADC1133       MDS-1240       119       452         AD531       ADG200       MDSL-10825       141       454         AD540       ADG201       MDSL-1035       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD801       DAC-M       RTI-1200       165       606         AD2003       DAC-QG       RTI-1201       180       610         AD2009       DAC-QG       RTI-1202       183       751         AD2020       DAC-QK       RTI-1220       184       752         AD2020       DAC-QZ       RTI-1221       230       756         AD2022       DAC-10DF       SCM1677       232       934         AD2033       DAC1002       SDC1604       233       942         AD2033       DAC108       SHA-1A       260       944         AD7513       DAC1108       SHA-4       273       956         AD7519       DAC1108       SHA-3       272       947         AD7557 <td>AD520</td> <td>ADC1105</td> <td>MDS-0815E</td> <td>52</td> <td>440</td>	AD520	ADC1105	MDS-0815E	52	440
AD528       ADC1111       MDS-1020E       118       450         AD530       ADC1133       MDS-1240       119       452         AD531       AD6200       MDSL-0825       141       454         AD540       ADG201       MDSL-1035       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD801       DAC-M       RTI-1200       165       606         AD2003       DAC-QG       RTI-1201       180       610         AD2008       DAC-QK       RTI-1202       183       751         AD2009       DAC-QS       RTI-1220       184       752         AD2020       DAC-QCS       RTI-1221       230       756         AD2022       DAC-10DF       SCM1677       232       934         AD2033       DAC102       SDC1604       233       942         AD7513       DAC1106       SHA-2A       261       946         AD7519       DAC1108       SHA-3       272       947         AD7527       DAC1108       SHA-4       273       956         AD7555       DAC1132       SHA-114       276       407         AD7570 <td>AD523</td> <td>ADC1109</td> <td>MDS-1020</td> <td>105</td> <td>441</td>	AD523	ADC1109	MDS-1020	105	441
AD530ADC1133MDS-1240119452AD531ADG200MDSL-0825141454AD540ADG201MDSL-1035146456AD559BDM1615/1616/1617MDSL-1250148605AD801DAC-MRTI-1200165606AD2003DAC-QGRTI-1201180610AD2009DAC-QKRTI-1202183751AD2009DAC-QSRTI-1220184752AD2020DAC-QZRTI-1221230756AD2022DAC-10DFSCM1677232934AD2033DAC1009SHA-1A260944AD7513DAC106SHA-2A261946AD7519DAC1108SHA-3272947AD7527DAC118SHA-4273956AD7555DAC1132SHA-1114276AD7570DAC1420SHA-1134285AD7583DAC1423THC-0750288	AD528	ADC1111	MDS-1020E	118	450
AD531ADG200MDSL-0825141454AD540ADG201MDSL-1035146456AD559BDM1615/1616/1617MDSL-1250148605AD801DAC-MRTI-1200165606AD2003DAC-QGRTI-1201180610AD2008DAC-QKRTI-1202183751AD2009DAC-QSRTI-1221230756AD2020DAC-QZRTI-1221230756AD2023DAC-10DFSCM1677232934AD2033DAC102SDC1604233942AD2033DAC108SHA-1A260944AD7513DAC1106SHA-2A261946AD7519DAC118SHA-3272947AD7555DAC1132SHA-1114276AD7570DAC1420SHA-1134285AD7583DAC1423THC-0750288	AD530	ADC1133	MDS-1240	119	452
AD540       ADG201       MDSL-1035       146       456         AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD801       DAC-M       RTI-1200       165       606         AD2003       DAC-QG       RTI-1201       180       610         AD2008       DAC-QM       RTI-1202       183       751         AD2009       DAC-QS       RTI-1220       184       752         AD2020       DAC-QZ       RTI-1221       230       756         AD2023       DAC-10DF       SCM1677       232       934         AD2033       DAC102       SDC1604       233       942         AD2033       DAC102       SDC1604       233       942         AD7513       DAC108       SHA-1A       260       944         AD7519       DAC118       SHA-3       272       947         AD7527       DAC118       SHA-3       272       947         AD7555       DAC1132       SHA-1114       276       956         AD7544       DAC1420       SHA-1134       285       407576         AD7583       DAC1423       THC-0750       288       ADC-QM       ADC1423       TH	AD531	ADG200	MDSL-0825	141	454
AD559       BDM1615/1616/1617       MDSL-1250       148       605         AD801       DAC-M       RTI-1200       165       606         AD2003       DAC-QG       RTI-1201       180       610         AD2008       DAC-QM       RTI-1202       183       751         AD2009       DAC-QS       RTI-1220       184       752         AD2020       DAC-QZ       RTI-1221       230       756         AD2022       DAC-10DF       SCM1677       232       934         AD2033       DAC102       SDC1604       233       942         AD2033       DAC1009       SHA-1A       260       944         AD7513       DAC1106       SHA-2A       261       946         AD7519       DAC1108       SHA-3       272       947         AD7527       DAC118       SHA-4       273       956         AD7544       DAC1125       SHA-114       276       407         AD7570       DAC1420       SHA-1134       285       407583         AD7583       DAC1423       THC-0750       288       402-403	AD540	ADG201	MDSL-1035	146	456
AD801         DAC-M         RTI-1200         165         606           AD2003         DAC-QG         RTI-1201         180         610           AD2008         DAC-QM         RTI-1202         183         751           AD2009         DAC-QS         RTI-1220         183         752           AD2020         DAC-QZ         RTI-1220         184         752           AD2020         DAC-QZ         RTI-1221         230         756           AD2023         DAC-10DF         SDC1604         233         942           AD2033         DAC1009         SHA-1A         260         944           AD7513         DAC1106         SHA-2A         261         946           AD7519         DAC1108         SHA-3         272         947           AD7527         DAC1118         SHA-4         273         956           AD7544         DAC1125         SHA-114         276         275           AD7570         DAC1420         SHA-1134         285         288           AD7583         DAC1423         THC-0750         288         310	AD559	BDM1615/1616/1617	MDSL-1250	148	605
AD2003         DAC-QG         RTI-1201         180         610           AD2008         DAC-QM         RTI-1202         183         751           AD2009         DAC-QS         RTI-1220         184         752           AD2020         DAC-QZ         RTI-1221         230         756           AD2022         DAC-10DF         SCM1677         232         934           AD2023         DAC-10Z         SDC1604         233         942           AD2033         DAC1009         SHA-1A         260         944           AD7513         DAC1106         SHA-2A         261         946           AD7519         DAC1108         SHA-3         272         947           AD7527         DAC1108         SHA-4         273         956           AD7555         DAC1125         SHA-5         275         947           AD7555         DAC1132         SHA-1114         276         76           AD7570         DAC1420         SHA-1134         285         75           AD7583         DAC1423         THC-0750         288         75	AD801	DAC-M	RTI-1200	165	606
AD2008         DAC-QM         RTI-1202         183         751           AD2009         DAC-QS         RTI-1220         184         752           AD2020         DAC-QZ         RTI-1221         230         756           AD2022         DAC-10DF         SCM1677         232         934           AD2023         DAC-10Z         SDC1604         233         942           AD2033         DAC1009         SHA-1A         260         944           AD7513         DAC1106         SHA-2A         261         946           AD7519         DAC1108         SHA-3         272         947           AD7527         DAC1118         SHA-4         273         956           AD7555         DAC1125         SHA-5         275           AD7570         DAC1420         SHA-1114         276           AD7583         DAC1422         THC-0750         288           ADC-QM         DAC1423         THC-1500         310	AD2003	DAC-QG	RTI-1201 .	180	610
AD2009         DAC-QS         RTI-1220         184         752           AD2020         DAC-QZ         RTI-1221         230         756           AD2022         DAC-10DF         SCM1677         232         934           AD2023         DAC-10Z         SDC1604         233         942           AD2033         DAC1009         SHA-1A         260         944           AD7513         DAC1106         SHA-2A         261         946           AD7519         DAC1108         SHA-3         272         947           AD7527         DAC1118         SHA-4         273         956           AD7555         DAC1125         SHA-5         275           AD7570         DAC1420         SHA-1134         285           AD7583         DAC1422         THC-0750         288	AD2008	DAC-QM	RTI-1202	183	751
AD2020         DAC-QZ         RTI-1221         230         756           AD2022         DAC-10DF         SCM1677         232         934           AD2023         DAC-10Z         SDC1604         233         942           AD2033         DAC1009         SHA-1A         260         944           AD7513         DAC1106         SHA-2A         261         946           AD7519         DAC1108         SHA-3         272         947           AD7527         DAC1118         SHA-4         273         956           AD7555         DAC1125         SHA-5         275           AD7570         DAC1420         SHA-1134         285           AD7583         DAC1422         THC-0750         288           ADC-QM         DAC1423         THC-1500         310	AD2009	DAC-QS	RTI-1220	184	752
AD2022         DAC-10DF         SCM1677         232         934           AD2023         DAC-10Z         SDC1604         233         942           AD2033         DAC1009         SHA-1A         260         944           AD7513         DAC1106         SHA-2A         261         946           AD7519         DAC1108         SHA-3         272         947           AD7527         DAC1118         SHA-4         273         956           AD7555         DAC1132         SHA-1114         276           AD7570         DAC1420         SHA-1134         285           AD7583         DAC1423         THC-0750         288	AD2020	DAC-QZ	RTI-1221	230	756
AD2023         DAC-10Z         SDC1604         233         942           AD2033         DAC1009         SHA-1A         260         944           AD7513         DAC1106         SHA-2A         261         946           AD7519         DAC1108         SHA-3         272         947           AD7527         DAC1118         SHA-4         273         956           AD7555         DAC1132         SHA-1114         276           AD7570         DAC1420         SHA-1134         285           AD7583         DAC1423         THC-0750         288	AD2022	DAC-10DF	SCM1677	232	934
AD2033         DAC1009         SHA-1A         260         944           AD7513         DAC1106         SHA-2A         261         946           AD7519         DAC1108         SHA-3         272         947           AD7527         DAC1118         SHA-4         273         956           AD7555         DAC1132         SHA-114         276           AD7570         DAC1420         SHA-1134         285           AD7583         DAC1423         THC-0750         288	AD2023	DAC-10Z	SDC1604	233	942
AD7513DAC1106SHA-2A261946AD7519DAC1108SHA-3272947AD7527DAC1118SHA-4273956AD7544DAC1125SHA-5275AD7555DAC1132SHA-1114276AD7570DAC1420SHA-1134285AD7583DAC1422THC-0750288ADC-QMDAC1423THC-1500310	AD2033	DAC1009	SHA-1A	260	944
AD7519DAC1108SHA-3272947AD7527DAC1118SHA-4273956AD7544DAC1125SHA-5275AD7555DAC1132SHA-1114276AD7570DAC1420SHA-1134285AD7583DAC1422THC-0750288ADC-QMDAC1423THC-1500310	AD7513	DAC1106	SHA-2A	261	946
AD7527DAC1118SHA-4273956AD7544DAC1125SHA-5275AD7555DAC1132SHA-1114276AD7570DAC1420SHA-1134285AD7583DAC1422THC-0750288ADC-QMDAC1423THC-1500310	AD7519	DAC1108	SHA-3	272	947
AD7544DAC1125SHA-5275AD7555DAC1132SHA-1114276AD7570DAC1420SHA-1134285AD7583DAC1422THC-0750288ADC-QMDAC1423THC-1500310	AD7527	DAC1118	SHA-4	273	956
AD7555DAC1132SHA-1114276AD7570DAC1420SHA-1134285AD7583DAC1422THC-0750288ADC-QMDAC1423THC-1500310	AD7544	DAC1125	SHA-5	275	
AD7570DAC1420SHA-1134285AD7583DAC1422THC-0750288ADC-QMDAC1423THC-1500310	AD7555	DAC1132	SHA-1114	276	
AD7583         DAC1422         THC-0750         288           ADC-QM         DAC1423         THC-1500         310	AD7570	DAC1420	SHA-1134	285	
ADC-QM DAC1423 THC-1500 310	AD7583	DAC1422	THC-0750	288 .	
	ADC-QM	DAC1423	THC-1500	310	

### Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but-as a rule-they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, get in touch with Analog Devices.

	Closest		Closest
	Recommended		Recommended
Model	Equivalent	Model -	Equivalent
AD501	AD511	47	48
AD505	AD509	101 (module)	45
AD508	AD517	102	48
AD513	AD503	106	118
AD516	AD506	107	118
AD550	None	108	52
AD551	None	110	48
AD553	None	111	AD308
AD555	AD7519	114	119
AD810-813	None	115	43
AD814-816	None	120	50
AD818	None	142	48
AD820-822	None	142	52
AD830-833	None	145	50
AD835-839	None	142	AD517
A D840-842	None	155	165
A D7516		101	165
ADC1121	AD7550	105	105
ADM501	ADM501/506	170	1/1
ADM301	ADM301/300	220	234
ADP301	ADF311	231	255
DAC-IOH	DAC-102	2/4J	284J
DACITIZ	DACIZOS	279	2861
DACITZZ	AD/541	280	281
IDC1703	IRDC1730/1731	282]	292A
MDA-LB	None	283	292A
MDA-LD	None	301 (module)	52
MDA-UB	None	302	310 (module)
MDA-UD	None	350	None
MDA-8H	MDA-10Z	427	424
MDA-10H	MDA-10Z	602J10	AD524
MDA-11MF	AD7521	602J100	AD524
MDS-0830	HDS-0820	602K100	AD524
MDS-0850	HDS-0820	603	AD524
MDS-1040	HDS-1025	901	904
MDS-1080	HDS-1025	907	921
MDSL-0802	HDS-0820	908	921
MDSL-1002	HDS-1025	909	921
MDSL-1201	HDS-1250	931	None
SERDEX	μMAC-5000	932	None /
SHA-6	SHA1144	933	None
TSDC1608-1611	TSL1612	935	None
2N3954	None	948	947
2N5900	None	971	921
41	AD515	AD612	AD524
		AD614	AD524

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A 12-page short-form guide to analog-digital conversion products for synchros, resolvers, and Inductosyns<sup>\*</sup>, in forms ranging from hybrid ICs to instruments and systems.

### APPLICATION GUIDE FOR ISOLATION AMPLIFIERS

A 16-page guide to specifications and applications of isolation amplifiers for industrial, instrumentation, and medical applications.

### APPLICATION GUIDE TO CMOS MULTIPLYING D-TO-A CONVERTERS

This guide includes detailed information on the internal design and successful application of CMOS MDACs. Typical circuits discussed include measurement, function generation, programmable filters, and control of audio signals.

### A COOKBOOK TO DIGITAL FILTERING AND OTHER DSP APPLICATIONS

A collection of reprints of papers that originally appeared in EDN Magazine, during 1983. Topics include FIR filtering, temporal averaging, multiband filters, IIR filtering, and implementing modern control theory with digital signal processing.

### DESIGNER'S GUIDE TO HIGH-RESOLUTION PRODUCTS

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### BOOKS

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